Supertex inc.

Leadership in CMOS/DMOS Technologies

Databook 1993–1994

High Voltage Integrated Circuits and DMOS Transistors

Supertex inc.

Leadership in CMOS/DMOS Technologies

DATABOOK

1993–1994

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Supertex inc.

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Supertex inc.

Product Nomenclature/Ordering Information

DMOS Proprietary Products

SX V N 01 09 N3

HI-REL	FAMILY TYPE	POLARITY	FAMILY NUMBER	BVDSS DIVIDED BY 10	PACKAGE TYPE
SX = Similar to JANTX	A = Lateral DMOS Arrays	N = N-Channel	01	01	N1 = TO-3
SXV = Similar to JANTXV	D = Vertical Depletion-Mode DMOS Discretes	P = P-Channel	03	02	N2 = TO-39
SJ = Similar to JAN	L = Lateral DMOS Discretes (Depletion-Mode and Enhance-ment-Mode)	C = Complementary (2N & 2P)	05	04	N3 = TO-92
SC = Commercial Burn-in	T = Low Threshold DMOS Discretes	Q = Arrays	06	06	N5 = TO-220
RB = MIL-STD-883 for Arrays	V = Vertical DMOS Discretes & Quads		07	09	N6 = 14 Pin Plastic DIP
			11	10	N7 = 14 Pin Ceramic DIP
			12	16	N8 = TO-243AA(SOT-89)
			13	20	N9 = TO-52
			21	24	NA = 18 Pin Plastic DIP
			22	30	ND = Die in Waffle Pack
			25	35	NF = 20 Terminal Ceramic LCC
			26	40	NW = Die in Wafer Form
				45	WG = 20 Lead SOW
				50	
				55	
				60	
				(e.g., 09 = 90V)	

CMOS Products

Encoder/Decoder

ED - 5 P

FAMILY TYPE	NUMBER OF ADDRESS BITS	PACKAGE TYPE
ED = Programmable Encoder/Decoder	ED-5 = 5	PJ = Molded Plastic Surface Mount J-Lead Chip Carrier
DC = Data Coder	DC-7 = 7	P = Molded Plastic DIP
ET = Encoder/ Transmitter	ED-9 = 9	X = Dice
	ED-11 = 11	WG = Small Outline Surface Mount
	ET-13 = 13	
	ED-15 = 15	

Smoke Detectors

S D 2 P

FAMILY TYPE

SD = Smoke Detectors

PRODUCT DESIGNATOR

2

PACKAGE TYPE

P = Molded Plastic DIP

X = Dice

HVIC Products

RB HV 54 08 DJ

HI-REL

RB = MIL-STD-883 processing

RC = MIL-STD-883 processing except burn-in

FAMILY TYPE

HV = High Voltage IC

PRODUCT DESIGNATOR

03	45	93
04	46	94
05	49	97
06	51	98
10	52	217
12	53	218
14	54	227
15	55	228
16	56	341
18	57	343
21	58	345
22	60	348
25	65	500
26	68	501
30	70	518
31	72	577
33	77	622
34	78	701
35	83	702
36	84	711
38	87	712
41	88	
42	91	

ABSOLUTE MAX VOLTAGE DIVIDED BY 10

04	18
06	20
08	22
10	25
12	27
14	30
16	37

(e.g., 22 = 220V)

PACKAGE TYPE

P = Plastic DIP

C = Ceramic Side Brazed

D = CERDIP

T = T.A.B. Tape

X = Dice

CS = Ceramic Chip Carrier - STD Bent Leads

DG = CERDIP Gullwing

NG = Narrow Body Gullwing

PG = Plastic Gullwing

WG = S.O.W. Gullwing

DJ = Quad CERDIP J Lead

PJ = Quad Plastic J Lead

Success Through Innovation

Supertex designs and manufactures complex proprietary and industry-standard integrated circuits (ICs). Our customers include the medical, data processing, military, telecommunications, instrumentation, and consumer product industries. Throughout the years the company has developed several advanced technologies utilizing high-performance Complementary Metal Oxide Semiconductors (CMOS) and Double-Diffused MOS (DMOS) processes.

In 1980, Supertex pioneered high voltage integrated circuitry with its proprietary HVCMOS® technology, a merging of the CMOS and DMOS process technologies onto one chip. Supertex HVCMOS chips have the "brains" and low power consumption of CMOS ICs and the high voltage output of DMOS FET transistors.

These advanced HVCMOS ICs, as well as Supertex's families of CMOS and DMOS products, provide performance and cost benefits, giving customers a competitive edge in developing their products.

Supertex now focuses on two process technologies, DMOS and HVCMOS, which allows for a diversified product mix of integrated circuits and MOS field effect transistors (FETs) and arrays. The Company's products are targeted for application-specific markets such as ultrasound imaging for medical electronics, flat-panel display terminals and high reliability products for military systems. Supertex has earned domestic as well as international recognition as a demonstrated technological leader in high voltage semiconductor products.

Product Development Milestones

Supertex has continued the commitment to product and technological development to enhance and complement our existing product lines. Supertex is a recognized world leader in high voltage ICs and MOSFET innovations. While responding to market demands for state-of-the-art products, the Company maintains a leadership position as an industry innovator, evidenced by the product development milestones listed below:

1976 Industry leader in CMOS wafer foundry technology and production.

1977 Patent filed for silicon-gate high power VMOS process.

First in the industry to introduce both N and P-channel silicon-gate VMOS power FETs.

1978 State-of-the-art high voltage 500V power VMOS FET introduced.

1979 Development of combined bipolar and DMOS technologies (Superfet™).

High Voltage DMOS/CMOS IC technology developed for medical ultrasonic imaging applications.

Widest product offering for CMOS encoder/decoder ICs, using Manchester coding.

1980 First in the industry to introduce high voltage DMOS lateral arrays.

1981 First to develop fully TTL-compatible CMOS logic ICs.

1982 First fully integrated electroluminescent (EL) flat panel display driver chip set, including gray scales.

1983 First to introduce 64-line density EL display driver ICs.

1984 First HVCMOS IC to be used in a major plotter program.

MVIC (40-volt) and HVIC technologies developed for wafer foundry production.

1985 First Hi-Rel HVCMOS display driver IC in the industry.

Introduction of industry's first low threshold N-channel power MOSFET family.

1986 Introduction of low cost, low power 32-channel flat panel display driver ICs.

Introduction of industry's first low threshold P-channel power MOSFET family.

First to introduce 8-channel high voltage level translator chip.

1987 Introduction of 32-channel complements (N and P-channel) for high voltage, high current push-pull applications.

Introduction of low power 32-channel AC plasma flat panel display driver ICs.

1988 Introduction of 32-channel 300V complementary (N and P-channel) high voltage ICs for electrostatic plotters and ATE bareboard testers.

Joint market introduction of microprocessor supervisory chips.

Introduction of first commercial gray-shade/video analog display driver ICs.

(continued)

Product Development Milestones (continued)

1989 Introduction of second generation low power high voltage analog multiplexers with CMOS control logic.

Introduction of single chip 225V push-pull IC with CMOS control logic.

Introduction of 64-channel second generation 80V push-pull ICs with CMOS control logic and 400V open drain ICs.

1990 Implementation of macro-cell custom capability in high voltage ICs.

Introduction of ultralow threshold DMOS discrete transistors for Ni-Cad and other battery operated applications.

1992 Introduction of current mode power supply family utilizing high and low voltage bi-CMOS processes.

Custom Wafer Foundry

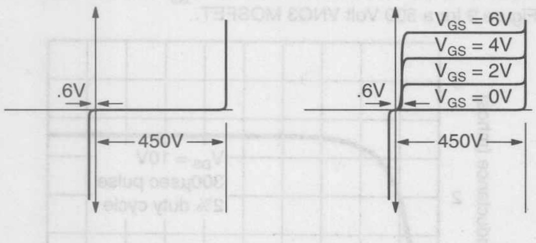
Supertex specializes in HVCMOS and DMOS Wafer Foundry production providing state-of-the-art wafer fabrication for Customer-Owned-Tooling (COT) production. Standard as well as modified processes can be produced per specific customer requirements. Engineering and pre-production volumes can be run with very short throughput times. Supertex can also support the customers' needs for back-end packaging and testing.

In addition, Supertex can also run standard metal-gate CMOS and PMOS processes.

Chapter 3 – Applications Notes

DMOS FET Electrical Performance

The electrical behavior of MOSFETs has been explained by numerous authors. A different, and non-traditional way of viewing their behavior arises when the device structure is closely examined. The source and body regions comprise one side of a diode, with the drain region being the other side. A voltage on the gate allows carriers to flow from source to drain through an induced surface channel. Figure 1A shows the forward and reverse current vs. voltage characteristics of a diode, while Figure 1B shows the current vs. voltage characteristics of a MOSFET.



A. Diode Characteristics B. Gated Diode Characteristics

Figure 1

A MOSFET is characterized by a set of parameters different in many ways from a bipolar transistor. The parameters specified in a MOSFET data sheet are defined and briefly explained below:

A. $V_{GS(TH)}$ – The gate threshold voltage. It is defined as the voltage from gate to source required to produce a specified drain current. For ease of measuring, the drain is commonly shorted to the gate. (The measurement circuit is shown in Figure 2.)

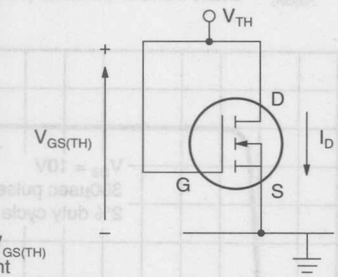


Figure 2:
N-Channel $V_{GS(TH)}$ Measurement

Threshold current is usually measured at a current in the range of 1 to 10mA. (Threshold voltage measurement can be normalized to the amount of source perimeter when comparing different size transistors. Full current is usually obtained at $V_{GS} = V_{GS(TH)} + 8$ volts (N-channel). The threshold voltage is a function of temperature as shown in Figure 3 for a 500 volt Supertex transistor. The decrease in the measured value of $V_{GS(TH)}$ is primarily caused by thermally generated carriers or leakage current that add to the induced surface current flow, thus decreasing the amount of applied voltage needed to obtain a specified current.

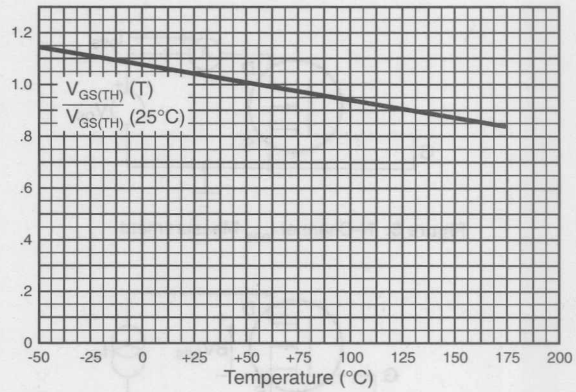


Figure 3:
Normalized $V_{GS(TH)}$ vs. Temperature for the VN03 Transistor

B. I_{GSS} – The gate to body leakage current. It is measured with drain and source at ground, and gate biased to specified voltage. NOTE: Due to input capacitance, large die size MOSFETs may prove difficult to measure with automatic test equipment, unless a preconditioning test is performed to charge the gate capacitance prior to test. (See Figure 4 for the measurement circuit.)

This leakage current results from current flow through the insulating layer of silicon dioxide surrounding the gate. Typical DC-leakage currents are in the picoampere range between the temperatures of -55°C and +200° C. This value is well below the level of concern in most power conversion circuits. When an on-chip diode is incorporated between the gate and the source, the leakage current, which is that of a reverse-biased diode, doubles approximately every 10°C.

C. I_{DSS} – The zero gate voltage drain current or offstate leakage current. It is determined by applying specified voltage from drain to source (with gate shorted to source) and measuring the resulting current. (See Figure 5 for the measurement circuit.)

This leakage current is that of a reverse-biased diode. As with a reverse-biased diode, this current is a measure of the integrity of the structure and may degrade under extremes of voltage and temperature.

D. BV_{DSS} – The breakdown voltage of drain to source with gate shorted to source. It is determined by forcing a specified current from drain to source and measuring the resulting voltage. Properly designed MOSFETs should not have a latchback breakdown and a low current measurement is sufficiently accurate. (See Figure 6 for the measurement circuit.)

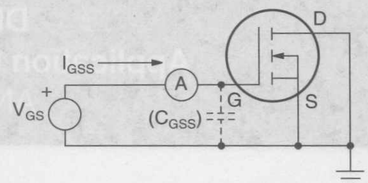


Figure 4: N-Channel I_{GSS} Measurement

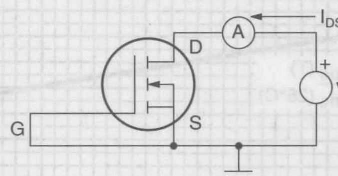


Figure 5: N-Channel I_{DSS} Measurement

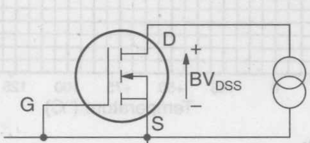


Figure 6: N-Channel BV_{DSS} Measurement

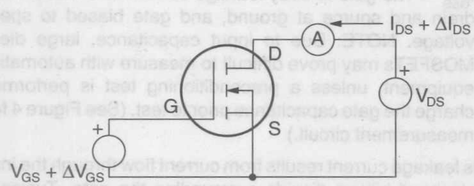


Figure 7: N-Channel G_{fs} Measurement

This parameter is most likely to degrade if exceeded for an extended period of time in high voltage applications, because of the large current (and, hence, high power dissipation that may occur). A lower clamping breakdown voltage diode from source-to-drain will prevent degradation of the parameter.

E. g_{fs} or g_m – The small signal forward transconductance. It is the ratio of $\Delta I_D/\Delta V_{GS}$ measured for a 10% change in drain current at a specified quiescent drain bias point.

This parameter depends on device structure as shown in the equation below (see Figure 7 for measurement circuit):

$$g_m = \frac{\mu off \; Z\epsilon_{OX}}{Lt_{OX}} \left(V_{GS} - V_{GS(TH)}\right)$$

where $\frac{Z}{L}$ = $\frac{\text{Source perimeter}}{\text{Channel length}}$

μ_{off} = Effective carrier mobility

ϵ_{OX} = Gate Dielectric constant

t_{OX} = Gate oxide thickness

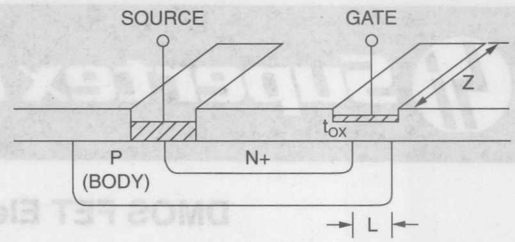


Figure 8: Parameters Affecting MOSFET Transconductance

These parameters are shown in Figure 8. The forward transconductance is proportional to source perimeter, hence proportional to chip area. For a given device area, maximizing the source perimeter results in a maximum value of g_m. This parameter is also increased by decreasing the gate dielectric thickness, but this approach limits the total voltage swing on the gate because of the dielectric strength of silicon dioxide (60V/1000Å of SiO_2). Typical gate oxide thicknesses are in the 1000Å range. In MOSFETs, the transconductance vs. V_{GS} varies as shown in Figure 9 for a 500 Volt VNO3 MOSFET.

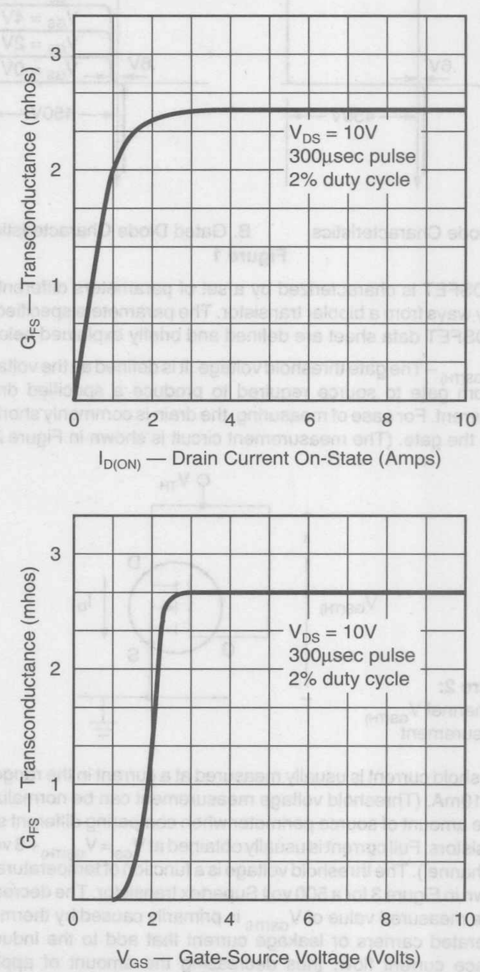


Figure 9: Transconductance vs. Drain Current or Gate-Source Voltage for the VN03

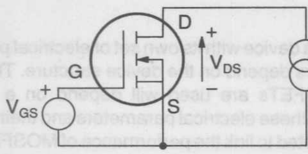


Figure 10: N-Channel $R_{DS(ON)}$ Measurement

F. $R_{DS(ON)}$ – The static drain-source on-state resistance. It is measured as the drain-source voltage divided by the drain current at specified values of drain current and gate source voltage. (See Figure 10 for the measurement circuit.)

The on-state resistance of a high voltage MOSFET is dominated by the resistance of the drain region. For a given breakdown voltage and device area, there is a minimum value of $R_{DS(ON)}$. The variations in source geometrics and body-to-drain breakdown structures discussed earlier are all aimed at realizing this minimum $R_{DS(ON)}$ value. In device operation, $R_{DS(ON)}$ may appear to be considerably higher than at room temperature. This behavior occurs because the heating of the device decreases the carrier mobility, thus reducing the current for a given voltage. This behavior for a 500 volt VNO3 MOSFET is shown in Figure 11. This negative feedback characteristic is the key to MOSFETs thermal stability.

G. $I_{D(ON)}$ – The on-state drain current. It is measured at specified values of drain-source and gate-source voltage. NOTE: To reduce heating of the device, this should be performed in a pulse mode, or with an adequate heat sink. (See Figure 12 for measurement circuit.)

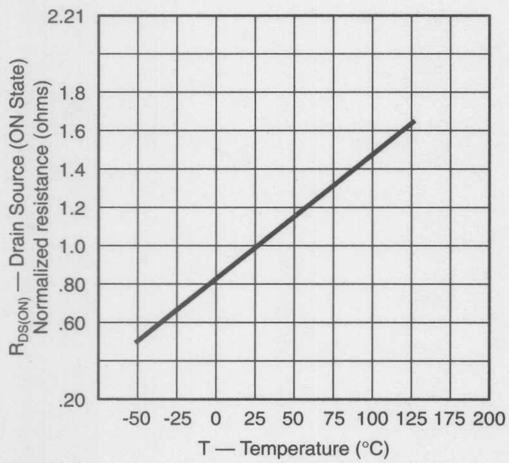


Figure 11: $R_{DS(ON)}$ as a Function of Temperature for the VN03

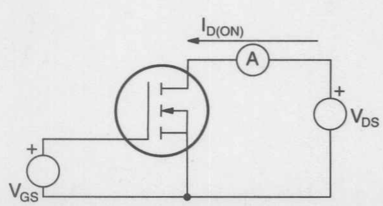


Figure 12: N-Channel $I_{D(ON)}$ Measurement

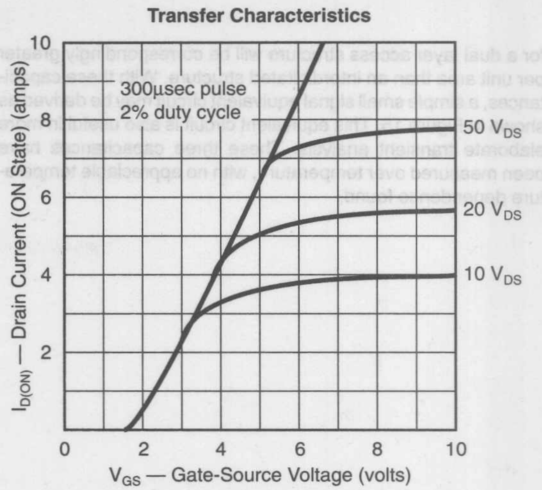


Figure 13: $I_{D(ON)}$ as a function of Gate-Source Voltage for the VN03

The on-state drain current is proportional to the amount of source perimeter and the total chip area. Since current flow causes device heating, the pulsed value of $I_{D(ON)}$ is considerably greater than the steady state value because of the increasing value of $R_{DS(ON)}$ with temperature. This specific behavior is shown by the dotted line for the VNO3 in Figure 13.

H. Capacitances – MOSFETs are characterized by three capacitances:

1. C_{ISS}: Input capacitance
2. C_{OSS}: Common source capacitance
3. C_{RSS}: Reverse transfer capacitance

These measured capacitances are related to device structure as shown in Figure 14. We see from this figure that the value of C_{ISS}

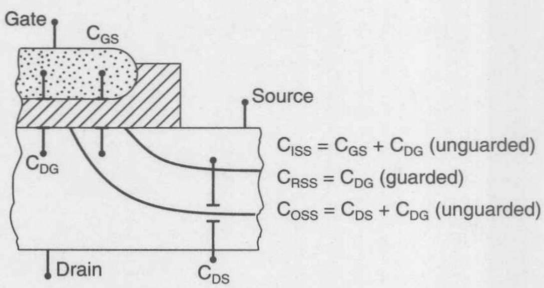


Figure 14: DMOS Transistor Capacitance

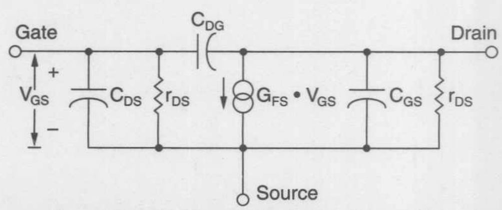


Figure 15: FET Equivalent Circuit—Small Signal

for a dual layer access structure will be correspondingly greater per unit area than an interdigitated structure. With these capacitances, a simple small signal equivalent circuit may be derived as shown in Figure 15. This equivalent circuit is also useful in more elaborate transient analysis. These three capacitances have been measured over temperature, with no appreciable temperature dependence found.

Conclusion

The MOSFET is a device with its own set of electrical parameters. These parameters depend on the device structure. The success with which MOSFETs are used will depend on a designer's understanding of these electrical parameters and their limits. This article has attempted to link the performance of MOSFETs to their optimum design and processing and to establish some physical limits for optimum performance.

Low-Threshold MOSFETs: Structure, Performance and Applications

Since an increasing amount of attention is being focused on system interface from low-level logic, the need for higher current and/or low on-resistance at drive levels of only 3-5 volts has become a major concern. Supertex has always known of the importance of the gate drive consideration and has been offering N-channel low-threshold devices with threshold voltages of 2.4 and 1.6 volts for many years. Additionally, standard and low-threshold versions of P-channel DMOS devices are available. To understand the reasons that low-threshold processing requires very specialized techniques, one needs to understand the DMOS structure.

DMOS Structure

Most double-diffused MOS (DMOS) structures have very similar cross-section characteristics, as shown in Figure 1. For conduction to occur, a channel of electrons is needed between the gate and the source. This potential produces an inversion layer called the channel. The depth of this layer is the limiting factor in allowing current flow between the drain and source terminal. The greater the voltage applied, the deeper the induced channel; resulting in more current flow. The voltage needed to invert the channel region is called the threshold voltage $V_{GS(th)}$. However, when examining most manufacturers' databooks, one finds $V_{GS(th)}$ defined as the voltage needed to produce a specified drain current (I_D). This differs from the theoretical definition of knowing when a channel is produced, which is of little interest to MOSFET users. Comparing $V_{GS(th)}$ at the same I_D simplifies the analysis of databook parametric guarantees, allowing the designer to compare the product to actual needs.

The control of the threshold voltage is dependent on many factors, such as dopant concentration, gate-to-silicon work function and surface change. The greater the body dopant concentration, the larger the applied voltage needed to produce a channel, which translates to a higher threshold voltage. One method of reducing threshold voltage is to reduce the body dopant concentration until the required $V_{GS(th)}$ is met. This technique by itself is dangerous because it degrades other device parameters. The first and most important of these is drain-source breakdown (BV_{DSS}), which is a result of certain conditions, most commonly punch-through.

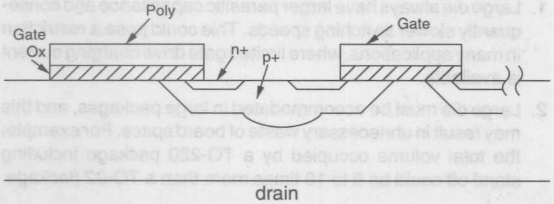


Figure 1: Double Diffused MOS (DMOS)

Punch-through is defined as the drain voltage needed to create an electric field connecting the drain and source, as shown in Figure 2, at voltages less than the actual BV_{DSS} rating.

The susceptibility to punch-through increases dramatically as the body dopant concentration is lowered. There is an optimum body dopant level that is needed in order to stay away from the punch-through mechanism, but this concentration is too high for low thresholds. This is one of the reasons why P-channel devices typically have higher thresholds, because the optimum body dosage is higher than N-channel FETs.

Another technique, used by some manufacturers, is to lower threshold by reducing the gate oxide thickness. Again, there are trade-offs using this method: (1) The input capacitance increases which will effect the switching speed efficiency and (2) the maximum gate voltage rating is decreased, making it more susceptible to input voltage spikes.

Supertex has developed a proprietary technique to successfully lower threshold voltage without these major trade-offs. This method mainly depends on modifying the diffusion profile and altering the charge distribution to produce low-threshold N- and P-channel devices. This process, which makes use of Supertex's interdigitated design structure, allows typical thresholds of 1.1 volts for N-channel and 1.8 volts for P-channel, DMOS devices.

An added benefit of Supertex's design is the lower input capacitance achieved by the interdigitated geometry, rather than the more conventional closed cell approach. Less charge is needed to control the device input. Therefore, it can be concluded that a lower threshold device will start conducting earlier for a given gate drive and allow control of larger drain current than a higher threshold device.

The availability of such low-threshold DMOS devices insures the performance needed to be driven by low level logic systems, in which the maximum voltage available is only 3-5 volts.

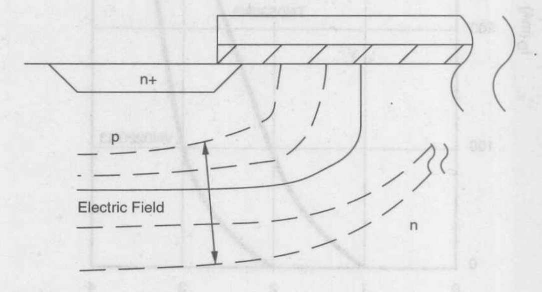


Figure 2: Electric Field Connecting Drain and Source

Part Number	IRF 520			VN12105			
Parameter	**Min**	**Max**	**Conditions**	**Min**	**Max**	**Conditions**	**Unit**
$V_{GS(th)}$ Gate Threshold Voltage	2.0	4.0	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	0.8	2.4	$V_{DS} = V_{GS}$, $I_D = 10mA$	V
$ID_{(ON)}$ On-State Drain Current	8.0		$V_{DS} > I_{D(ON)}$ x $R_{DS(ON)}$ max $V_{GS} = 10V$	20.0		$V_{DS} = 25V$ $V_{GS} = 10V$	A
				5.0		$V_{DS} = 25V$ $V_{GS} = 5V$	A
$R_{DS(ON)}$ State Drain-to-Source On Resistance		0.3	$V_{GS} = 10V$ $I_D = 4.0A$		0.3	$V_{GS} = 10V$ $I_D = 10.0A$	Ω
					0.45	$V_{GS} = 5V$ $I_D = 2.0A$	Ω

Table 1: Comparison between MOSFET and standard threshold Supertex device

Performance Advantages

With the first device shipped in 1982, Supertex was the pioneer in low-threshold DMOS FET technology and still maintains a performance edge over other manufacturers. Supertex currently supplies the lowest threshold MOSFETs in the industry. A threshold voltage of 1.6 volts for N-channel and 2.4 volts maximum for P-channel clearly supports this claim.

Supertex measures threshold voltages at I_D = 1mA, 2.5mA, and 10mA for small, medium and large-sized devices, respectively. Although some manufacturers use test conditions as low as I_D = 250µA for large devices, Supertex devices, in comparison, still have lower values of threshold voltages at higher values of I_D. See Table 1 for a comparison between a popular MOSFET and a standard-threshold Supertex device.

A true comparison can be made by normalizing the value of the I_D test condition. The threshold voltage for VN1210N5 will be lower than 2.4 volts, maximum, when it is tested at I_D = 250µA. Supertex's test conditions therefore portray a realistic picture of the device's capabilities at low V_{GS} conditions.

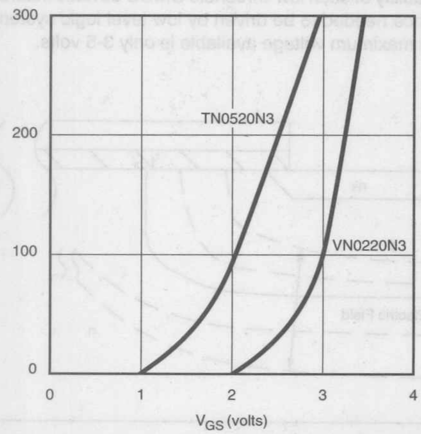


Figure 3: Typical Transfer Characteristics

The threshold voltage is an important indicator of performance at low V_{GS} conditions because a device that starts conducting at a very low bias will exhibit good characteristics under such conditions. In fact, $R_{DS(ON)}$, maximum, and $I_{D(ON)}$, minimum, at low V_{GS} conditions are much more important than just the threshold voltage value because quiescent gate voltage conditions are usually at least a few volts above the $V_{GS(th)}$ value. Figure 3 shows the transfer characteristics of a standard-threshold and a low-threshold device. For example, if the drain current requirement is 100mA, TN0520N3 will typically need V_{GS} = 1.8 volts and VN0220N3 will require 2.8 volts to achieve this value. In case a 2.8 volts drive is not available, as in many applications, a VN0220N3 will be incapable of functioning in the circuit. In spite of the TN05 die being half the size of a VN02, the TN0520N3 performance is far superior at low gate to source voltages.

When confronted by low gate drive voltage, a designer basically has two choices:

Approach 1: Use a large industry-standard-threshold device to obtain the required low $R_{DS(ON)}$, maximum and $I_{D(ON)}$, minimum values. $I_{D(ON)}$ can be obtained from the transfer characteristics and $R_{DS(ON)}$ values will be read off the typical saturation or output characteristics.

Approach 2: Compared to the device used in Approach 1, use a relatively small (die size), low-threshold device to achieve the desired $I_{D(ON)}$ and $R_{DS(ON)}$ at the given minimum gate-to-source voltage.

Comparison of Approach 1 and 2

1. Large die always have larger parasitic capacitance and consequently slower switching speeds. This could pose a restriction in many applications, where limited gate drive charging current is available.
2. Large die must be accommodated in large packages, and this may result in unnecessary waste of board space. For example, the total volume occupied by a TO-220 package including stand off could be 8 to 10 times more than a TO-92 package.

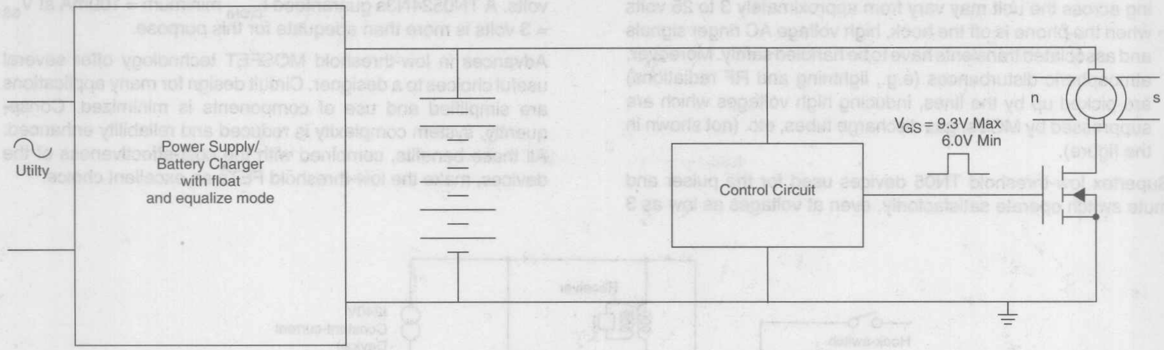


Figure 4: Motor of a Fluid Injection Pump

3. A judicious choice using smaller die in a smaller package can result in considerable cost savings. With more silicon and several times the raw material content for packaging, a low-threshold TO-92 will definitely be a much more cost-effective alternative.

Supertex publishes $R_{DS(ON)}$, maximum, and $I_{D(ON)}$ minimum, specifications at V_{GS} = 5 volts (see Table 1). This data is very useful to a designer because it is always desirable to rely on guaranteed values instead of typical curves. Typical curves are based on a high statistical probability of the majority of devices closely meeting values on the curves. They do not 100% guarantee performance of all devices. Manufacturing tolerances and some variations from one fabrication lot to another are likely to cause lower than expected values of these parameters. Depending entirely on curves tends to be risky for production runs even if prototypes built earlier perform satisfactorily.

The combined effect of low-threshold voltage and low-input capacitance is ease of drive, which is a key consideration in most circuits employing MOSFETs. What better trait can a designer expect than a small amount of charge controlling high voltages and large currents? These low-threshold FETs from Supertex are ideally suited to interface low-voltage logic to the outside world.

Applications

Low-threshold MOSFETs play a key role in circuit design whenever there is a low gate-to-source voltage situation. Conventional devices are often very inefficient and sometimes unusable in some applications as follows:

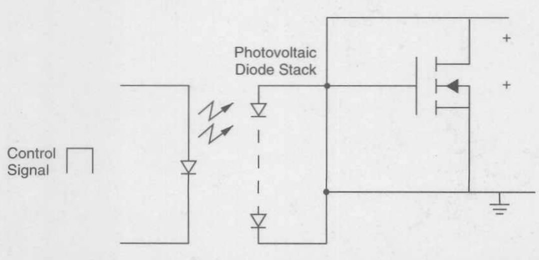


Figure 5: Photovoltaic Drive Scheme

- Handheld, battery-operated equipment requiring satisfactory operation at low/end-of-discharge voltages. This is necessary for complete utilization of battery energy. Inadequate turn-on of a FET can cause two problems: A) loss of control signal or data; or B) loss of power due to resistive losses. Supertex TN/TP series devices are being used for a variety of data acquisition and remote-control applications.
- Medical equipment with battery backup is another popular application. Figure 4 shows the motor of a fluid injection pump powered by the utility supply and backed by a NiCad battery. The V_{GS} = 6 volts condition demands careful attention, because the $R_{DS(ON)}$ has to be low in order to ensure a low drain to source voltage drop. A large voltage drop can A) affect motor performance, and B) cause high I^2R losses, reducing system efficiency and battery back-up time.

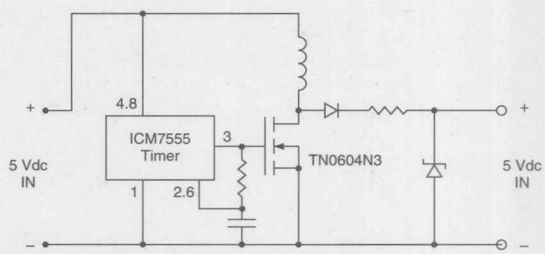


Figure 6: Charge Pump Converting 5VDC to 12VDC

- Solid-state relays utilize optically-isolated drive schemes for isolation purposes. Figure 5 shows a commonly-used photovoltaic drive scheme. Usually a low voltage is available to turn on the FET to meet the relay's assured $R_{DS(ON)}$ specifications. Precautions are taken to avoid excessive drive since the charge applied during turn-on must be quickly discharged during turn-off. Turn-off circuitry is not shown in this simplified schematic.
- Figure 6 shows a simple charge pump converting $5V_{dc}$ to $12V_{dc}$. The key parameter for efficient functioning of this circuit is $R_{DS(ON)}$ at V_{GS} = 5 volts.
- Telephone handsets encounter wide variations of voltage during normal operation (Figure 7). While the DC voltage appear-

ing across the unit may vary from approximately 3 to 25 volts when the phone is off the hook, high voltage AC ringer signals and associated transients have to be handled safely. Moreover, atmospheric disturbances (e.g., lightning and RF radiations) are picked up by the lines, inducing high voltages which are suppressed by MOVs, gas discharge tubes, etc. (not shown in the figure).

Supertex low-threshold TN05 devices used for the pulser and mute switch operate satisfactorily, even at voltages as low as 3 volts. A TN0524N3s guaranteed $I_{D(ON)}$ minimum = 100mA at V_{GS} = 3 volts is more than adequate for this purpose.

Advances in low-threshold MOSFET technology offer several useful choices to a designer. Circuit design for many applications are simplified and use of components is minimized. Consequently, system complexity is reduced and reliability enhanced. All these benefits, combined with the cost-effectiveness of the devices, make the low-threshold FETs an excellent choice.

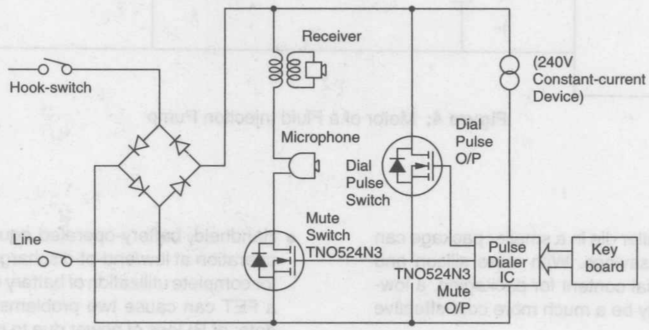


Figure 7: MOSFETs in a Telephone Handset

Supertex inc.

HVCMOS Application Note AN–H3

3

Basics of EL Panel Drive Techniques

Thin film electroluminescent (EL) panels operate on a principle of successive pulses of opposite polarity. These pulses must exceed a threshold of approximately 200V for the panel to emit light.

A flat panel display is a sandwich of phosphor material with dielectric coating on either side; transparent ITO (Indium Tin Oxide) row electrodes on one side and column electrodes on the opposite side. These layers are built up on a sheet of glass to form a very thin, lightweight display panel.

Since the drive electrodes are dielectrically isolated from the phosphor material, and each other, the display panel exhibits a capacitive load to the drive electronics. On larger panels this capacitance can be quite high. Surge currents can be large; therefore, coupling from the row to the column electrodes should be considered.

The drive electronics used to operate the panel are organized in a manner to surround the display panel with contacts as shown in Figure 1.

Generally, the row electrode electronics supply the major portion of the threshold voltage, called the scan pulse, and the opposite polarity "refresh" pulse , which is necessary for the panel to emit light. The refresh pulse is usually applied to all rows at one time while the scan pulse is applied to one row at a time (starting with row #1), similar to a television raster scan.

Depending on the data to be displayed in each column, the column electrode electronics supply a voltage of opposite polarity to the row scan pulse. This combination of row and column voltage across the phosphor will exceed the threshold and cause the phosphor in areas between the energized row electrodes and the energized column electrodes to glow. This sequence, applied to successive rows, causes certain portions of the display to be illuminated.

Because the phosphor requires successive pulses of opposite polarity to operate, an opposite polarity refresh pulse is applied to all row electrodes simultaneously while the column drivers are kept at ground. The sequence then begins again at row #1 with the next frame of data. Figure 2 is a representative timing diagram of the signals applied to a TFEL panel showing the first four rows and the first column.

Due to the fact that the phosphor illumination threshold has a slope of illumination versus applied voltage within a short range, the column drive electronics can be made to vary the applied voltage within this range, dictated by the intensity of light desired for a particular element on the display. By this means, a gray shade image can be created using the EL display.

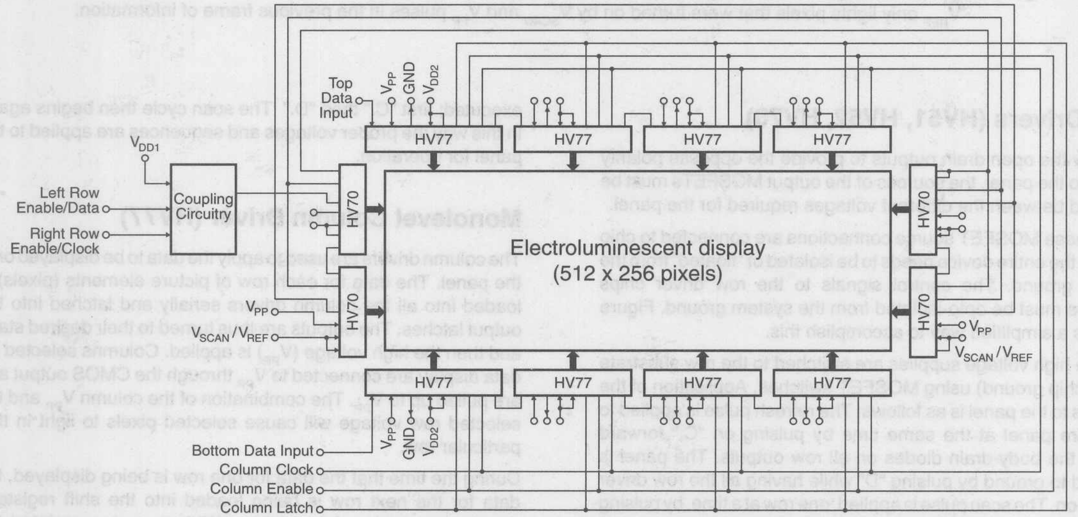


Figure 1: Block diagram of the driver system for a TFEL (Thin Film Electroluminescent) panel. Note that the column drivers have two data lines with interleaved pixel data.

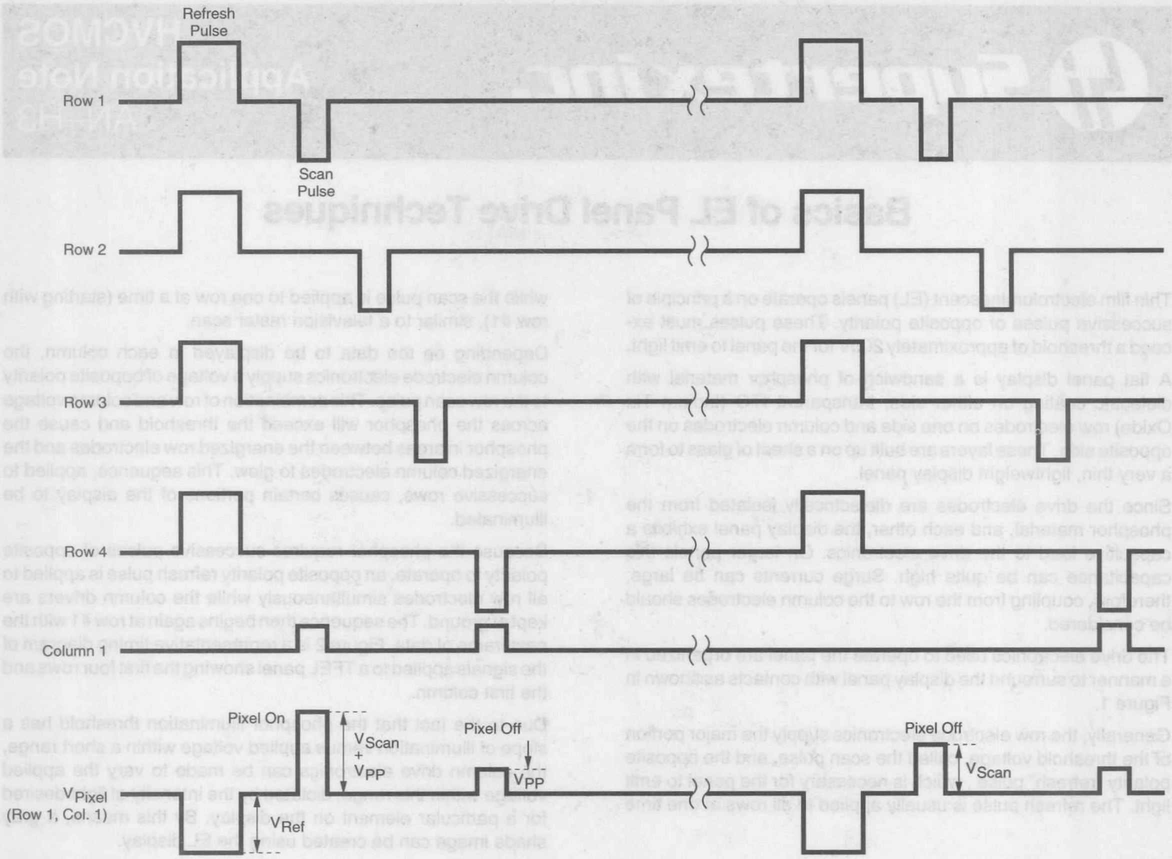


Figure 2: Simplified diagram illustrating row and column timing to operate an EL Panel. V_{REF} only lights pixels that were turned on by V_{SCAN} and V_{PP} pulses in the previous frame of information.

Row Drivers (HV51, HV52, HV70)

To allow the open drain outputs to provide the opposite polarity pulses to the panel, the sources of the output MOSFETs must be switched between the different voltages required for the panel.

Since these MOSFET source connections are connected to chip ground, the entire device needs to be isolated or "floated" from the system ground. The control signals to the row driver chips therefore must be opto-isolated from the system ground. Figure 3 shows a simplified way to accomplish this.

The two high voltage supplies are switched to the row substrate (driver chip ground) using MOSFET switches. Application of the voltages to the panel is as follows: The refresh pulse is applied to the entire panel at the same time by pulsing on "C," forward biasing the body-drain diodes on all row outputs. The panel is returned to ground by pulsing "D" while having all the row driver outputs on. The scan pulse is applied, one row at a time, by pulsing on "A" while the selected row output is on. The selected row is returned to ground by turning on "B." The next row to be scanned is then selected, and the scan is repeated; first "A," then "B." When the entire panel has been scanned, the refresh sequence is executed; first "C," then "D." The scan cycle then begins again. In this way the proper voltages and sequences are applied to the panel for operation.

Monolevel Column Driver (HV77)

The column drivers are used to apply the data to be displayed onto the panel. The data for each row of picture elements (pixels) is loaded into all the column drivers serially and latched into the output latches. The outputs are thus turned to their desired state, and then the high voltage (V_{PP}) is applied. Columns selected for data display are connected to V_{PP} through the CMOS output and are pulled up to V_{PP}. The combination of the column V_{PP} and the selected row voltage will cause selected pixels to light in that particular row.

During the time that the data for one row is being displayed, the data for the next row is being loaded into the shift registers, awaiting the display of the next row. When a row is completed, the column driver V_{PP} is brought low and the data waiting in the shift register is loaded into the output latches. The cycle then begins again for each successive row.

The column drivers are designed with a serial shift register output for use in cascading the column drivers together. This allows the data for one row to be loaded serially, using one serial input at the first column driver device.

Gray Scale Column Driver (HV38)

This device is designed to take four data inputs in parallel into four shift registers. The data is then taken from equivalent stages of each shift register and converted to an analog level, 1 of 16 between ground and V_{PP}. This is done by a digital counter using four bits of input data. The counter is preset with data counting down to turn off a transistor. This transistor isolates a ramp input (VR) from an internal storage capacitor, which controls a CMOS output stage. The output voltage therefore represents the value of the ramp voltage (VR) at the time the counter for each output counted down. This voltage, applied to the column of the panel, combines with the row scan voltage to vary the light output from each pixel in the selected row.

Panel Brightness

The varying brightness of an EL panel by voltage variation can only achieve a limited range. Dramatically increased panel output such as required by panels to be operated in direct sunlight, requires another method of increasing output. This is done by increasing the panel frame rate, or refresh rate. Normal CRT based systems work on a 60Hz frame rate. Most applications of EL panels replacing CRTs, then, also operate at this rate. This is fine for office and home use but does not provide enough brightness to accommodate most military applications. By increasing the refresh rate up to tenfold, a dramatic increase in brightness can be achieved.

This increase in refresh rate requires some changes in the column driver configuration. Instead of cascading all the column drivers together, each column driver shift register input is driven in parallel by the controlling system at the same time. This increases the number of data lines required but allows the data to be loaded much faster, enabling the faster frame rates desired. The row drivers are used at a much slower rate, so no changes are required to achieve faster operation.

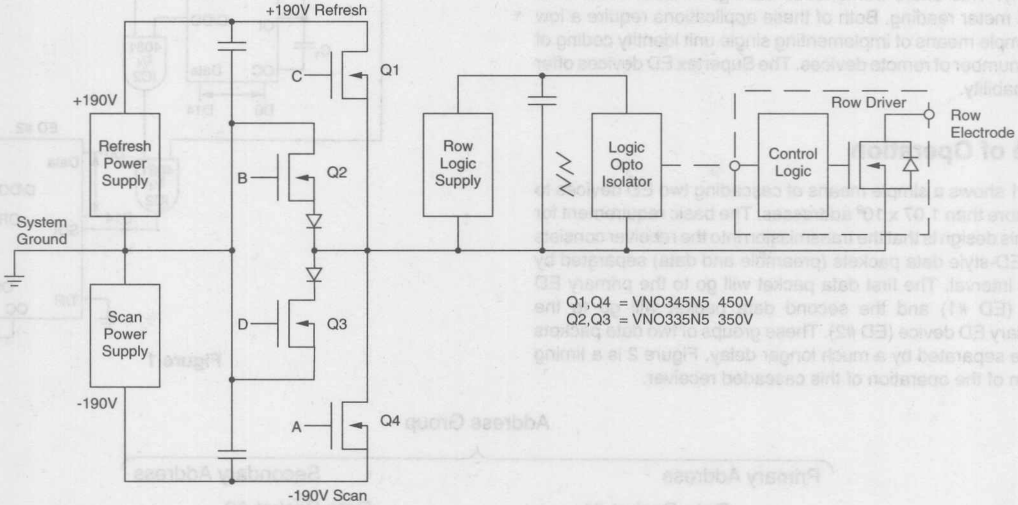


Figure 3: Row driver panel switching block diagram.

Cascading Encoder-Decoder

The Supertex family of encoder-decoder devices allows address matching of up to 32,768 different codes. Four bits of data can be sent to up to 2048 different receive devices. This has been adequate for the vast majority of applications. Some applications, however, require even more addressing capability than the largest part can offer.

A cable TV control system, with which a cable company would want to control operation of all the decoders in their area, is one application in which the possible remote addresses could number more than 32,768. Another possible use is remote meter reading of domestic and industrial power meters by the local utility company. This offers tremendous savings in labor costs over manual meter reading. Both of these applications require a low cost, simple means of implementing single unit identity coding of a large number of remote devices. The Supertex ED devices offer this capability.

Mode of Operation

Figure 1 shows a simple means of cascading two ED devices to allow more than 1.07 x 10^9 addresses. The basic requirement for using this design is that the transmission into the receiver consists of two ED-style data packets (preamble and data) separated by a short interval. The first data packet will go to the primary ED device (ED #1) and the second data packet will go to the secondary ED device (ED #2). These groups of two data packets must be separated by a much longer delay. Figure 2 is a timing diagram of the operation of this cascaded receiver.

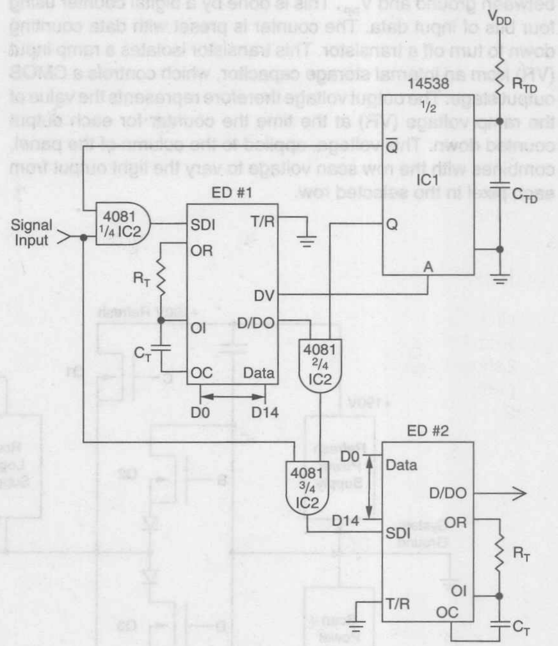


Figure 1

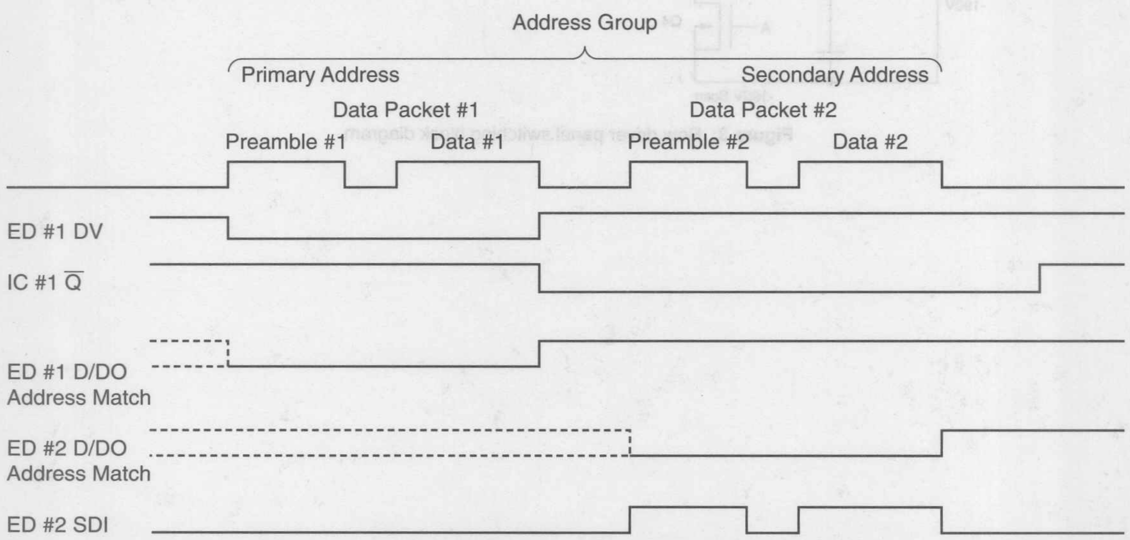


Figure 2

On initial condition, in which the receiver is waiting for an address group to arrive, one-shot IC #1 enables the incoming signal into the Start/Data Input (SDI) of ED #1 while disabling the path to ED #2. When the group arrives, the first data packet is input into ED #1. When this data packet, both preamble and data, have been received by ED #1, the Data Valid (DV) signal will go high, triggering the one-shot. This will disable the SDI input to ED #1. If the data in data packet 1 matched the address data on the ED #1 data pins, then ED #1 Decode/Data Output (DDO) pin will also go high. This and the triggered one-shot enables the path from the signal input to the SDI pin of ED #2. The second data packet will then be received by ED #2 and compared to the data input pins. If the address matches, the ED #2 DDO will go high.

The one-shot timing must be set to allow data packet 2 to be completely received before the one-shot times out and returns to the off condition. This time period will vary depending on the transmission speed of the communication link and the ED speed used. After both data packets have been received and the one-shot has timed out on all the receivers in the system, the transmitter can then send out a new address group.

Address Decode

The circuit shown in Figure 1 and described in the previous section implements the address decode function. The DDO pin on ED #2 should be connected to a device that operates on a positive going edge to signal the correct addressing of both ED #1 and ED #2.

Different combinations of ED devices can give a different number of possible addresses. The following table illustrates these possibilities:

ED #1	ED #2	# of possible addresses
ED-15	ED-15	1,073,741,824
ED-15	ED-9	16,777,220
ED-15	ED-5	1,048,576

The ED-9 cannot be used in the ED #1 position because it does not have a DV output available.

Address and Data

Often it is necessary not only to address a particular device within a large number of devices in a system, but also to send some amount of data only to that device. The ED-11 and DC-7 devices easily implement this capability in the cascaded design. Figure 3 illustrates a data transmission variation of the cascade circuit.

The input controls for ED #1 and #2 operate the same as for the address matching case. In this case, however, the Serial Data Output (SDO) and Data Clock (DC) of ED #2 are connected to a 4094 serial to parallel shift register. The SDO is connected to the Data In pin, while the DC is connected to the Clock pin to clock the data into the shift register. The rising edge of the ED #2 DDO signal is converted to a pulse and used to transfer the data from the shift register to the parallel output latches of the 4094 if the

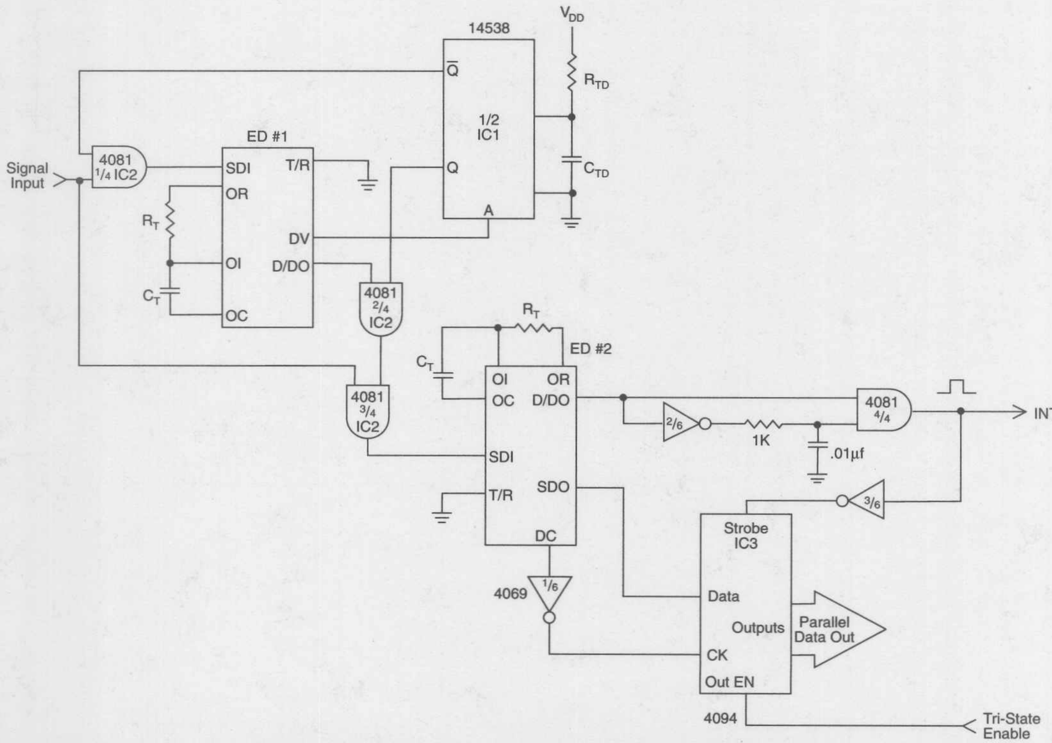


Figure 3

address match is detected. The DDO pulse is also available from the receiver system as an interrupt to the external circuitry signalling the arrival of data from the transmitter.

ED #1	ED #2	Data Bits	Address Combinations
ED-15	ED-11	4	67,108,864
ED-15	DC-7	8	4,194,304
ED-15	ED-5	15	32,768 *special case
ED-5	ED-11	4	65,536
ED-5	DC-7	8	4,098
ED-5	ED-5	15	32 *special case

* The special cases noted above represent a situation in which 15 data bits must be received. This is implemented by using ED #1 only for address matching and using ED #2 only for data reception. To receive 15 bits, two 4094s must be serially connected to form a 16 bit shift register. The Data Valid (DV) output of ED #2 would be connected in place of the DDO output to strobe the data into the latches of the 4094s.

Transmitter

The transmitter used to address this receiver design would normally be microprocessor controlled, with a peripheral adapter port connected to the data pins of an ED-15 device. The data pins could be changed to implement the data packet #1 and #2 by the much faster microprocessor. Alternatively, two ED-15s could be OR-gated to a transmission media and controlled by normal logic.

Conclusion

This application should help implement a simple low cost means to address a large number of remote devices in an addressing system. If there are any questions or suggestions for improvement, please contact the applications engineering department at Supertex.

DC-7, ED-5, ED-9, ED-11 Applications

The Supertex "ED Family" of remote control encoder/decoder chips has almost unlimited uses. To make the user aware of some of the salient features of these unique ICs, we have put together this application note. When used in conjunction with the data sheet for these parts, most of the questions that may arise from attempts to design systems around them may be answered.

Remote Control Systems

As electronic systems become increasingly more sophisticated, the need to perform certain functions at a distance becomes increasingly important. In many cases, the need arises for central automatic control of remote operations. Here, too, remote control devices are necessary. Until recently, remote control of various functions required a plethora of discrete circuits, raising the cost, in many cases, to prohibitive levels. Recently the MOS LSI industry has responded with integrated circuits of varying usefulness and complexity. Most of these ICs are geared to perform a single task such as opening garage doors, controlling TV functions, and the like. Until now, all remote control ICs were sold in a set; i.e., a separate encoder and decoder. The Supertex EDs on the other hand are a single chip. The encode/decode function is determined by a programming pin, which is tied to V_{DD} for the encode function and V_{SS} for the decode function. Having only one chip reduces the complexity of purchasing remote control. Spares are easier to stock, and reliability is enhanced.

The Supertex EDs

In addition to the "lock-and-key" feature of ED codability, the ED-11 has the feature of being able to transmit and receive 4 additional bits of binary data which are available at the decoder's output. The DC-7 has 8 bits of data. These can be used to perform tasks such as channel recognition (with digital readouts), microprocessor interface and event sequencing. This feature makes the ED family of encoders/decoders extremely versatile.

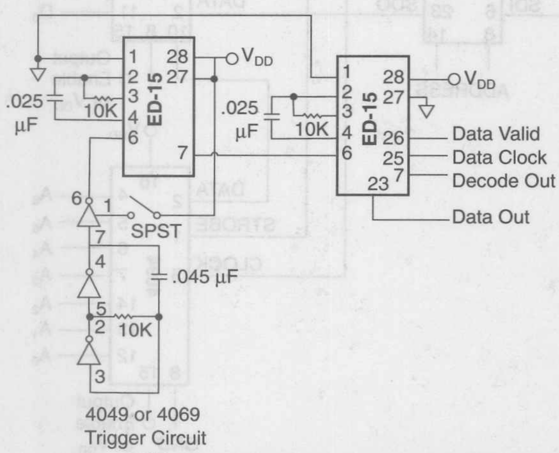


Figure 1: Basic two-wire ED system

Simple, Two-Wire Interface Utilizing ED-15s

The basic application for the ED-15 is the simple two wire interface. This configuration is useful for optimizing ED parameters such as encoder/decoder frequency stability, and lockup time. It is also a useful way of observing waveforms and can be invaluable for troubleshooting a more complicated system using other transmission media.

In Figure 1, the output is not latched and will stay high only so long as the trigger circuit keeps cycling the encoder. The CMOS oscillator is necessary to produce the start pulse. By utilizing an oscillator, it is possible to get a continuous data stream. This is useful for observing all waveforms involved. The start pulse oscillator can even be used to trigger the scope, making the waveforms easy to sync. The wire used can be just a jumper when both encoder and decoder are on the same breadboard, but twisted pair or shielded cable should be used for long runs.

ED-11, DC-7 System Utilizing Hardwire Transmission and Output Latches for Additional Data

As stated earlier, one of the great features of the ED family of encoder/decoders is the ability of the ED-11 and ED-5 to transmit 4 bits of binary code along with the "lock-and-key" recognition bits, the DC-7 to transmit 8 bits of binary code along with the "lock-and-key" recognition bits, and these 4 or 8 bits to appear at the data clock output of the receiver. This feature allows the transmission of useful data instead of just the "code valid" output common to other so-called remote control encoder/decoders. The following is an adaptation of the hard-wired system seen above. The difference is that even though an ED-15 is used for the encoder, an ED-11 is used for the receiver, and this data is decoded for use as a parallel latched data bus. Of course, since the last 4 bits in the ED-11 are used as actual transmitted non-dedicated data, it has only 2048 different possible code combinations instead of the 32,768 combinations possible with the ED-15 system. The trigger circuit is the same as above and will be represented from here on only as a block diagram.

In Figure 2, an ED-11 can be used for the transmitter as well as for the receiver. An ED-15 is shown to illustrate the compatibility of the ED family of encoder/decoders. The 4015 in the circuit is a serial to parallel converter and the 4042 is a quad 4-bit latch. The data valid pin is used to clock the parallel data into the latch and Q as well as $\overline{Q}$ outputs are available on this IC. The bit sequence chart is given below the schematic to show the relationship of the "key-code" bits to the last 4 data bits.

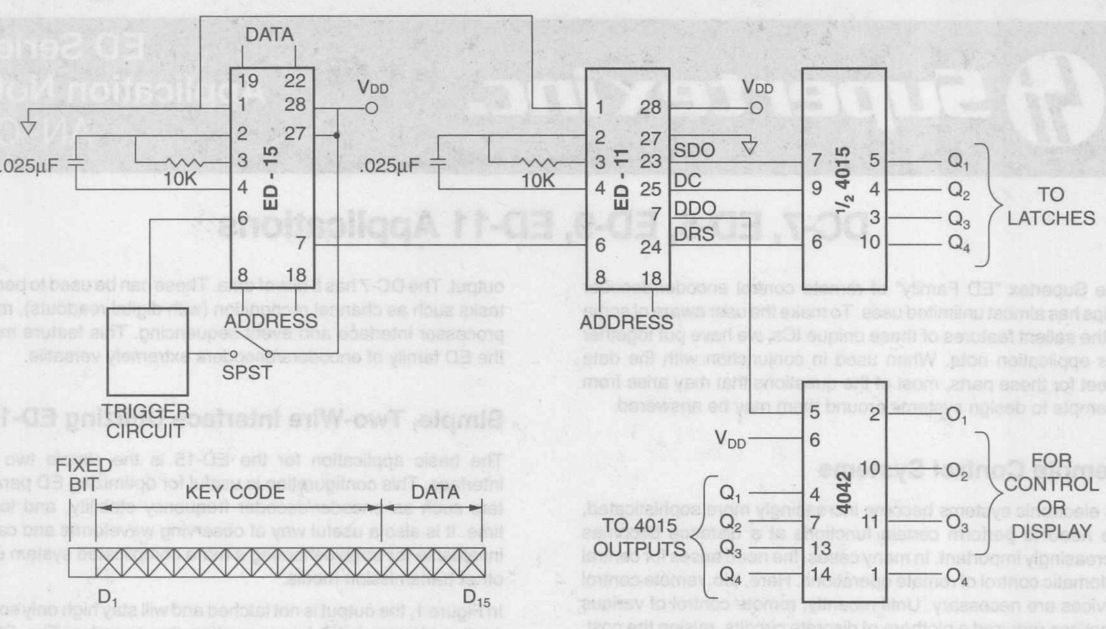


Figure 2: ED system with latched parallel data out

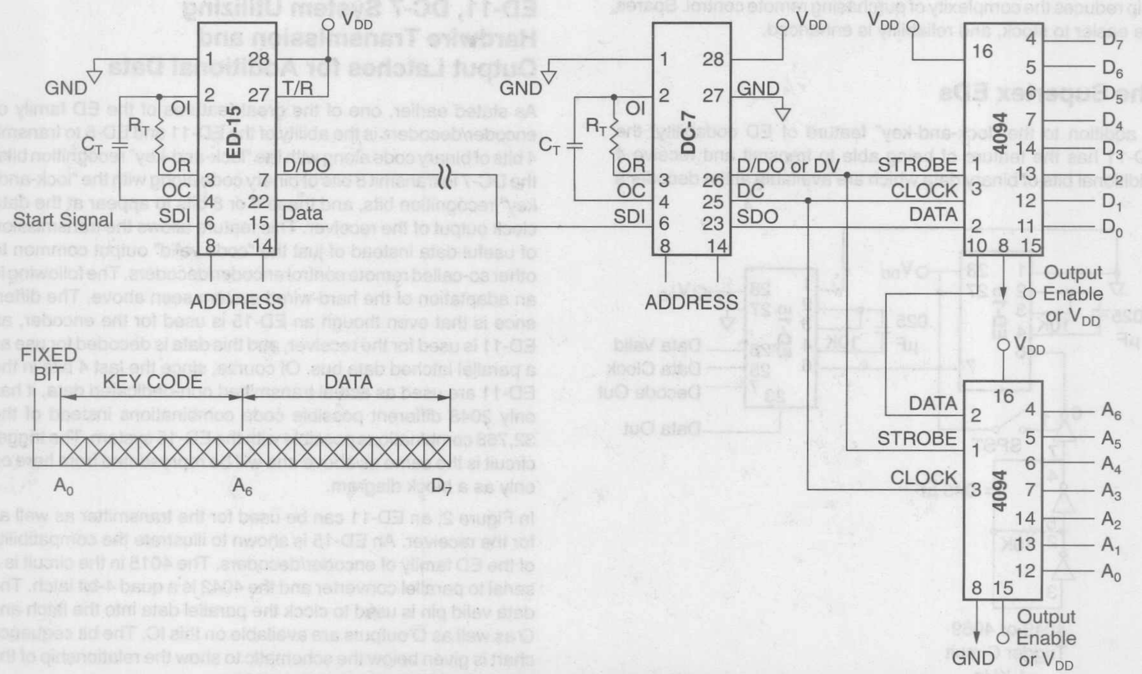


Figure 3: DC-7 system with latched parallel data out

In Figure 3, a DC-7 can be used for the transmitters as well as for the receiver. An ED-15 is shown to illustrate the compatibility of the ED family of encoder/decoders. The 4094 in the circuit is a serial to parallel converter and an 8-bit latch. This circuit demonstrates the use of the DC-7 in which both the data and address can be transmitted from one location to another and both the data and address of the transmitter recovered. In an application in which only the data is to be recovered and a special address assigned to the receiver, the D/DO signal should be connected to the 4094 and only the TOP 4094 used. In a system in which all incoming data and addresses are to be decoded the DV signal would be connected to both 4094s as shown. The bit sequence chart is given below the schematic to show the relationship of the "key-code" bits to the last 8 data bits.

Infrared Transmission

Often it is necessary to transmit data over some distance without wires. In such an instance it is necessary to couple the data (in this case from ED-series encoder/decoders) by way of some transmission media. Here is a simple but effective way to use IR as a medium for signalling between two EDs.

The circuit in Figure 4 is designed so that the ED-15 is operating at 25KHz. The output of the chip (Pin 7) is applied to an NPN transistor gated with a 3.3KΩ base resistor to act as a switch. The data stream turns the 2N4401 hard on or off depending upon the coded state. This in turn switches on and off the Monsanto MV5000 series infrared LEDs. Three of the LEDs are used to make aiming at the receiver easier.

The receiver circuit consists of a three-stage amplifier (the CA 3035) with Siemens BP104IR photo diodes arrayed for maximum coverage of the reception area. The output of the CA3035 is then applied to the ED-15 receiver chip and the signal is decoded in the normal way. The range of this set-up should be about 10 meters.

Even though in this application the ED-15 is shown, it will work equally well with any of the other ED ICs. This application can be combined with the application in Figure 2 to provide 4 bits of parallel data or Figure 3 to provide 8 bits of parallel data to operate displays, relays, etc.

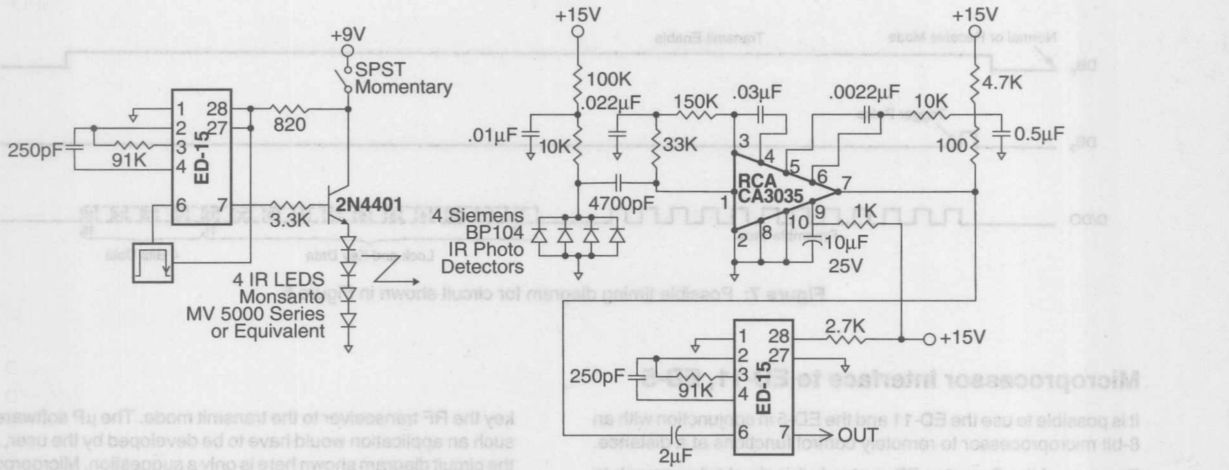


Figure 4: IR remote control transmitter/receiver

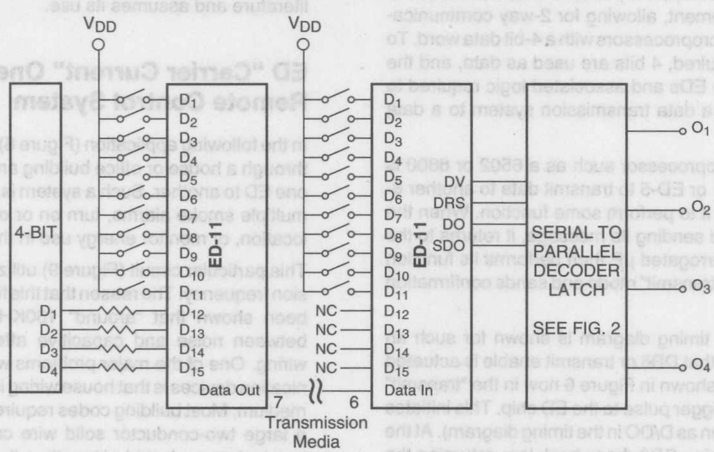


Figure 5: Block Diagram showing basic configuration for transmitting microprocessor data over remote control system using ED-11s as encode/decode

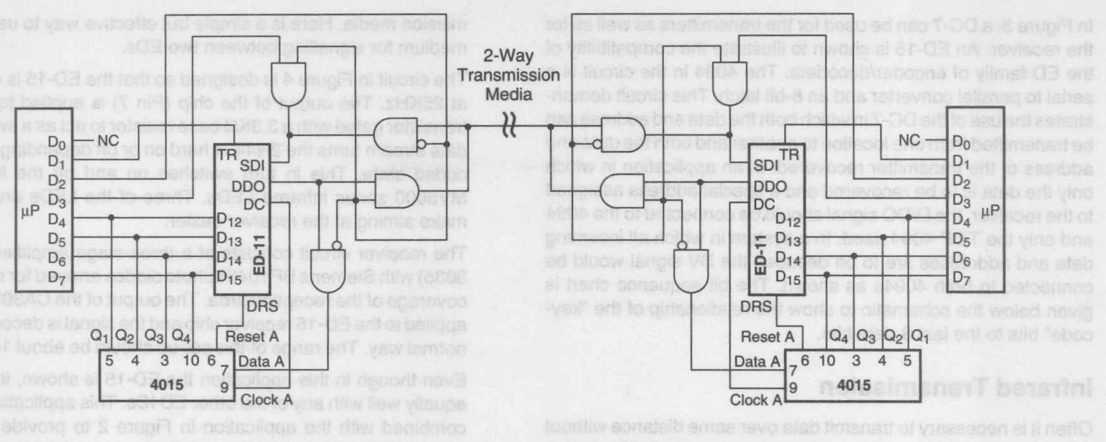


Figure 6: ED system illustrating "handshaking" capabilities of Supertex ED-11s

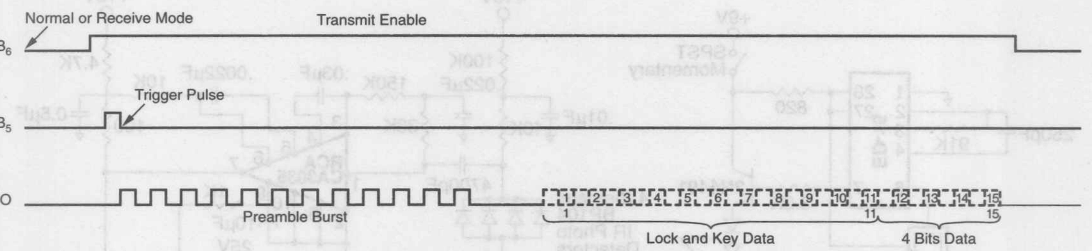


Figure 7: Possible timing diagram for circuit shown in Figure 5

Microprocessor Interface to ED-11, ED-5

It is possible to use the ED-11 and the ED-5 in conjunction with an 8-bit microprocessor to remotely control functions at a distance.

Because of the Supertex ED system's "single chip" approach to encode-decode remote control, it is possible to use these ICs in a "hand-shaking" arrangement, allowing for 2-way communication between 2 or more microprocessors with a 4-bit data word. To do this, an 8-bit μp is required, 4 bits are used as data, and the remaining bits control the EDs and associated logic required to change the system from a data transmission system to a data receiving system.

In Figure 6, an 8-bit microprocessor such as a 6502 or 6800 is used to enable the ED-11 or ED-5 to transmit data to another 8-bit microprocessor telling it to perform some function. When the transmitting μP is finished sending its message, it returns to the "receiver" mode. The interrogated μP then performs its function and switches itself to the "transmit" mode and sends confirmation back to the first μP.

In Figure 7, a "possible" timing diagram is shown for such an application. One can see that DB6 or transmit enable is actuated first. With all of the gates shown in Figure 6 now in the "transmit" mode, DB5 sends out a trigger pulse to the ED chip. This initiates a data transmission (shown as D/DO in the timing diagram). At the end of this data transmission DB6 drops back low, returning the ED and data systems to the "receive" mode. For RF transmission the DB6 signal can also be used (via a buffer) to drive a relay to key the RF transceiver to the transmit mode. The μP software for such an application would have to be developed by the user, and the circuit diagram shown here is only a suggestion. Microprocessor information used in this circuit is from the 6502 or 6800 literature and assumes its use.

ED "Carrier Current" One-Way Remote Control System

In the following application (Figure 8), the AC power lines running through a house or office building are used to transmit data from one ED to another. Such a system is an ideal way to interconnect multiple smoke alarms, turn on or off appliances from a central location, or monitor energy use in the home or plant.

This particular circuit (Figure 9) utilizes 160KHz as the transmission frequency. The reason that this frequency is used is that it has been shown that "around" 160KHz is the best compromise between noise and capacitive attenuation of typical building wiring. One of the major problems with "carrier current" communication devices is that house wiring is a very difficult transmission medium. Most building codes require that buildings be wired with a large two-conductor solid wire called "ROMEX." Since both conductors are jacketed together, the capacitance between them is quite high and the attenuation of high frequencies is considerable. To compound this problem many building codes require that

the wiring be conduited. This will be found mostly in commercial and multiple-dwelling buildings, but since the conduit is ground, the capacitance is even greater. Another problem with building wiring as a communication medium is the fact that many appliances hooked to the wiring are large inductive loads (motors, power transformers, etc.). When these inductors are in parallel with the ROMEX, very effective high frequency filters are formed.

External Oscillator for ED-15, ED-11, ED-5, DC-7

Often it is desired to drive the ED-series devices with an external clock. Due to external considerations it is not recommended in the general case.

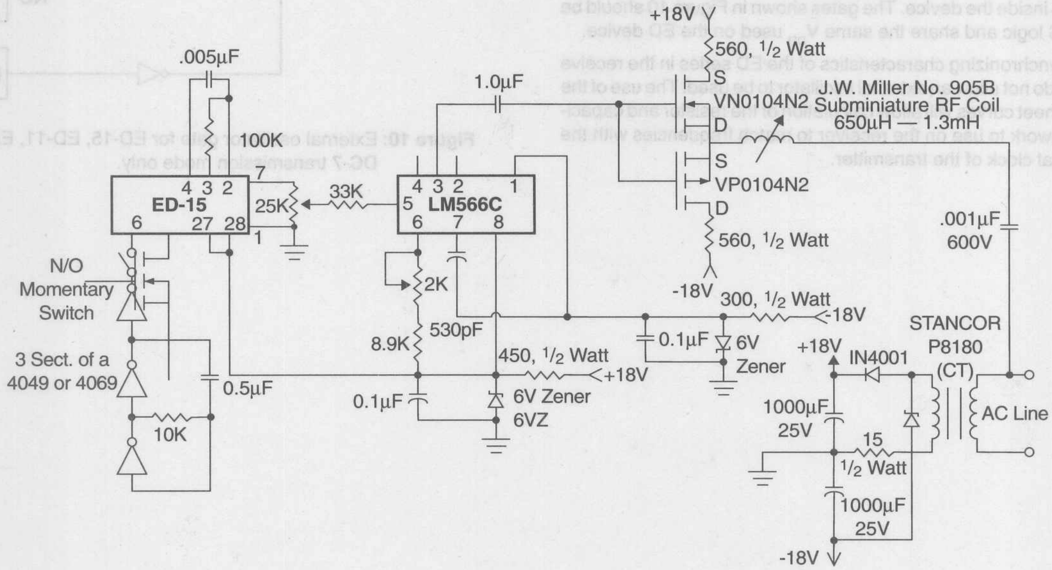


Figure 8: Carrier Current Transmitter

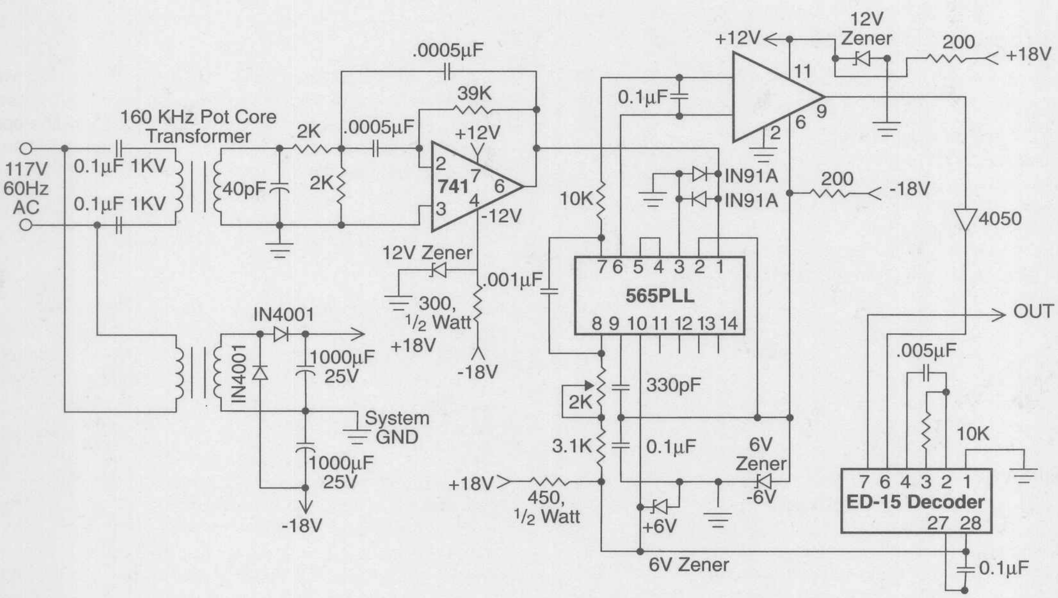


Figure 9: Carrier Current Receiver. 160KHz transformer consists of an 18x11mm ungapped pot core (Siemens, ferrocube, etc.) utilizing magnetics incorporated type "F" material wound with 80-1/2 turns of No. 35 wire for the secondary and 4-1/2 turns for the primary. This gives a turns ratio of approximately 15 to 1.

However, the ED-15, ED-11, ED-5 and DC-7 device types may be externally driven in the transmission mode if certain precautions are taken. Using the circuit in Figure 10 will allow driving of the transmitter chip. The external oscillator MUST be gated on only during the transmission time after the START pulse. During all other times the O/I pin MUST be held high. The DRS signal in the transmit mode is a convenient signal to use as a gate for this purpose. A 1KΩ resistor in series will minimize possible current spikes inside the device. The gates shown in Figure 10 should be CMOS logic and share the same V_{DD} used on the ED device.

The synchronizing characteristics of the ED series in the receive mode do not allow an external oscillator to be used. The use of the data sheet curves will allow calculation of the resistor and capacitor network to use on the receiver to match frequencies with the external clock of the transmitter.

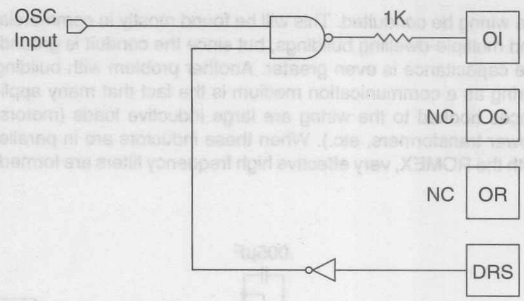


Figure 10: External oscillator gate for ED-15, ED-11, ED-5, DC-7 transmission mode only.

Encoder-Decoders for Power Line Carrier Remote Control

Power Line Carrier Communication is starting to emerge as a viable, cost effective means for control and information exchange in both consumer and industrial applications.

Energy Management Systems for heating, air conditioning and lighting control are obvious examples of the use of the power line as a communication link. A system is shown in Figure 1 using Supertex Encoders and Decoders for transmitting and receiving control information over the power line. The prototype system was designed to allow remote On/Off and brightness control for a fluorescent lighting fixture using a dimming ballast. The design was simple and implemented in about a week's time.

System Description

The system uses an ED Encoder-Decoder chip set to generate the Power Line control messages and to decode the messages for appropriate action. The system transmitter is able to selectively address 32 different receivers and transmit 16 different control commands to the receivers that are connected to the AC power line.

The control message is coupled to the AC power line by a Signetics NE5050 Power Line Modem. The modem takes a serial bit stream, generated by the ED-9, and turns it into a series of 125KHz bursts. Each burst represents a digital "1" in the serial bit stream. This series of 125KHz bursts is transmitted over the AC power line to any receiver that is coupled to the AC line.

The series of 125KHz bursts are received by a second Power Line Modem and translated back into the original serial bit stream generated by the ED-9. This serial bit stream message contains address and control information. The message is decoded by an ED-5 to determine address match and control command. If the address does not match, then the rest of the message is ignored.

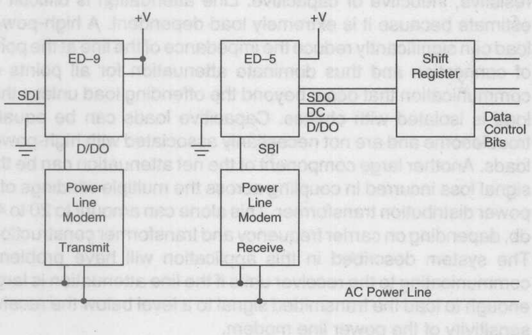


Figure 1. System Diagram

When there is an address match at the receiver, the ED-5 will serially transmit the data information into the serial to parallel shift register. The data can then be decoded to determine which of the 16 control commands was transmitted.

Transmitter (Figure 2)

The ED-9 performs address matching only. In this application, the 9 bits that are available for addressing are split into 5 bits of address (D4, D5, D6, D7, D9) and 4 bits of control data (D12-D15). The 5 bits of address are set with dip switches, and the 4 data bits can be set with dip switches or a rotary selector switch.

The transmission of a message is initiated by a pulse on the Start/Data input (SDI). The message baud rate, f_c, is determined by the RC combination of 10K ohms and .039µf at the OI, OR, and OC pins of the ED-9.

$f_c = 0.375/RC = 961KHz$
$T_c = 1/f_c = 1.04ms$
Data Bit Width $= 2T_c = 2.08ms$
Data Clock Width $= 0.5T_c = .52ms$

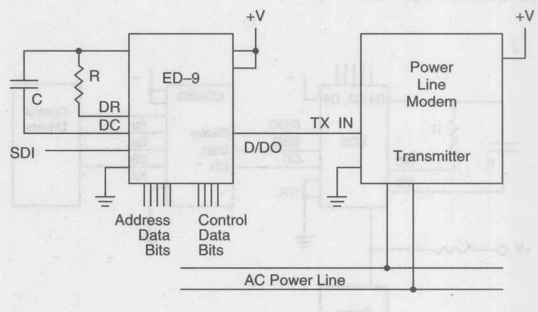


Figure 2. Transmit Circuit

Message Format (Figure 3)

The message (shown in Figure 3) consists of a preamble burst and a data transmission. The preamble burst is used to synchronize the receiver with the transmitter.

The data transmission consists of 15 bits of information. In this application only 5 bits are used for address information and 4 bits for control information. The data transmission is Manchester encoded. Manchester coding uses the transition from low to high to represent a binary "1" and a transition from high to low to represent a binary "0." With this technique, the first half of each data bit time is always the logical inverse of the second half. This

provides for a level transition during each data-bit time, and allows a synchronized receiver to easily read the correct data, even when large noise spikes are present.

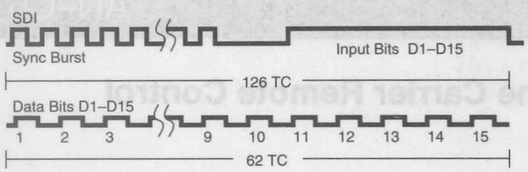


Figure 3. Message Format

Receiver (Figure 4)

The receiver uses an ED-5 in the receive mode by first checking the address of the incoming message against the preset 5-bit address in the receiver unit. If the address in the message matches the receiver address, then the 4-bit control data is serially shifted into the serial-to-parallel shift register. This 4-bit word is now available for further decoding and control.

The message enters the device on the Start/Data Input (SDI) pin. The ED-5 then matches the message address information with the address of the receiver, and if the bits match, the Decode/Data Out (D/DO) pin goes high until the next stream of serial data arrives at the SDI pin. D/DO going high pulses the strobe input to the CD4094. This action resets the shift register, and the DC output from the ED-5 clocks the entire message into the shift register. The last four bits of the message (D12-D15) contain the control information (refer to Figure 5). The control information will be at the outputs of the shift register (Q1-Q4) at the completion of the receive sequence.

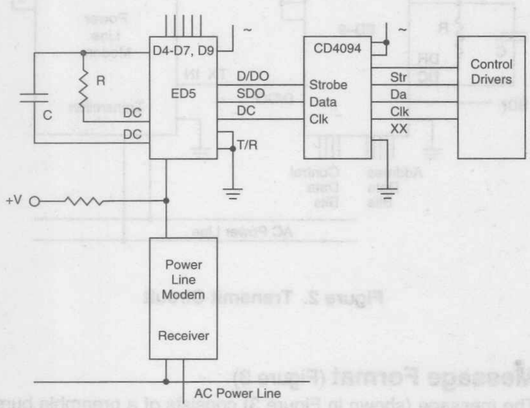


Figure 4. Receive Circuit

Power Line Interface

The Power Line Modem was calibrated to transmit a 125KHz burst at a signal level of 7.5 volts p-p into a 50 ohm load. Impedances of residential wiring may be over 50 ohms while industrial impedances may be less than 1 ohm, with the receiver sensitivity set at 15 millivolts.

The AC Power Line

The constraints imposed by the power line interface dictate the overall system operation. The power lines are a hostile environment for signals. The noise on the power line can be put into two categories: broad band and impulse. The broad band noise levels vary from a few to hundreds of millivolts. Impulse noise levels can range from millivolts to tens of volts. Examples of noise sources are light dimmers, universal motors, hair dryers, induction motors, radio and television receivers, and fluorescent lights. In general, noise levels in a factory environment will be much greater than in a residential environment.

The system described in this application note can, depending on the noise level, be affected by impulse noise on the power line. The communication link between the transmitter and receiver is an open loop one way command link. An impulse could cause false command decode if the impulse happened at the time when the receiver was decoding the control data section of the data transmission. The receiver would have to have properly received and decoded the address for the command to be improperly executed.

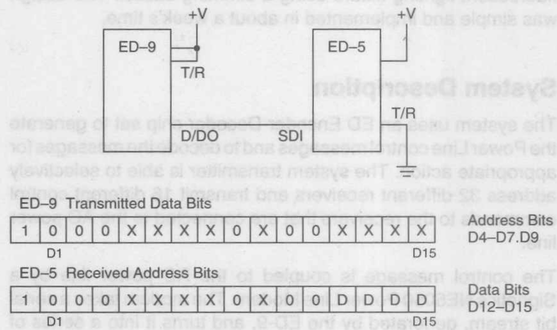


Figure 5. Data Patterns

Impulse noise could also cause errors in the address section of the data transmission, in which case the control command would be ignored due to improper address match. The effect of impulse noise on the operating system is not as much a problem with the encoder/decoder section but with the power line modem, which is improperly decoding the 125KHz bursts.

The impedance of the line is likewise ill-defined. It may be resistive, inductive or capacitive. Line attenuation is difficult to estimate because it is extremely load dependent. A high-power load can significantly reduce the impedance of the line at the point of connection and thus dominate attenuation for all points of communication that occur beyond the offending load unless that load is isolated with chokes. Capacitive loads can be equally troublesome and are not necessarily associated with high-power loads. Another large component of the net attenuation can be the signal loss incurred in coupling across the multiple windings of a power distribution transformer. This alone can amount to 20 to 40 db, depending on carrier frequency and transformer construction. The system described in this application will have problems communicating to the receiver units if the line attenuation is large enough to load the transmitted signal to a level below the receive sensitivity of the power line modem.

Designing for the Power Line Environment

The application described in this paper is a relatively simple use of existing technology to achieve a low cost means of control communication over the AC power line. The system is very flexible with regards to the ability to add microprocessor intelligence to the transmit and receive ends of the communication link. This added intelligence may be used to overcome some of the problems associated with power line noise.

The microprocessor could be used to allow both receive and transmit at the same location. The microprocessor would enable the use of a closed-loop communication link with the unit that is to be controlled. This ability could be used to obtain status reports from the control unit, to make sure the unit properly responded to control information. In the case of a unit not properly responding to control messages, the controller would simply resend the control message until the unit properly responds. The microprocessor software could also include algorithms that detect power line noise or other power line communication. When noise or communication is detected, the microprocessor would simply wait until the power line was quiet enough for it to transmit its control message.

There are numerous methods for overcoming the problems associated with power line impedance. If the problem is due to the transmitted signal level, then line drivers can be added to boost the transmitted signal level. If the problem is due to cross phase attenuation caused by transformers, then a capacitor can be used to couple the communication signal across the windings.

The primary problem that everybody is faced with when interfacing to the power line is that the communication media (power line) is different at each installation. The key is to offer a system that is flexible enough to adapt to the demands of the environment.

Summary

Flexibility of the Supertex Encoder-Decoder devices can be utilized to make practical a simple power line interface design that has the capability to transmit data bidirectionally as well as the simple address match On/Off function. This design is only a representation of the many possible new product designs that can result from the use of the Supertex Encoder-Decoder in power line systems.

Supertex inc.

ED Series
Application Note
AN–C7

Encoder-Decoders for Telemetry and Control

Today's industrial environment is the site of a modern revolution – the newest technology in control electronics is available for even the simplest task, at a reasonable price. New techniques of measurement offer increased speed and accuracy with low-cost simplicity. But, interfacing these components in the electrically noisy environment of a modern factory has proved to be a difficult problem. Motors, switches and other high-voltage, high current components used in a factory create a difficult environment for the transmission of the digital signals of the new electronics technology.

A device for maintaining digital data integrity while allowing simple transmission in a factory environment is needed. This device should be easy to interface with (or without) a microprocessor, offer serial transmission to minimize wiring, and be inexpensive. Additional features would include address recognition, so that several devices could be attached to the same control loop, and two-way communication capability.

A family of products meets these requirements. Designed originally for garage-door openers, this series of Encoder-Decoders has performed in many control and telemetry applications, including control loops, cordless phones, security systems, wildlife tracking, pagers, etc. Control loops are addressed here.

Device Description

ED Encoder-Decoders use an address-matching technique. They use CMOS technology to provide low power consumption for battery-operated systems.

Table 1 lists the basic characteristics. The ED-9 performs address-matching only, in the smallest package for lowest cost. The DC-7 allows a combination of 7-bit data transmission for microprocessor applications.

All can be used in either the Transmit or Receive mode by changing the logic level of the T/R pin. This allows the same device to be switched for two-way communications, thus reducing the cost and parts count.

The devices have an on-chip oscillator, using only a resistor and capacitor to set the clock frequency for device operation. The basic clock frequency is 20KHz, with a serial transmission frequency being 1/4 that. The actual data flow rate, which must allow for preamble and delay times, works out to be one "word" every 6.7ms.

Device	Number of Address Bits	Number of Data Bits	Serial Output
ED5	5	0	Yes
DC7	7	8	Yes
ED9	9	0	No
ED11	11	4	Yes
ED15	15	0	Yes

Table 1. ED Series of Encoder-Decoders

Data Transmission

The data transmission for the ED family is a 15-bit serial data "packet" with a 12-bit preamble. The data is Manchester encoded to provide noise immunity.

Manchester code (as implemented in the ED series) divides the time for each data bit in the serial string into two halves. A binary 1 becomes a transition from low to high; a binary 0 becomes a transition from high to low (Figure 1). The first half of each data bit time is always the logical inverse of the second half. This provides for a level of transition (high-to-low or low-to-high) during each data-bit time, and allows a synchronized receiver to easily read the correct data, even when large noise spikes are present. Figure 1 illustrates the Manchester-encoding method.

Each preamble burst, which is sent before the data bits, consists of 12 consecutive bits. The preamble is sent because the receiver of the transmitted signal, another ED family device, has no way of inherently synchronizing with the transmitter. The preamble burst allows a digital phase-locked loop (used in the Receive mode) to "lock in" to the transmitted signal. Then, when the actual data arrives, after the preamble, the Receive device can correctly extract the data from the bit stream. The Receive device also generates a clock signal which is in phase with the data stream (described later).

In the Transmission mode of operation a pulse on the Start/Data Input (SDI) will initiate the transmission of the data packet. The device will send a complete data packet (preamble and data) for each pulse on the start pin.

In the Receive mode, three functional options are available, depending on which device is selected: address matching, data recovery, or a combination of the two. All devices, when enabled in the Receive mode, accept a serial data packet generated by any other ED device. The serial data enters the device on the Start/Data Input (SDI) pin. The 12-bit preamble burst, which arrives first, is routed to the digital phase-locked loop to start and synchronize the R-C oscillator on the device. The 15-bit data word is the next to arrive. This is where the functional types differ.

Matching Operation

In the Receive mode, the data input pins are used to input data to be matched with the data received from the serial transmission. Each device is designed to "match" a different number of bits. If the bits on the data pins exactly match the received data, the Decode/Data Out (DDO) pin goes high until the next stream of serial data arrives at the SDI pin. If the data bits do not match, the DDO pin remains low. This is how the original application to garage-door openers was implemented, and it is the only function that the ED-9 can perform. As shown in Table 1, the ED-9 has no serial data output.

Courtesy Measurement and Controls Magazine

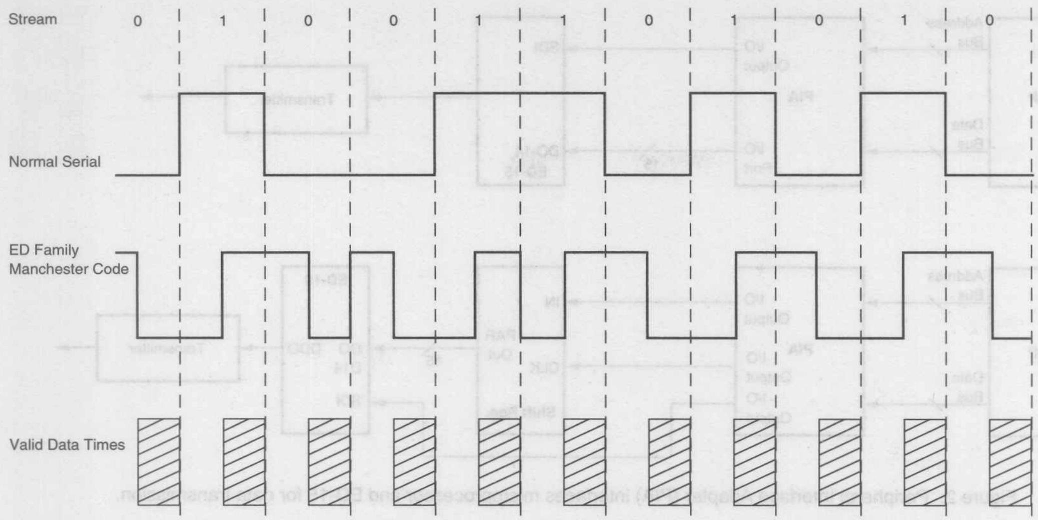


Figure 1. Manchester code converts a binary 1 into a low-high transition, and a binary 0 into a high-low transition.

Data Recovery

All the other ED series devices (ED-15, ED-11, ED-5, DC-7) can be used for data recovery. In these, the received data is carried through the device unaltered, and output on the Serial Data Out (SDO) pin. At the same time, the clock signal is output at the Data Clock (DC) pin. The leading edge of each clock pulse is situated during the time that the data on the SDO pin is correct (valid). The data clock signal can thus be used to load the correct received data into an external shift register for other uses.

This function does not depend on the data-making function, and can be used regardless of whether the data on the data pins matches the received data. When a data word is received, matched or not, the Data Valid (DV) pin goes high to signal the reception of a complete data word. This signal can be used to signal an awaiting system that data is present in the shift register.

Two of these devices (ED-11, DC-7) can use both functions simultaneously to achieve more capability. Both have 15 data input pins, one for each data bit in the Transmission mode. In the Receive mode, however, not all 15 data input pins are matched to the incoming data. In the ED-11, only the 11 most-significant data bits are matched; the 4 least-significant bits are ignored. The DC-7 matches only the 7 most-significant bits of the data; the 8 least-significant bits (1 byte) are ignored. This allows these devices to be used to transmit data (4 bits or 8 bits) to a receiver that is selected by the matching codes (11 bits or 7 bits). The use of this capability will be explained.

Communication media can be via (1) RF transmission (as in garage-door openers), (2) a long direct wire hookup, with digital line drivers, (3) infrared optical link or (4) fiber optic line. Use of the devices is independent of the communication medium used; presentation of a digital serial signal to the receiver input is all that is required. In the following application examples, although one particular communication medium is described, others could be substituted wherever desired.

Microprocessor Interfacing

ED devices are easily interfaced to microprocessor systems for either transmission or reception. If you are working directly with the microprocessor device and using assembly language, the task is made simpler because the microprocessor is fast compared to the ED devices. For data transmission, direct hookup to a Peripheral Interface Adapter (PIA), of the correct number of parallel bits to correspond to the data input pins on the ED device is the simplest interface. An alternative would be using one output from a PIA into a serial shift-register corresponding to the ED data input pins. A simple start pulse generated by the microprocessor after the data bits are set will then send the data out. Figure 2 illustrates these methods.

For the Receive mode, several types of interface are possible, depending on the receive function required. For address-match recognition only, the Data Input pins would be set by manual dip switches, and the Decode pin DDO would be connected to the microprocessor, either on a PIA pin or an Interrupt input. This would tell the microprocessor that a transmitter had called its "name."

For reception of data through an ED device to a microprocessor directly, the ED device would be connected to a serial shift register through the SDO and DC function, to latch the data into parallel format. This shift register would be connected to an input PIA. Either the Data Valid (DV) or Decode (DDO) signal would be used to signal the microprocessor (via an Interrupt input) that data was available to the PIA. The DDO signal would be used only with the ED-11 or DC-7, which combine the matching function with data transmission.

An alternate method of interfacing the ED series device to a fast microprocessor is to connect the serial data output directly to a PIA pin, and use the Data Clock (DC) output as an interrupt to tell the microprocessor that the nest data bit is available. Fast response is necessary in this case.

A third method of interface for data reception is to use a tri-state output shift register, attached directly to the data bus of the microprocessor. An interrupt input from the DDO or DV will let the microprocessor read the data from the shift register in a similar manner as data is read from memory.

These are some of the more common interface possibilities available. Interface to a bundled system where an external parallel port is used may limit input flexibility due to the software overhead involved in using higher-level languages, but effective interface is still easily accomplished.

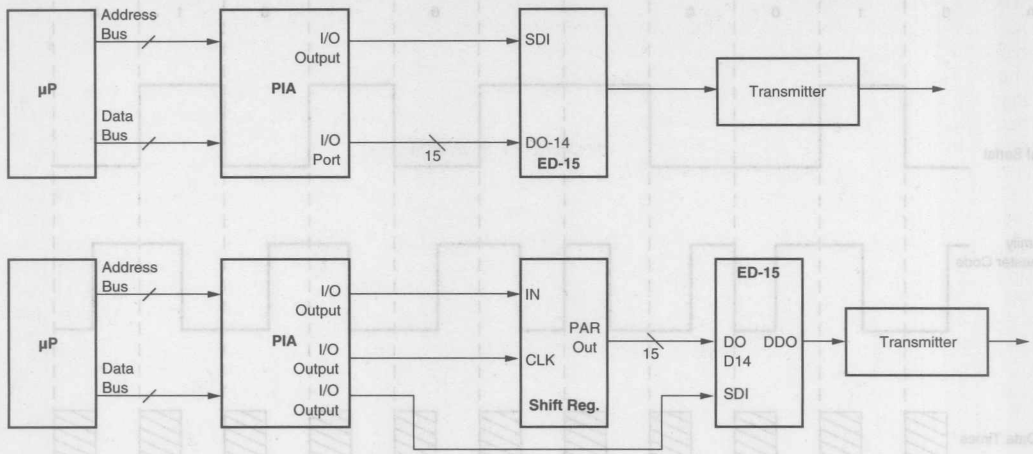


Figure 2. Peripheral Interface Adapter (PIA) interfaces microprocessor and ED-15 for data transmission.

Basic Systems

The simplest use of the ED device is where one transmitter is used with one receiver. For address matching (such as a garage-door opener), the devices are used as shown in Figure 3. The start pulse is generated by a simple push-button. Switch bounce is not a problem because these devices "restart" the transmission each time the SDI pin pulses. Therefore, the last "bounce" will send a complete data packet, which will be received correctly. When the transmission is completed, the Data Valid (DV) pin goes high to signal a successful reception of a correctly formatted signal. If the input data stream also matches the receive device Data Input pins, the Decode Output (DDO) pin also goes high at this time.

A similar simple application for data transmission would use an ED device with serial Data Output and Data Clock to allow data collection at the receiver. In Figure 4, one DC-7 and one ED-15 are used, with the data byte latched into a 4094 serial-to-parallel shift register.

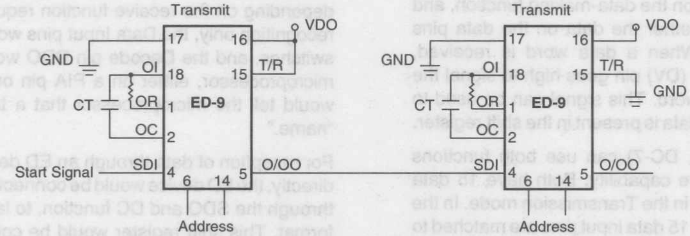


Figure 3. Address matching use.

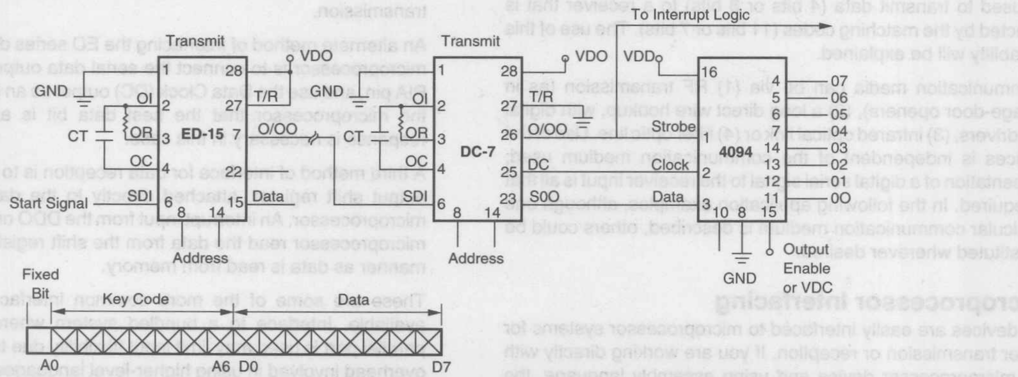


Figure 4. Addressed data transmission. Data is loaded into a shift register and latched if the transmitted address matches the receive address.

Multipoint Control Network

ED-11 or DC-7 devices can be used to implement a simple, low cost multipoint control network using a serial loop daisy-chained to each controlled system. Figure 5A illustrates this interconnect scheme. One transmission device is connected to a common serial data bus with multiple receivers, one per controlled system. The number of receive devices possible is determined by the number of address bits implemented in the transmit and receive devices. The DC-7 can address 128 receivers; the ED-11 can address 2048 receivers.

The transmitting ED device in this type of network is normally connected to a microcomputer of some kind, while the receivers may interface directly to the controlled system. In operation, the microprocessor will select the data word to initiate the desired function in that system. This information is then placed on the Data Input pins or the transmission ED device, and a Start pulse applied to the SDI pin. The serial transmission will be received by all ED devices in the network; however, only the device with a similar address pin code will match and raise the DDO pin high. The SDO pins of the receiver EDs are each connected to serial-parallel shift registers to capture the data word portion of the transmission. The system with the address match will read the command word form the shift register and execute the command.

The serial wire loop is only one implementation of this type of control network. A multipoint "star" type of network (Figure 5B), ideal for a factory floor where visibility is good, could be implemented easily using an infrared transmitter at the control station. Each receiver station would use a infrared detector to receive the signal; no wiring is necessary. Additional receive stations are easily added to the network.

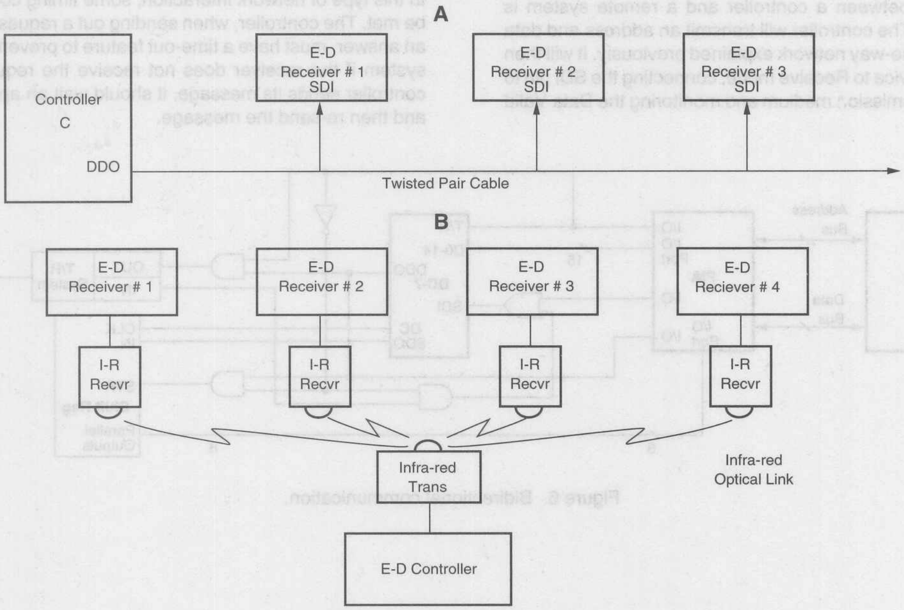


Figure 5. Multipoint one-way control network.

A Bidirectional Network

An enhancement to the network described in the previous section is to implement two-way communication. Many applications require this flexibility, where a controller needs to monitor the status of a remote system, or have a remote instrument make a measurement and report the results to the central controller. This type of network, where the controller sends out a request and receives a response, is called a "polled" system; it is the simplest way to implement two-way communication. No interrupt conflicts are involved, and the controller selects the priority in which the controlled systems are queried.

The capability of ED devices to be switched between transmitter and receiver allows low-cost implementation of two-way communication with a minimum number of parts. Using a microprocessor with the ED data input pins attached to a Peripheral Interface Adapter (PIA) port is the simplest method, although discrete logic is usable for less complex requirements. Figure 6 shows one possible configuration.

The interaction between a controller and a remote system is straightforward. The controller will transmit an address and data word, as in the one-way network explained previously. It will then switch the ED device to Receive mode, connecting the SDI pin to the network transmission medium and monitoring the Data Valid (DV) pin for a signal that a transmission has been received. The SDO and DC pins of the controller are connected to a shift register to receive the information from the remote system.

The remote system, with its ED device in the Receive mode, receives the transmission from the controller and matches the address to the status of its Data Input pins. At the same time, the data word is latched into a shift register through the SDO and DC pins. If an address match is found, the remote system then takes the data word from the shift register and executes the command. If data or status is to be sent back to the controller, the remote system will then apply the data to be sent back to the controller on the Data Input pins associated with the data bits of the transmitted packet. The Decode Data Out (DDO) pin is connected to the transmission media, and Start pulse is applied to the SDI pin. The remote ED device then will transmit the address and data to the controller. The remote system transmits its own address back to the controller with the data to prevent other remote systems from receiving and decoding the transmission in error.

In this type of network interaction, some timing constraints must be met. The controller, when sending out a request and awaiting an answer, must have a time-out feature to prevent lockup of the system if the receiver does not receive the request. After the controller sends its message, it should wait an appropriate time and then re-send the message.

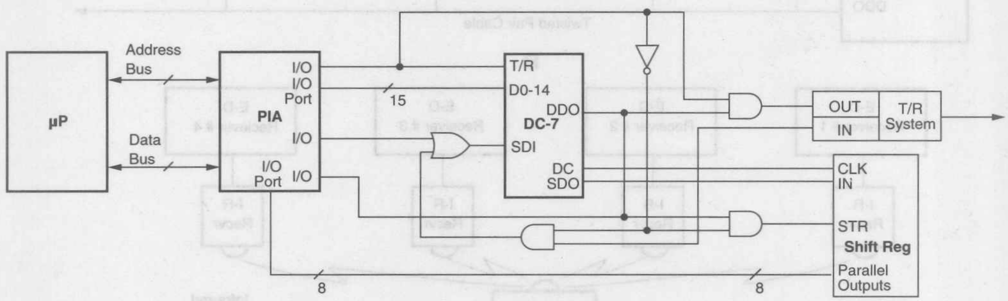


Figure 6. Bidirectional communication.

3

High Voltage Pulser Circuits

Introduction

The high voltage pulser circuit shown in Figure 1 utilizes Supertex complementary N- and P-channel DMOS transistors to achieve excellent performance and efficiency with minimal components. The output voltage swings are -100V to +100V. Rise and fall times are less than 10 nsec while sourcing and sinking over 0.75 and 1.0 amps respectively. The output is conveniently controlled by TTL or CMOS input signals.

High voltage, high speed, and high current pulses at low duty cycles are required in several applications. Ultrasound cleaning equipment, flaw detection, medical imaging, and test instruments are but a few examples. Complementary N- and P-channel DMOS transistors, VN1304N3, VP1304N3, TN0102N3, TP0102N3, TP0620N3, and TN0620N3 are used for their low threshold voltages, low input capacitances and high output current capabilities. These are essential features to generate high voltage pulses with high speeds and currents. Another aspect considered was their cost-effective TO-92 package, which saves board space.

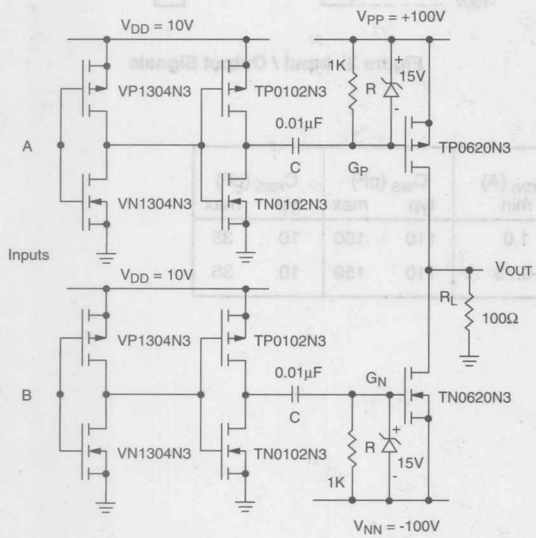


Figure 1. High Voltage Pulser

Circuit Description/Design Considerations

The high voltage pulser in Figure 1 consists of 3 basic stages: (A) input signal interface, (B) high current buffer and level translation, and (C) high voltage and current output drivers. Each stage has its own specific requirements for device parameters, which will be discussed in the following section.

Stage 1:

Stage 1, consisting of VN1304N3 and VP1304N3, is an input stage to interface directly with TTL or CMOS logic signals. Low input capacitance and fast switching speed are the most important considerations in this stage. The VN1304N3 and VP1304N3 are chosen for their low input capacitance, 35pF maximum, and their 2nS typical/ 5nS maximum td(on), tr, td(off) and tf switching speed. This will minimize loading and distortion on the input drive signals. Often the input signals are from fairly resistive sources, which may be in the order of 100's of ohms, creating large RC constants. Low C_{ISS} and C_{RSS} will allow the gate voltage to charge past the transistors' threshold voltage rapidly, to accomplish high speed switching.

The low threshold ratings will accommodate TTL and CMOS compatibility. Max threshold ratings, $V_{GS(th)}$, for VN1304N3 and VP1304N3 are 2.4V and -3.5V respectively. For the 'worst case' design consideration, VN1304N3 will turn on when the input signal voltage reaches 2.4V. For a given input signal voltage rise and fall time of 50 nsec for 0 to 10V, the time required for the input to reach 2.4V is 12 nsec. For VP1304N3, time required to turn on is about 35 nsec. Once the devices are turned on, the output voltage rising and falling edges will have a waveform similar to that of an RC circuit where R is the on-resistance of the transistor and C is the total equivalent capacitance the transistor is driving.

In addition to performing the interface to TTL and CMOS signals and improving rise and fall times, Stage 1 is also a high current low impedance buffer. Output currents of more than 250mA source and 500mA sink (based on $I_{D(ON)}$ specifications of these devices) are available to adequately drive the inputs of the 2nd stage.

Stage 2:

Stage 2 provides high output peak currents, improves rise and fall times, and performs high voltage level translation. This stage consists of device types TN0102N3 & TP0102N3. The Supertex low threshold DMOS transistors TN0102N3 and TP0102N3 provide typical output peak currents of 2.8 amps sink and 1.7A source. Such high currents are required to adequately drive the input capacitances, including Miller effect of the output transistors, to accomplish fast switching speeds. The low threshold guaranteed maximum limits of 1.6V and -2.4V for TN0102N3 and TP0102N3 respectively will further improve rise and fall time transitions. Resistor R and Capacitor C provide the DC level shifting. Value of C should be much larger than C_{IN} of the output stage where C_{IN} is equal to C_{ISS} plus Miller effect: $C_{IN} = C_{ISS} + C_{RSS}\ (G_{FS} \cdot R_L)$. Resistor value R is selected such that time constant RC is much greater than the output high voltage pulse width required.

With the source at +100V, gate voltage driving the P-channel of the output stage are +100V and +90V to provide gate-to-source drives of 0V and -10V. Similarly for the N-channel, with the source at -100V, gate voltages are -100V and -90V to provide 0V and +10V gate-to-source drives.

Stage 3:

Stage 3 is the output stage and consists of Supertex low threshold DMOS discrete transistors TP0620N3 and TN0620N3. These devices have a breakdown voltage rating of 200V minimum. Output voltage swings can switch from -100V to +100V. Input capacitance is increased due to Miller effect, $C_{IN} = C_{ISS} + C_{RSS}\ (G_{FS} \cdot R_L)$. Low C_{RSS} & C_{ISS} capacitance, high output current, low on-resistance and 200V breakdown voltage are required parameters for the output transistors. The Supertex TP0620N3 and TN0620N3 are ideally suited. Their guaranteed parameters are listed in Table 1:

During power up and power down conditions, it is possible for transient voltages greater than 20V to appear across the gate-to-source on the output transistors. Maximum gate-to-source voltage, V_{GS}, is rated at ±20V. 15V zener diodes are connected across the gate and source of the output transistors to protect against such transient voltages. These diodes will not be zenering during normal operation.

The zener protection diodes can be omitted if V_{PP} and V_{NN} can be ramped slowly to their rail voltages during power up.

Input signals and corresponding voltages are shown in Figure 2. Actual output waveforms with a 100Ω load for a 60 nsec and a 100 nsec positive and negative pulse are shown on Figures 3A to 3D. V_{PP} and V_{NN} voltages can be varied without additional changes within the circuitry. For example, V_{NN} can be -10V and V_{PP} +190V for -10V to +190V pulses. Higher voltages and currents can be accomplished with minimal changes.

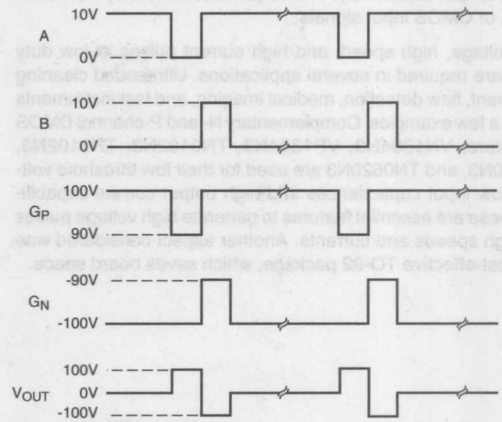


Figure 2. Input / Output Signals

Table 1

DEVICE	BV_{DSS} (V) min	$R_{DS(ON)}$ (Ω) typ	$R_{DS(ON)}$ (Ω) max	$I_{D(ON)}$ (A) min	C_{ISS} (pF) typ	C_{ISS} (pF) max	C_{RSS} (pF) typ	C_{RSS} (pF) max
TN0620N3	200	4.0	6.0	1.0	110	150	10	35
TP0620N3	-200	9.0	12.0	-0.75	110	150	10	35

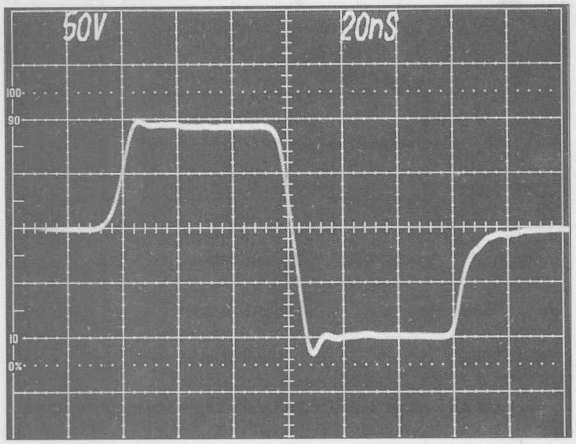


Figure 3A. 60 nsec Output Pulse

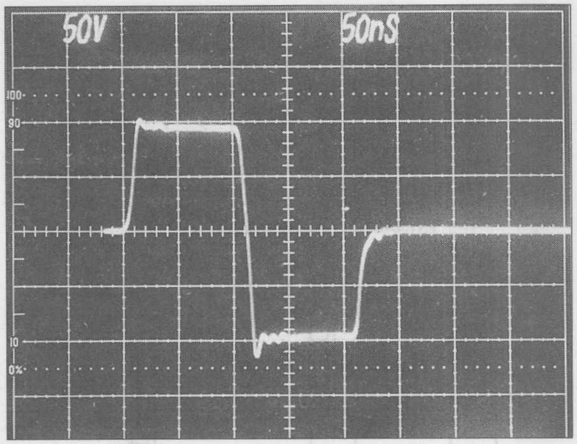


Figure 3B. 100 nsec Output Pulse

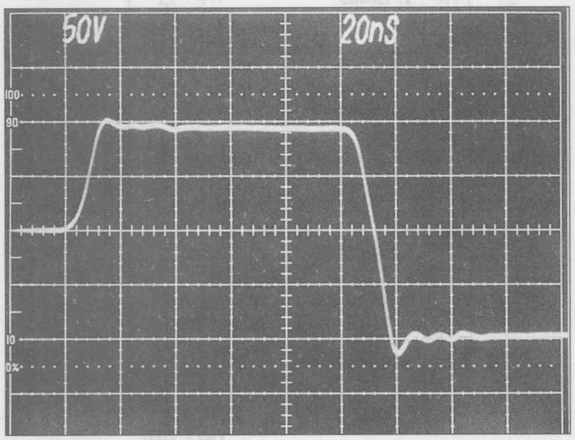


Figure 3C. Positive Going Pulse

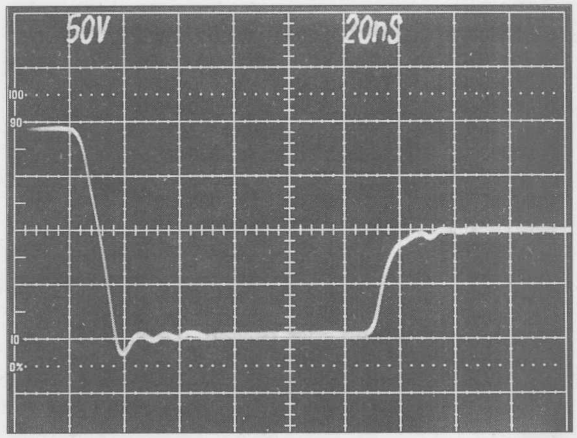


Figure 3D. Negative Going Pulse

Optional Variations

The high voltage pulser in Figure 1 can be easily modified to suit various high voltage pulser needs. Figures 4A to 4D show some examples.

Figure 4A is a positive high voltage pulser with one end pulling to ground. Basically, components R and C are not needed to drive the N-Channel.

Figures 4B and 4C are high and low side open drain pulsers. Supertex VP0650N3 and VN0650N3 are used to satisfy applications with 500V pulse requirements.

Figure 4D utilizes Supertex VN0550N3 and VP0550N3 for high voltage +250V push-pull 100mA requirements. Max input capacitances of VN0550N3 and VP0550N3 are only 55pF and 60pF respectively. These can be driven directly from Stage 1 with minimal loss in switching speed.

Conclusion

Supertex DMOS transistors are ideal for high speed, high voltage, high current pulsing applications. Bipolar transistors require base currents and time to recover from the saturation region. MOSFETs do not require any DC gate current thus enabling them to be easily driven with a simple AC coupling scheme. Because of Miller effect on the high voltage outputs, large peak currents are essential for the second stage to drive the outputs hard for fast switching speeds. The Supertex line of DMOS transistors has low input capacitance ratings making them ideal candidates for high speed, high voltage pulsing applications.

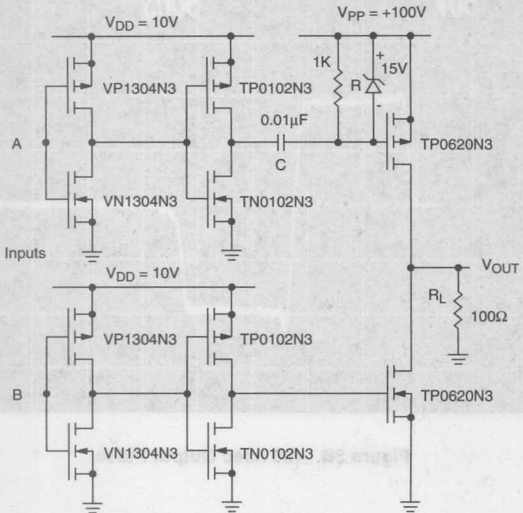


Figure 4A. Push-Pull Positive High Voltage Pulser

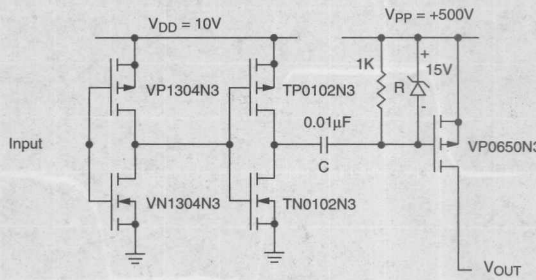


Figure 4B. High Side Open Drain High Voltage Pulser

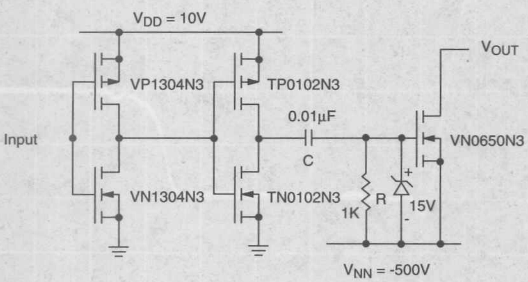


Figure 4C. Low Side Open Drain High Voltage Pulser

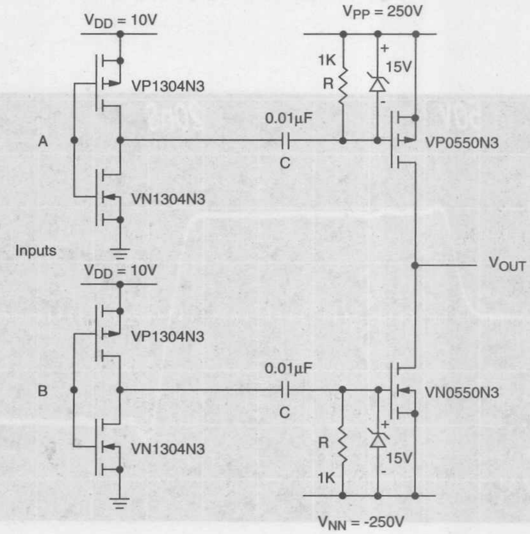


Figure 4D. Push-Pull ±250V High Voltage Pulser

Battery Back-Up Utilizes Low Threshold MOSFETs

Introduction

The simple battery back-up circuit shown in Figure 1 utilizes Supertex low threshold DMOS devices to achieve excellent efficiency.

In fact, one of the main reasons why MOSFETs are gaining popularity is that very low voltage drops, which surpass the performance of various kinds of diodes and bipolar transistors, can be achieved. Many other benefits of low gate threshold MOSFETs are explained in the text.

Circuit Description and Operation

The battery back-up circuit has two modes: 1) Battery charging, and 2) Battery back-up.

1) Battery charging mode

The 120VAC is stepped down via transformer and full-wave rectified by D1, D2, and C1 to 7.5VDC. This 7.5VDC supplies power to RL as well as providing the charging current to the batteries. R1, D3, and D4 generate a 1.2V reference for COMP 1 and 2. D5, R2, R3, C2, and COMP 2 keep Q1 and Q2 off when switch S is closed. The battery, consisting of 5 nickel cadmium cells in series, is being charged with a current set by R8 and the intrinsic drain to source diode of Q2. For fully discharged batteries, there will be a high charge current for a few seconds, rapidly decaying to a slow charge.

As the battery becomes almost fully charged to 6.8V, the current is reduced to a trickle charge current of a few milliamperes. The trickle charge current is further reduced to microamperes when V_{BATT} exceeds 7.0 volts. This is because the voltage across the diode of Q2 is 0.5 volts and will allow only a small amount of current flow. This maintains full charge of the battery, when not in use, over an extended period of operation.

2) Battery back-up mode

When switch S is opened, simulating power outage, unplugged equipment, or blown fuse, the circuit goes into battery back-up mode. COMP 2 turns Q1 and Q2 on. As V_{BATT} supplies the 60 ohm load, COMP 1 monitors the V_{BATT} voltage keeping it from fully discharging, as complete discharge and subsequent cell voltage reversal can degrade the performance of the NiCd battery. The circuit is designed for the COMP 1 to turn Q1 and Q2 off if V_{BATT} is less than 5.5V and on if greater than 6.5V. The hysteresis is designed to avoid oscillation and is set by R4, R5, R6, and R7.

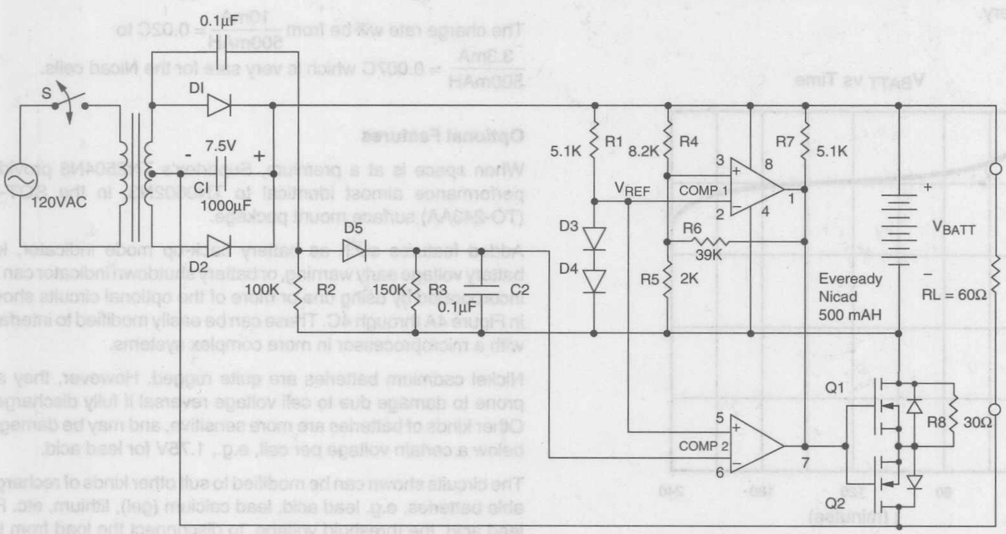


Figure 1. Battery Back-up Circuit

Design Considerations and Component Selection

The design of this circuit utilizes standard, readily available components. The number and different types of components are minimized. Diodes D1 to D5 are 1N4001. All resistors are standard 1/4 watt, 5% tolerance. National Semiconductor's Dual Comparator LM393N is used for its low biasing current. The battery consists of 5 Eveready nickel cadmium cells in series. The cells are AA size, CH15 with a C rating of 500 mAH.

The most important factor to be considered in the design is the selection of the MOSFETs Q1 and Q2, which are configured as an analog switch. In the battery back-up mode, the voltage drop across the MOSFETs must be low to minimize resistive voltage drop and power loss, consequently enhancing battery life.

Supertex TN0602N3, low threshold N-channel DMOS transistors, are selected for their guaranteed low on resistance at low gate drive. Another aspect considered was their cost-effective TO-92 package, which saves board space.

Device Type	$R_{DS(ON)}$ Typical	$R_{DS(ON)}$ Maximum	Test Conditions
TN0602N3	0.9 ohms	1.5 ohms	$V_{GS} = 5V$, $I_D = 750mA$
	0.6 ohms	0.75 ohms	$V_{GS} = 10V$, $I_D = 1.5A$

Q1 and Q2 are easily turned on with a simple pull-up resistor, R7. For a "worst case" design, $R_{DS(ON)} = 1.5$ ohms and a load current of 125 mA are used. Maximum voltage drop across Q1 and Q2 works out to only 375 mV. In actual operation, this voltage drop is substantially lower because the typical value of $R_{DS(ON)}$ is 0.8 ohms. The voltage drop across Q1 and Q2 was measured to be 200 mV.

Figure 2 is a discharge curve of V_{BATT} vs Time showing battery back-up operation of approximately 4 hours. Figure 3 is a charge curve of the battery.

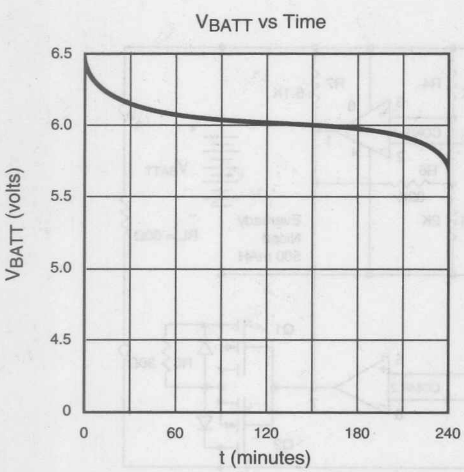


Figure 2. V_{BATT} Discharge Curve

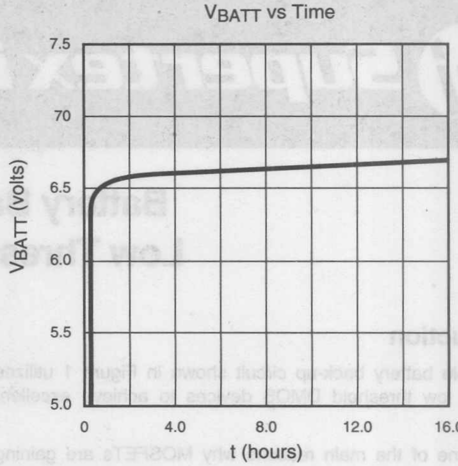


Figure 3. V_{BATT} Charge Curve

The component selection ensured that basic charging current guidelines for Nicad cells were not violated. Assuming the worst case, using fully discharged batteries, the maximum charging current will be 227mA.

$$\frac{\text{Rectified D.C. voltage - diode drop}}{R8} = \frac{7.5 - 0.7}{30} = 227mA$$

This current will last only for a few seconds, and is completely safe for the battery as well as Q2.

In the charging mode, the battery voltage will be between 6.5V to 6.7V for the majority of the time. The charging current will be from

$$\frac{7.5 - 6.5 - 0.7}{30} = 10mA \text{ to } \frac{7.5 - 6.7 - 0.7}{30} = 3.3mA$$

The charge rate will be from $\frac{10mA}{500mAH} = 0.02C$ to

$\frac{3.3mA}{500mAH} = 0.007C$ which is very safe for the Nicad cells.

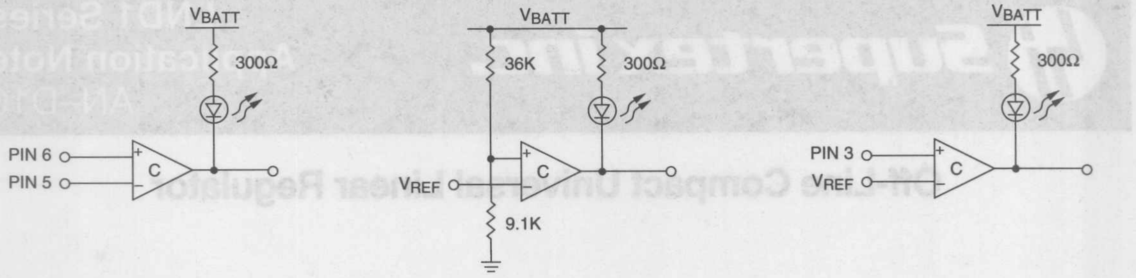
Optional Features

When space is at a premium, Supertex's TN2504N8 provides performance almost identical to TN0602N3, in the SOT-89 (TO-243AA) surface mount package.

Added features such as battery back-up mode indicator, low battery voltage early warning, or battery shutdown indicator can be incorporated by using one or more of the optional circuits shown in Figure 4A through 4C. These can be easily modified to interface with a microprocessor in more complex systems.

Nickel cadmium batteries are quite rugged. However, they are prone to damage due to cell voltage reversal if fully discharged. Other kinds of batteries are more sensitive, and may be damaged below a certain voltage per cell, e.g., 1.75V for lead acid.

The circuits shown can be modified to suit other kinds of rechargeable batteries, e.g. lead acid, lead calcium (gel), lithium, etc. For lead acid, the threshold voltage, to disconnect the load from the battery can be adjusted to 1.75 volt per cell.



A) Battery Back-up Mode Indicator B) Low Battery Voltage Early Warning C) Battery Shutdown Indicator

Figure 4. Optional Circuitry

Conclusion

Very low drain to source voltage drops can be achieved with MOSFETs. Bipolar transistor performance is limited by VCE (sat) and diodes by VF, depending upon the semiconductor material used. This circuit utilized the following features of MOSFETs:

1) Low drain to source voltage drop.
2) Complete turn-on/off of bidirectional currents.
3) Turn-on with low biasing voltages.
4) No biasing power compared to base current loss in bipolar transistors.
5) Utilization of the intrinsic drain to source diode for limiting charging currents to efficient and safe levels.

The battery back-up circuit described demonstrates the benefits of Supertex N-channel low gate threshold devices. These are available in either surface mount (TN2504N8) or TO-92 (TN0602N3) packages. These are ideally suited for battery powered applications. Very often, circuit designs require low on resistance to prolong battery life, low gate drive to meet battery voltage limitations, and small packages to accommodate board space limitations. The Supertex low threshold DMOS discrete transistor family were designed to satisfy such requirements.

Off-Line Compact Universal Linear Regulator

Introduction

An off-line compact universal linear regulator is shown in Figure 1. The regulating device is the Supertex LND150N3. The LND1 is a 500V N-channel depletion mode MOSFET with gate-to-source ESD protection. The regulated voltage, V_{OUT}, is an ideal supply for CMOS ICs and a variety of other circuits that require low current.

Circuit Description

The 120V AC input voltage is rectified by a full bridge, consisting of diodes D_1, D_2, D_3, and D_4. A small filter or smoothing capacitor, C_1, is used to hold the rectified voltage to approximately +170VDC.

The unregulated 170VDC is connected to the drain of the LND1. The LND1 and trimpot R_1 are configured as a 1.0mA constant current source. The 1.0mA constant current flows through R_2 which is a 5.1Kohm resistor to ground. A constant voltage drop of 5.1V is developed across R_2. V_{OUT} is taken as the voltage across R_2 and is used to supply, for example, a simple CMOS timer circuit.

Capacitor C_2 is a low voltage bypass capacitor to supply any peak current required by the CMOS timer circuit during switching transitions. D_5 is a 5.6V zener diode used to clamp transient voltages that may occur during powering up the 120VAC input line. D_5 does not conduct during normal operation.

Calculations for Component Values

C_1 is a 0.1µF 200V capacitor, chosen to minimize ripple on the 170VDC which would affect the regulated output voltage. The minimum value of C_1 is calculated as follows:

$$V_{IN} = A \sin 2\pi ft;\ A = 170V,\ f = 60Hz$$

$$I = C_1 \frac{dv}{dt};\ I = 1.0mA$$

$$dv = \Delta V = A - V_{OUT} - [I_{D(ON)} \bullet R_{DS(ON)}];\ dt = \Delta t = \frac{1}{2f}$$

$$C_1 \geq I \frac{\Delta t}{\Delta V} = (1.0mA)\left(\frac{\frac{1}{2(60Hz)}}{170V - 5.1V - (10mA)(1K\Omega)}\right)$$

$$C_1 \geq 0.054\mu F$$

The LND1 can maintain a virtually constant current over a wide input voltage range. Large ripple voltages on the drain of the LND1 will have very little effect on the output current. The device can also withstand transient voltages up to 500V.

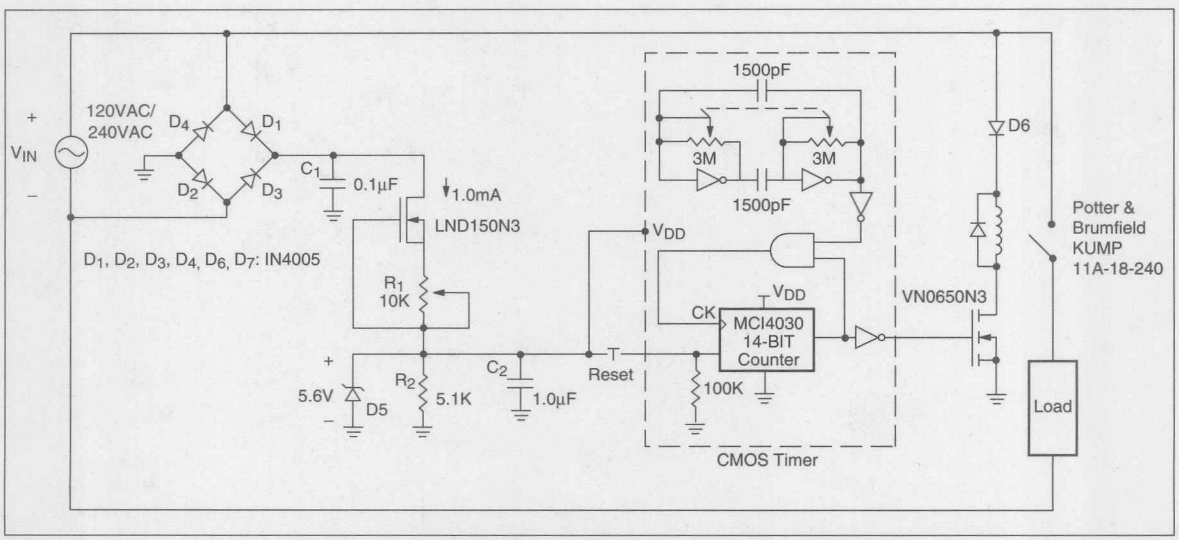


Figure 1. Linear Regulator

The value of the constant current source is a function of R_1, V_P, and I_{DSS} where V_P and I_{DSS} are characteristics of the device. R_1 is a variable resistor adjusted for 1.0 mA and is approximated by:

$$R_1 = \frac{V_P}{I_D}\left(\sqrt{I_D/I_{DSS}} \;-1\right)$$

where, I_D = desired constant current value,

V_P = pinch-off voltage, and

I_{DSS} = saturation current at V_{GS} = 0 V.

V_P and I_{DSS} may vary from lot to lot. The range of adjustment for R_1 is calculated for operation over the range of LND1 values for V_P and I_{DSS}.

Symbol	Parameter	Min	Max
V_P	Pinch-off Voltage	-1.0V	-5.0V
I_{DSS}	Saturation Current	-1.0mA	-10.0mA

For the above values, R_1 is calculated to be from 0 to 6.6Kohm. A 10Kohm trimpot is chosen for R_1.

Since the constant current is adjusted to 1.0mA, R_2 is chosen to be 5.1K to obtain a Vout of 5.1 VDC. The value of C_2 is selected to supply the peak current required by the load on V_{OUT} over a period of time. C_2 can be calculated as follows:

$C_2 = I_{OUT}(dt/dV_{OUT})$ where, I_{OUT} = output current

dt = required time duration of I_{OUT}

dV_{OUT} = acceptable change in V_{OUT}

For example, a 10.0mA output peak current for a duration of 1.0µsec with a maximum V_{OUT} drop of 100mV will require a C_2 value of 1.0mA(1.0µsec/100mV) = 0.1µF or greater. C_2 is chosen to be 1.0µF.

Figure 2 is an oscilloscope picture showing the actual voltage waveforms on the drain of the LND1 and V_{OUT}.

Figure 3 is an output characteristic showing the regulation of the circuit over a wide range of input voltage.

Alternative Applications

For a 10V source, R_2 can be replaced with a 10K resistor. Applications requiring multiple voltage references can be generated by using a string of resistors as shown in Figure 4.

The constant current can easily be changed by readjusting R_1 for the desired current. However, the power dissipation on the LND1 should be taken into consideration. P_D for the LND1 in the TO-92 package should not exceed $I_{DS}(V_{IN}-V_{OUT})$ = 600 mW.

Universality

The universality of the linear regulator can benefit a variety of industrial or consumer applications as it can be used from a very wide range of input voltages, anywhere in the world. Input voltages can be up to 450V for linear regulation. Protection is afforded for line voltage transients up to 500V since the LND1 breakdown voltage is guaranteed to be greater than 500V. A simple, low cost, transient protection (e.g., MOV) will protect the circuit from virtually anything, other than a direct lightning strike.

Regulation can also be achieved with AC or DC voltages from 6.8V to 240V with no modifications of the circuit. This allows manufacture of one model of equipment for worldwide usage without any voltage setting tappings.

Conclusion

The Supertex LND1 can be configured as a simple, constant current source to create an economical compact off-line, low current regulated, voltage supply for powering CMOS ICs and other low current loads. The need for transformers can be eliminated.

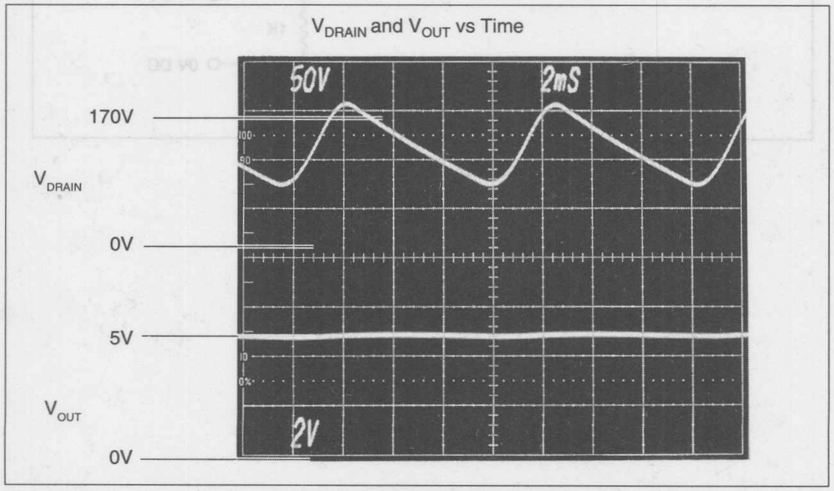


Figure 2. Input/Output Waveforms

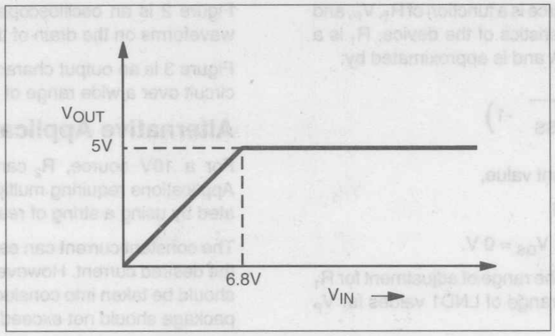


Figure 3. V_{OUT} vs V_{IN}

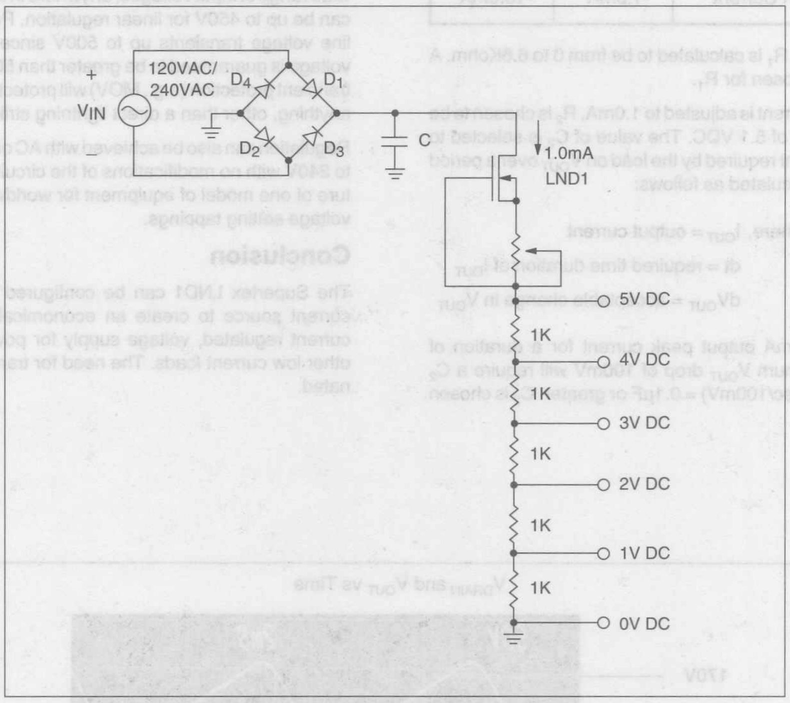


Figure 4. Multiple Voltage References

±500 Volt Protection Circuit

Introduction

A ±500V protection circuit for low voltage high impedance measuring instruments is shown in Figure 1. The protection is accomplished by limiting the amount of current going into the measuring instrument. The circuit will protect against destructive high voltages inadvertently connected to the probes (V_{MEAS}) of up to 500VDC of positive and negative polarity.

Circuit Description

The circuit consists of two transistors, Q_1 and Q_2, and one resistor, R. Both Q_1 and Q_2 are Supertex LND150N8, 500V N-channel depletion mode MOSFETs with gate-to-source ESD protection in a SOT-89 surface mount package. Q1 and Q2 are configured back-to-back as two constant current sources with a nominal value of 1.0mA. Resistor R sets the current limiting value. Figure 2 is a typical low voltage high impedance measurement instrument. Figure 3 is a simplified equivalent circuit showing the protection scheme.

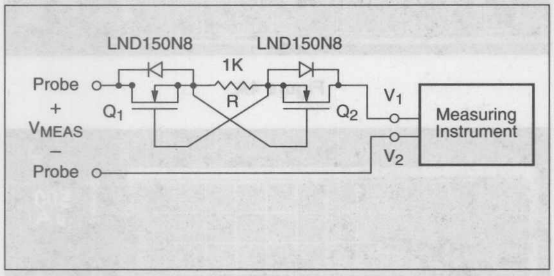


Figure1. ±500V Protection Circuit

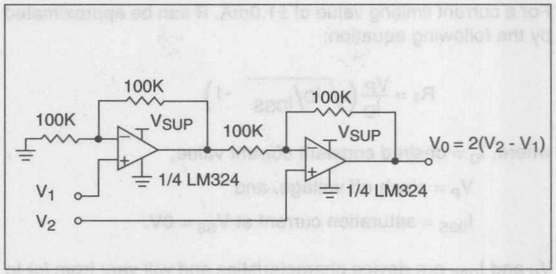


Figure 2. Typical Low Voltage High Impedance Measurement

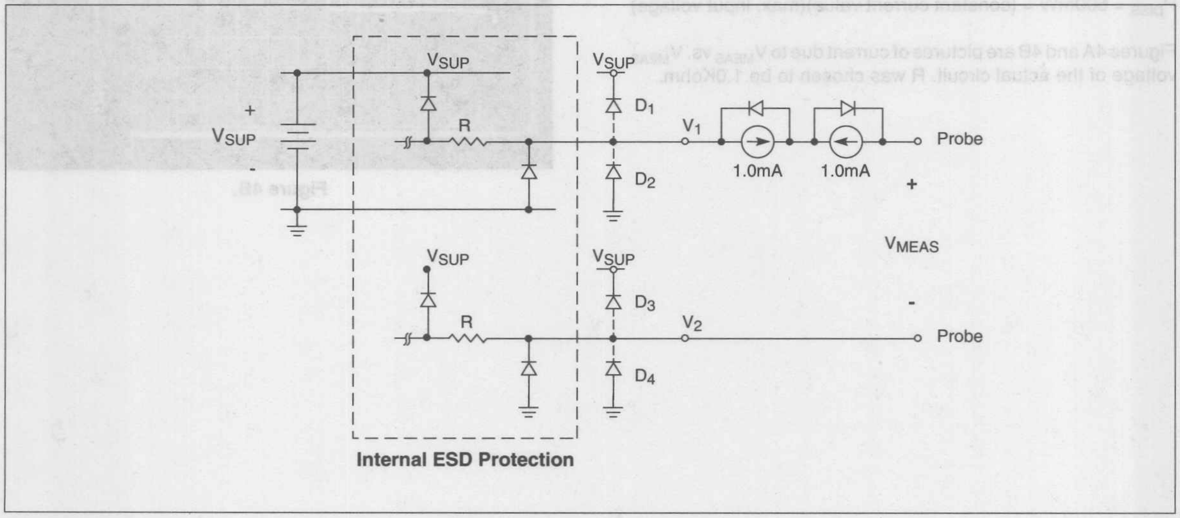


Figure 3. Equivalent Circuit

Under normal operation, the absolute value of V_{MEAS} is less than the supply voltage of the circuit. Q_1 and Q_2 will be fully on with a maximum guaranteed R_{DS} of 1.0Kohms. Since the instrument's input impedance is typically very high, say above 10Mohms, the additional 2.0Kohm series resistance from Q_1 and Q_2 will not affect measurement accuracy.

Under the fault condition, the absolute value of V_{MEAS} is greater than the supply voltage, Q_1 limits the current to 1.0mA against large positive voltages and Q2 limits the current to -1.0mA against large negative voltages across V_{MEAS}.

For example, if V_{MEAS} is connected to ±500V, Q_1 and Q_2 will limit the input current to ±1.0mA causing the input voltage to the measurement instrument to clamp to 1.3V above its supply voltage (when R = 600Ω) and 0.7V below ground.

Typically the measuring instrument has ESD protection diodes connected from both probes to its power supply and ground. The ESD protection diodes can usually handle 1.0mA continuously. In case there are no ESD diodes provided, external diodes D_1, D_2, D_3, and D_4 can be added.

Calculation for Resistor Value

For a current limiting value of ±1.0mA, R can be approximated by the following equation:

$$R_1 = \frac{V_P}{I_D}\left(\sqrt{I_D/I_{DSS}} \;\; -1\right)$$

where, I_D = desired constant current value,

V_P = pinch-off voltage, and

I_{DSS} = saturation current at V_{GS} = 0V.

V_P and I_{DSS} are device characteristics and will vary from lot to lot. Actual constant current values are not critical as long as the power dissipation of the LND1 is less than 600mW.

P_{DISS} = 600mW = (constant current value)(max. input voltage)

Figures 4A and 4B are pictures of current due to V_{MEAS} vs. V_{MEAS} voltage of the actual circuit. R was chosen to be 1.0Kohm.

Conclusion

The high voltage protection circuit is ideal for both bench measurement and handheld measurement instruments. It is simple, reliable and cost effective. It eliminates the possibility of input damage to very sensitive and expensive high impedance devices within the measurement instrument.

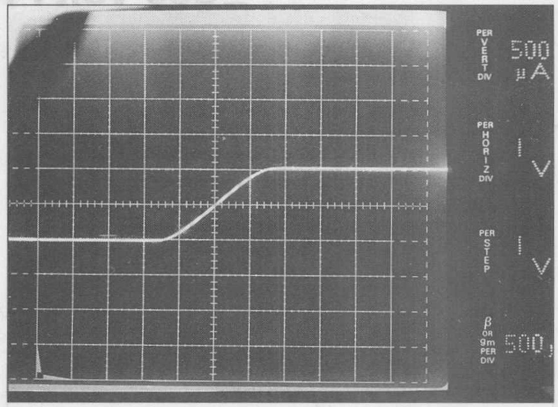


Figure 4A.

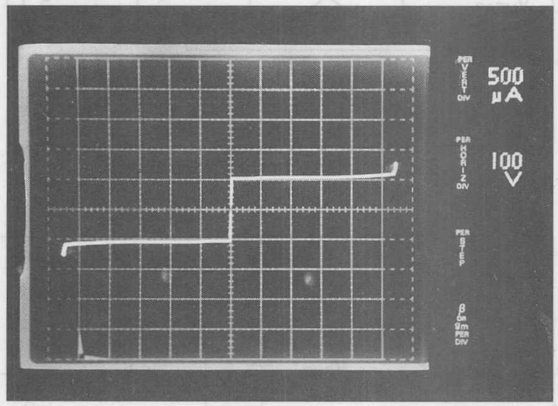


Figure 4B.

High Voltage Ramp Generator

Introduction

A low cost 500V high voltage ramp generator is shown in Figure 1. High voltage ramps are ideal for applications requiring a linear relationship between output voltage and time, e.g., high voltage sweeping, automatic test equipment and piezo electric drivers.

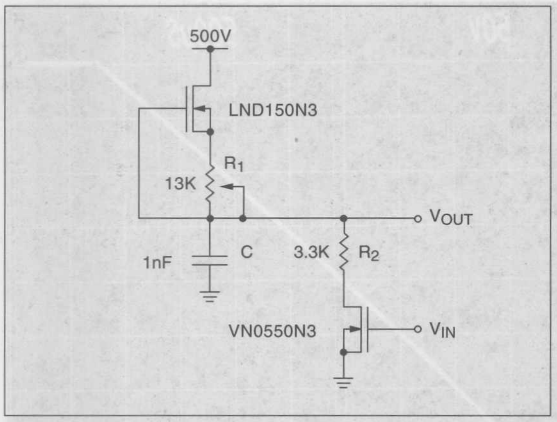


Figure 1.

Circuit Description

The high voltage ramp generator shown in Figure 1 utilizes two Supertex high voltage DMOS transistors, the LND150N3 and the VN0550N3, two resistors, R_1 and R_2, and a capacitor C. R_1 is a trimpot resistor. The LND150N3 is a 500V ESD protected N-channel depletion-mode MOSFET and the VN0550N3 is a 500V N-channel enhancement-mode MOSFET. Both transistors are available in the TO-92 package.

The LND1 is configured as a constant current source charging a capacitor C. R_1 introduces negative feedback to regulate and set the desired constant current value. When the constant current source begins charging capacitor C, a voltage ramp is generated across the capacitor. The voltage ramp, V_{OUT}, is the voltage across the capacitor.

The VN05 can be turned on with TTL or CMOS control signal to reset the ramp voltage V_{OUT} by discharging the capacitor to ground through R_2. The VN05 has a typical On-Resistance of 45 ohms at 10V gate drive and 50 ohms at 5V gate drive. Resistor R_2 is calculated to limit the discharge current for the VN05 to operate within its SOA rating.

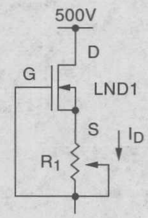
Calculations for Component Values

The ramp is designed to be 0.1 V/μsec. Capacitor value C should be kept small to reduce charging and discharging a large amount of energy. The selection of C should be large enough so that output loads and stray capacitances will not introduce significant error. C is chosen to be 1.0 nF.

The charging characteristic for a capacitor is $I = C\,(dv/dt)$.

$I = 1.0\text{ nF} \times 0.1\text{ V}/\mu\text{sec} = 100\ \mu\text{A}$.

Calculating R_1 for a 100 μA constant current source:



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2,\ V_{GS} = -I_D R_1$$

$$= I_{DSS}\left(1 + \frac{I_D R_1}{V_P}\right)^2$$

Solving for R_1:

$$R_1 = \frac{V_P}{I_D}\left(\sqrt{I_D/I_{DSS}} - 1\right)$$

V_P = pinch-off voltage. Measured value = -1.6V.

I_{DSS} = saturation current at V_{GS} = 0V. Measured value = 3.0 mA.

Calculating for R_1 using the typical values:

$$R_1 = \frac{-1.6V}{100\mu A}\left(\sqrt{100\mu A/3.0mA} - 1\right) = 13.1K\Omega$$

R_1 should therefore be adjusted to approximately 13.1Kohms.

During power up and down, it is possible to have high transient voltages to the gate of the LND1. The LND1 internal ESD gate-to-source protection will protect the device against such transients.

The VN05 performs the reset function by discharging capacitor C through resistor R_2. The VN05's low output capacitance, (C_{OSS}) of 10pF max, minimizes additional parallel capacitance across capacitor C.

It is desirable to discharge V_{OUT} rapidly and as close to ground as possible. This can be accomplished with a low value R_2. However, care should be taken not exceed the SOA rating of the VN0550N3.

Maximum peak power for VN05 in a TO-92 package is 3.0W. Calculating for a minimum R2:

$$P_{DISS} = I_D \bullet V_{DS},\ V_{DS} = 500V - (I_D \bullet R_2)$$

$$I_{D(ON)}\ \text{min} = 150mA,\ P_{DISS} = 3.0W$$

$$R_2 = (1/I_D)(500V - P_{DISS}/I_D)$$

$$= (1/150mA)(500V - 3.0W/150mA)$$

$$= 3.2K$$

R_2 is set to a standard resistor value of 3.3K.

Figures 2 and 3 show two different input signals with their corresponding output voltage ramps. The ramp can be adjusted by varying R_1.

Conclusion

The LND1 is ideally suited for high voltage, low constant current source applications. High voltage ramp generators, high voltage triangular waveform generators, high voltage references, biasing circuitry and active loads for discrete high voltage amplifiers are some examples.

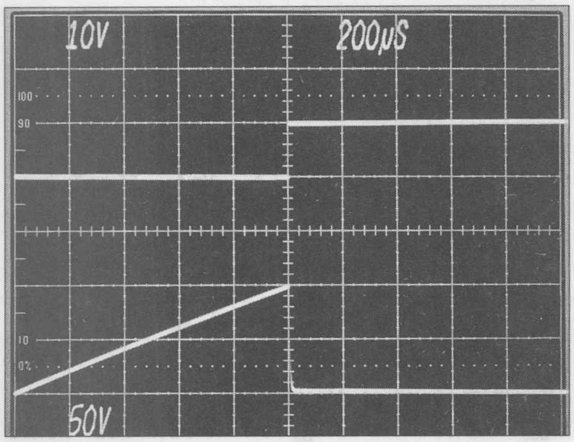


Figure 2.

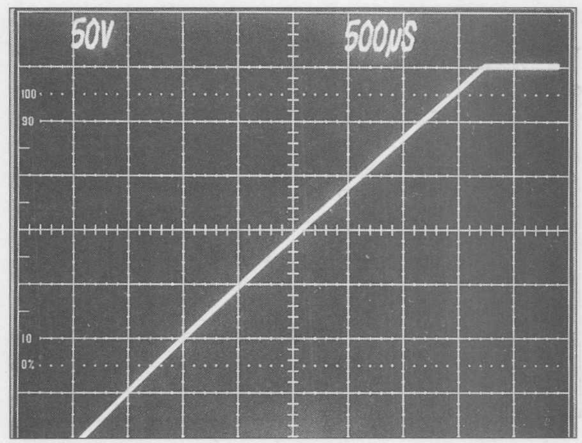


Figure 3.

Designing High-Performance Flyback Converters with the HV9110 and HV9120

by Ray Ruble, Applications Engineer

Introduction

Although the HV91XX family of PWM ICs can be used to control single-switch converters of any topology or size, their primary usage is in low-cost, low to medium power, discontinuous-mode flyback converters. Designing such converters is relatively simple and quick if one has a basic understanding of how a flyback converter functions. It is the purpose of this note to provide such an understanding, and to illustrate, with a couple of examples, one way in which such a converter design can proceed. It should be noted that this is an engineering approach, meant to allow the user to develop a working design quickly, not a textbook approach meant to teach underlying theory. Safety margins are taken into account, and the path taken through the design is intended to make these margins work with each other in order to generate an economical and producible power supply. Many apparently arbitrary values are used. They *are* arbitrary, and different ones could have been used that would have resulted in different power supplies, that would have been, for whatever feature was optimized, just as valid as the examples chosen.

On Flyback Function

A flyback converter functions, as does almost every other switchmode converter, by storing energy in an inductor during a main switch ON period, then discharging the stored energy into a load during the switch's OFF period. The trickiness to this (if there is any) is that the inductor has two or more windings, (an input winding and one or more output windings) and that the current flow alternates between the input and output windings, with effectively no current (other than a little leakage) flowing in the nonconducting winding while its partner carries the current.

The way a flyback converter works can lead to some confusion if the designer tries to approach the design of its magnetic as if it were a transformer, because, except for the case of multiple output windings, the magnetic in a flyback converter is NOT a transformer. Perhaps the easiest way to view the magnetic in a flyback converter is as an *energy bucket* which is alternately filled (when the main switch is ON) and dumped (when the switch is OFF). A flyback magnetic is NOT a transformer despite its superficial resemblance to one: A transformer functions as a voltage-in, voltage-out power transfer device, where input and output windings conduct simultaneously. A flyback magnetic is an energy-in, energy-out power transfer device where the input and output windings do *not* conduct current simultaneously. Obviously, voltages present on the active winding are reflected, by the turns ratio, to the inactive winding, but the old saw "The voltage on the main switch is twice the input voltage" is incorrect, because the voltage reflected from the output winding can be either higher or lower than the input voltage (generally it is lower) depending on the voltage at the output, and the time allotted for the output inductance to discharge into it. Discontinuous-mode operation merely means that all the energy (neglecting losses) put into the coupled inductor during one time period when the main switch is ON is then emptied out during the following period when the main switch is OFF. No energy is carried forward to a subsequent cycle. *(See Figure 1.)*

For both converter and magnetic design, a flyback magnetic can be thought of as two independent inductors which share a common core. Once the designer is accustomed to thinking of the flyback magnetic as a dual inductor, the rest of the design becomes easier.

What the designer needs to do is define the output side inductor so that it delivers enough energy to the load, while the switch is off, to produce the desired current at the desired voltage. Next, define the input side of the inductor so that it takes in enough energy when the switch is on to provide for both the output and system losses. To facilitate this, a conversion formula is necessary:

$$I_{DC} = I_{pk} \bullet \sqrt{\frac{t_{ON}}{3t_{period}}}$$

This formula converts DC to peaks of noncontiguous triangle waves.[1]

If we deal with ON time as a percent of total clock period, (duty cycle) and define

$$D = \frac{t_{ON}}{t_{period}}\ ;\ 1\text{-}D = \frac{t_{OFF}}{t_{period}}$$

the formula reduces to:

$$I_{DC} = I_{pk} \bullet \sqrt{\frac{D}{3}} \quad \text{for the input side and}$$

$$I_{DC} = I_{pk} \bullet \sqrt{\frac{1-D}{3}} \quad \text{for the output side}$$

Because the designer knows the length of time the switch will be ON and OFF (these are defined by the clock frequency and the PWM IC used) as well as the input and output voltages desired, the peak currents found from the formulae can be used with the defining formula for inductance

$$E = L \bullet (dI/dt)$$

to determine the required inductances for the input and output sides of the coupled inductor. In the process, the rest of the design generally falls into place.

Data Needed to Start the Design

1. Minimum and Maximum Input Voltage
2. Nominal Output Voltage(s) and Tolerance(s)
3. Maximum Output Wattage
4. Minimum Output Wattage
5. Maximum Allowable Output Ripple
6. A defined clock frequency
7. A list of mechanical and thermal constraints (if any)

Operating Frequency

Most designers approach converter design with the idea of operating at the highest possible frequency that is convenient. This is generally a useful approach, because it minimizes the size and cost of output capacitors and the coupled inductor. However, it is not always the best way to choose a frequency. In the case of low-power converters, once the magnetics are reduced in size to a vendor-dependent minimum, further reductions in size will raise the cost of the magnetics. Very small cores and ultra-fine wire are hard to handle.

There is another important consideration in the choice of frequency that is often overlooked: dynamic range. If the difference between the widest pulse a PWM IC can generate (which is a function of its operating frequency) and the narrowest pulse it can produce (a function of the PWM IC's speed and internal structure) is small, the ratio between $P_{out(max)}$ at low line and $P_{out(min)}$ at high line must also be small, or reducing the size of the inductor and output filters will be paid for by increasing the size and cost of the EMI filter. Further, if the PWM IC selected cannot handle the full range of pulse widths required, it will start cycle-skipping (failing to turn on at all for some cycles).

While most PWM ICs, including the HV91XX family, can simply skip cycles by not turning on at all, if the differential between V_{in} and P_{out} becomes too great, skipping cycles reduces the effective clock frequency of the converter, and re-defines the minimum frequency for which the input EMI filter must be designed. For example, if the converter skips every other cycle at high line/light

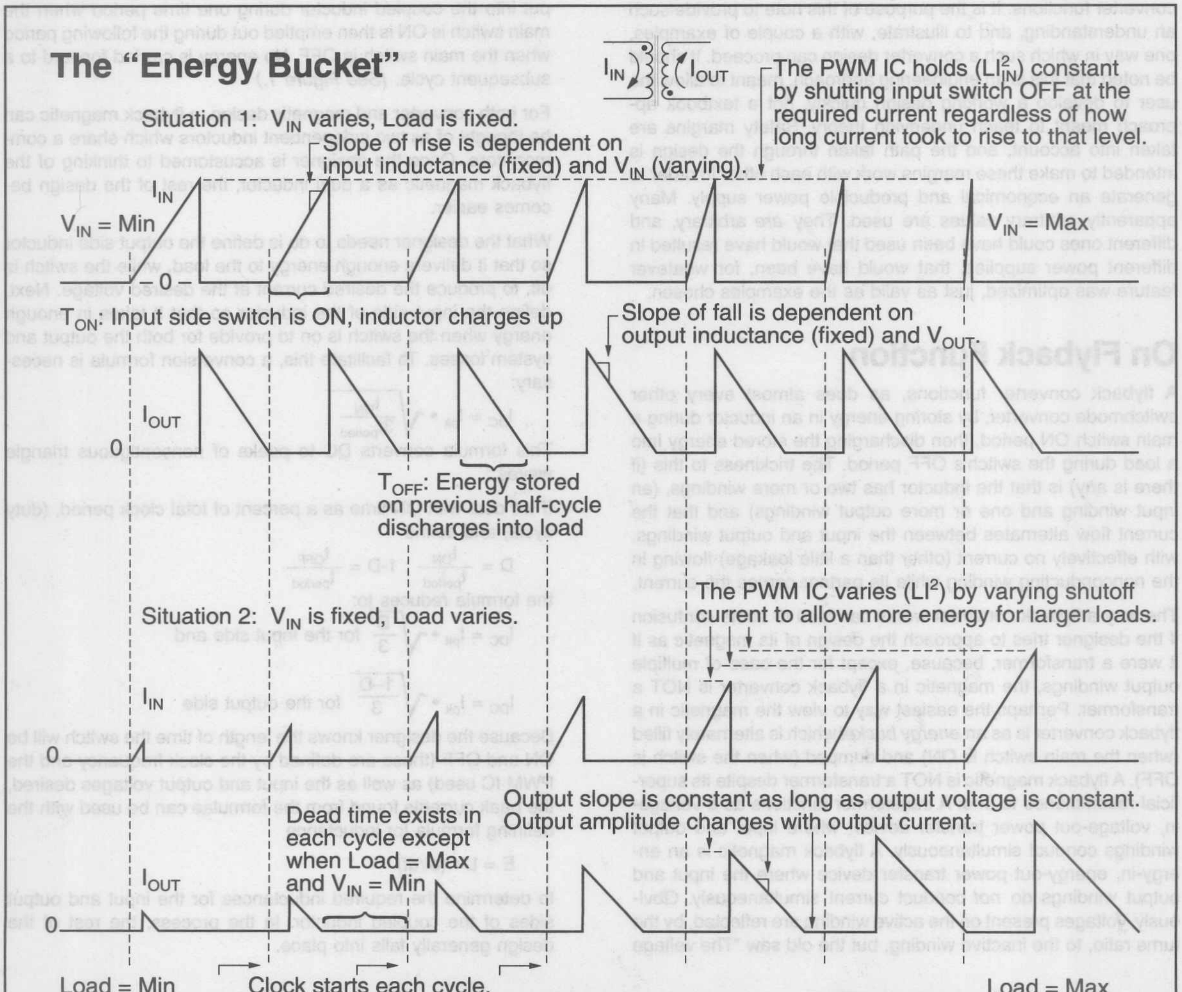


Figure 1

load, the size (and cost) of the EMI filter can be doubled. Cycle skipping also increases either the size of the output capacitors or the amount of ripple on the converter's output.

Recently, dynamic range has been overlooked because most bipolar PWMs do not have a wide dynamic range. For example, a bipolar 1845 PWM operating at 50KHz has a dynamic range of only ≈17.6:1. A CMOS 9110, in contrast, has a dynamic range of >120:1 at 50KHz. Proper use of dynamic range can have a significant effect on EMI filter cost.

Another consideration in choosing an optimal frequency is switching power loss, which increases linearly with frequency in non-resonant converters.

Example 1

A 48W converter patterned after an instrument power supply. This will be a simple generic example with no bells and whistles. First, we need the input parameters listed above:

Maximum Input Voltage: 65VDC

Minimum Input Voltage: 18VDC

Outputs: A: 5.0V, ±1%, 0.25 to 8A, ≤ 25mV ripple

B: 12.0V, ±5%, 0.01 to 0.7A, ≤ 0.5V ripple

Maximum Output Wattage: 48.4W

Minimum Output Wattage: 1.37W

Operating Frequency: 50KHz

(See Figure 2.)

An HV9110, which will accept input voltages of up to 120V is used. As previously noted, this chip will allow a dynamic range sufficient to handle the stated line/load variations at 50KHz. Setting the clock frequency requires selecting an appropriate timing resistor. From a graph on the data sheet, the appropriate resistor for 50KHz operation is ≈330KΩ. This however does not account for the tolerance of either the resistor or the chip. To ensure that all device-resistor combinations operate at or above 50KHz, 261KΩ is a better choice. The reason that the clock frequency should be set to a minimum rather than a nominal value, despite the reduction in dynamic range this causes, is to prevent the slowest converter from saturating its coupled inductor. While magnetic saturation does not cause damage in a current-mode converter as it would in a voltage-mode converter, it still causes additional dissipation and stress on the main switch. It can also limit power throughput.

The Design

First, translate the RMS current of the major output winding at maximum load to a peak current. From the data sheet for the HV9110 it can be seen that maximum ON time for a cycle is 50% minus approximately 150 nsec. At 50KHz, this amounts to a little over 49%. We can declare a maximum duty cycle (D) of .49 and allow a small safety margin. If D_{MAX} is .49, then minimum 1-D is .51. Using .50 as a value for 1-D (thus allowing a 1% overall dead band as safety margin) determine peak secondary current:

$$I_{pk(5V)} = 8.0A \div \sqrt{\frac{.50}{3}} = 19.59A$$

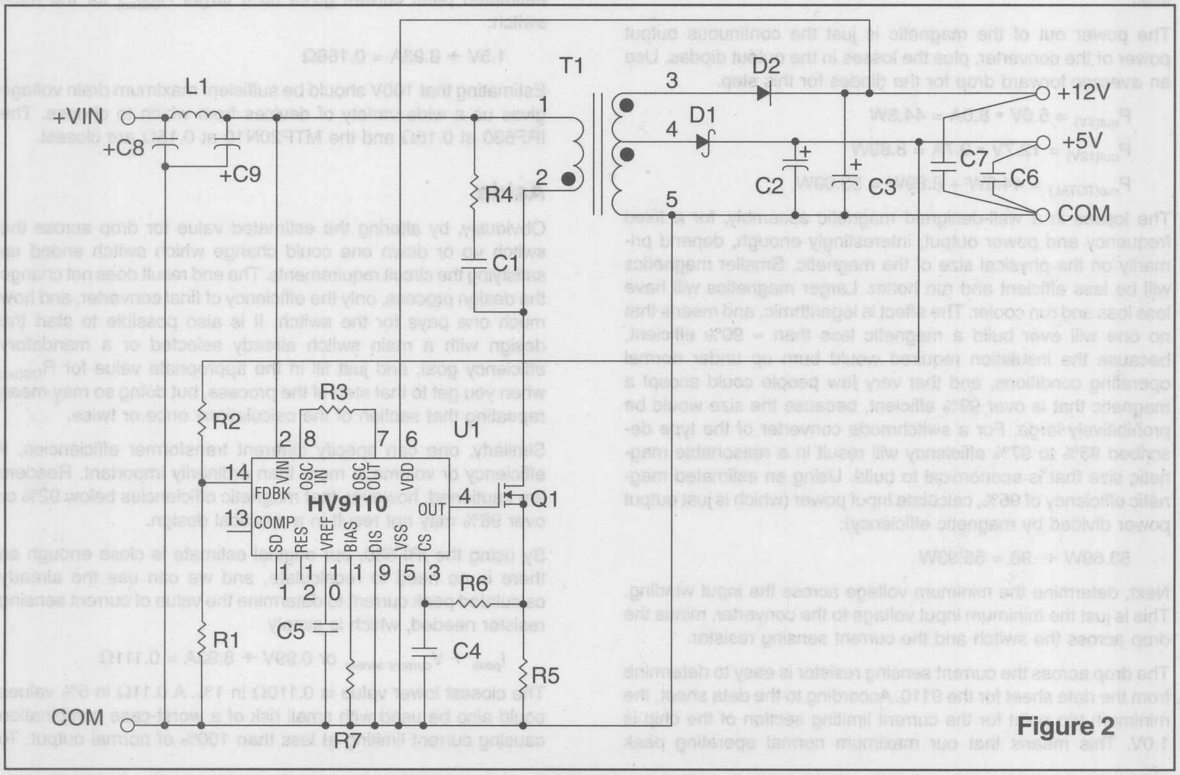


Figure 2

This value will also be used to determine the actual voltage required of the winding, which is the output voltage plus the drop in the output diode:

$$V_{winding} = V_{output} + V_{F(diode)}$$

Also, repeat this procedure for each auxiliary output winding as an aid in determining the real voltage required of these windings:

$$I_{pk(12V)} = 0.7A \div \sqrt{\frac{.50}{3}} = 1.715A$$

Next calculate minimum t_{off}, which will be 50% of the maximum PWM oscillator frequency. Using a 261K timing resistor, maximum frequency should be ≤ 67KHz, which gives a t_{period} of ≥14.9 µsec, and a $t_{off(min)}$ of 7.46 µsec.

Next, we need to generate an *estimate* of instantaneous forward drop of the diode on the main output. We cannot actually choose a diode until we know what its reverse voltage needs to be, which will not be known until input side inductance is calculated. 0.8V should be a reasonable estimate. This voltage is added to the 5V output voltage to determine the actual voltage on the main output winding (5.8V in this instance).

Knowing the peak current and voltage of the output winding and the minimum t_{off}, we can calculate the inductance of the output winding from the defining equation for inductance, E = L dI/dt.

$$5.8V \div \left(\frac{19.6A}{7.46 \times 10^{-6\,sec}}\right) = 2.21\mu H$$

The same procedure is used to calculate primary inductance. First we need to calculate the total power into the magnetic. This is the power out of the magnetic, plus the losses in the magnetic itself.

The power out of the magnetic is just the continuous output power of the converter, plus the losses in the output diodes. Use an *average* forward drop for the diodes for this step.

$$P_{out(5V)} = 5.6V \bullet 8.0A = 44.8W$$

$$P_{out(12V)} = 12.7V \bullet 0.7A = 8.89W$$

$$P_{out(TOTAL)} = 44.8W + 8.89W = 53.69W$$

The losses in a well-designed magnetic assembly, for a fixed frequency and power output, interestingly enough, depend primarily on the physical size of the magnetic. Smaller magnetics will be less efficient and run hotter. Larger magnetics will have less loss and run cooler. The effect is logarithmic, and means that no one will ever build a magnetic less than ≈ 90% efficient, because the insulation required would burn up under normal operating conditions, and that very few people could accept a magnetic that is over 99% efficient, because the size would be prohibitively large. For a switchmode converter of the type described 95% to 97% efficiency will result in a reasonable magnetic size that is economical to build. Using an estimated magnetic efficiency of 96%, calculate input power (which is just output power divided by magnetic efficiency):

$$53.69W \div .96 = 55.93W$$

Next, determine the minimum voltage across the input winding. This is just the minimum input voltage to the converter, minus the drop across the switch and the current sensing resistor.

The drop across the current sensing resistor is easy to determine from the data sheet for the 9110. According to the data sheet, the minimum trip point for the current limiting section of the chip is 1.0V. This means that our maximum normal operating peak voltage across the resistor should be slightly below 1.0V. If we establish a maximum peak voltage that is much less than 1V, we will increase the distance between maximum normal operating current and the maximum guaranteed overcurrent trip point, which is 1.4V. Usually the best choice is to operate with a normal peak voltage across the current sense resistor very close to 1V, so 0.99V is a reasonable value. Note that this voltage drop across the current sensing resistor only occurs during current limit. In normal operation at loads below maximum, the trip point for the switch moves down to limit the energy going to the output. That is how this form of converter regulates.

The drop across the switch is more complicated, because first we have to choose a main switch. To do this we need an estimate of what the current will be. Generally a close enough estimate can be made using the wattage into the magnetic and an estimated minimum voltage across the winding. If we assume that the voltage across the switch will be no greater than 1.5V peak, we can subtract this voltage, and the current sense voltage, from the minimum input voltage and estimate DC input current:

$$18V - (1.5V + 1V) = 15.5V$$

Dividing the previously determined input wattage to the inductor produces a DC input current:

$$55.93W \div 15.5V = 3.61A$$

Dividing that by the DC to peak conversion factor (based on t_{ON} = 49%) gives us an estimated peak current.

$$3.61 \div \sqrt{\frac{.49}{3}} = 8.93A$$

Dividing the previously assumed drop across the switch by the estimated peak current gives us a target $R_{DS(on)}$ for the main switch:

$$1.5V \div 8.93A = 0.168\Omega$$

Estimating that 100V should be sufficient maximum drain voltage gives us a wide variety of devices from which to choose. The IRF530 at 0.16Ω and the MTP20N10 at 0.15Ω are closest.

Aside

Obviously, by altering the estimated value for drop across the switch up or down one could change which switch ended up satisfying the circuit requirements. The end result does not change the design process, only the efficiency of final converter, and how much one pays for the switch. It is also possible to start the design with a main switch already selected or a mandatory efficiency goal, and just fill in the appropriate value for $R_{DS(on)}$ when you get to that step of the process, but doing so may mean repeating that section of the calculations once or twice.

Similarly, one can specify different transformer efficiencies, if efficiency or volume is more than ordinarily important. Readers are cautioned, however, that magnetic efficiencies below 92% or over 98% may not result in a practical design.

By using the IRF530, our original estimate is close enough so there is no need to recalculate, and we can use the already calculated peak current to determine the value of current sensing resistor needed, which is simply

$$I_{peak} \div V_{current\ sense},\ \text{or}\ 0.99V \div 8.93A = 0.111\Omega$$

The closest lower value is 0.110Ω in 1%. A 0.11Ω in 5% values could also be used with small risk of a worst-case combination causing current limiting at less than 100% of normal output. To

determine wattage we can use the DC input current:

$3.61A^2 \bullet 0.11\Omega = 1.43W$

so a 1.5W or 2W resistor would work.

A Word on Current Sense Resistors

Obtaining a good current sensing resistor is still a problem. Most common resistors are not fit for this service because they are too inductive. What answer there is probably lies in bulk metal resistors, or noninductive resistors, but be careful. Some "noninductive" resistors are only "noninductive" at low frequencies, and can be the source of considerable error at high frequencies. Carbon film resistors and most metal film resistors are not recommended. Also, most of the low value resistors that look like carbon composition resistors are actually film or wirewound resistors in molded cases. 4-terminal resistors specifically meant for current sensing are for the most part wirewound, and meant only for DC, not switched current measurements. Be sure to test the inductance of the resistor you intend to use before you install it in your circuit! Also, even a good noninductive resistor will not work properly if long leads or long printed circuit board traces are allowed to add inductance to the mechanical assembly. Good PCB layout practice is mandatory.

The Design (continued)

We can also use the same procedure ($I^2 \bullet R$) to determine the approximate power loss in the main switch. This is not the absolute loss, which will be a little higher due to the rise in $R_{DS(on)}$ with temperature in the MOSFET, but generally it will be close enough to start determination of heatsinking requirements.

$3.61A^2 \bullet 0.16\Omega = 2.085W$

Note that because the DC input current is equivalent in this instance to the RMS current through the switch (or the current sense resistor), one does not need to account for duty cycle or time effects.

Next, we need to determine the inductance required of the input winding. Now that we know the voltage across the winding and the peak current through the winding, all we need do is calculate the minimum t_{on} and repeat the same procedure as for the output:

$$t_{ON} = .49 \bullet 14.92\mu sec = 7.31\mu sec$$

$$\text{then } L = 15.5V \div \left(\frac{8.93A}{7.31\mu sec}\right) = 12.7\mu H$$

Now that we have the inductances of the output and input windings we can determine the voltage stresses applies to the switch and diodes, and make a final determination of the appropriate devices. The trick here is that the inductance varies as the square of the number of turns, so the turns ratio varies as the square root of the ratio of the inductances.

$$\text{turns ratio} = \sqrt{\frac{12.7}{2.21}} = 2.40 :1 \text{ or } 1: .417$$

Thus, when there is 65V present on the input winding, there will be 65V • .417 = 27.1V on the 5V output winding. Adding to this the +5V that will be present on the cathode end of the diode from the output gives 32.1V, and means that a 45V diode allows a 40% margin for noise spikes and should work well. Two good choices are the Motorola #MBR1045 and the #MBR1645, the difference between them being that the larger one would be a bit more efficient.

Similarly, when the main switch is OFF, in addition to the 65V present from the input, there will be

$5.8V \bullet 2.40 = 13.9V$

reflected from the output, for a total of 78.9V present on the drain of the main switch. This leaves a 26% margin for spikes. A 100V FET should work.

A similar procedure based on turns ratio finds the voltage present on the diode on the 12V output. This output is ratiometrically linked to the 5V winding with its own turns ratio of 12.8 : 5.8, or 2.20:1, so when there is 27.1V reflected from the input winding there will be 27.1V • 2.2 = 59.6V, plus 12V from the output, for a total of 71.6V across the 12V diode. A 100V, 1A ultra high speed silicon diode, like a Motorola #MUR105 is a reasonable choice. Note that in the case of multiple outputs which conduct at the same time, the flyback magnetic *does* act like a transformer, but this is the *only* case in which it does.

Next, we can complete the definition of the magnetic assembly. The inductances of the input and output side are known. What remains is to define the resistances of the windings. These can be calculated from the rule that for an optimum size/efficiency magnetic, 50% of the loss occurs as resistive loss in the windings, and this loss is balanced among the windings based on the percentage of total power handled by each (the other 50% of the loss occurs in the core as hysteresis loss). Output power, as previously calculated, is 53.69W. Input power was calculated to be 55.93W. Thus power loss in the magnetic is

$55.93W - 53.69W = 2.24W.$

The copper loss should be close to 1.12W. Half of this, .56W, occurs in the input winding, which must supply all the outputs. The other half is split between the 5V and 12V windings in the ratio of their respective powers. For the 5V winding this is:

$$\left(\frac{44.8}{53.7}\right) \bullet .56 = .467W$$

For the 12V winding it is:

$$\left(\frac{8.89}{53.7}\right) \bullet .56 = .093W$$

Knowing a target wattage and DC current for each winding (in this case DC = RMS) we can calculate resistances from $I^2 \bullet R$.

input: $.56W \div (3.61A)^2 = .043\Omega$

5V output: $.467W \div (8A)^2 = .0073\Omega$

12V output: $.093W \div (0.7A)^2 = 0.190\Omega$

This completes the definition of the magnetic assembly.

Actually, because it is difficult to balance power loss between windings, or between windings and core, easing the calculated values up somewhat (as much as 20%) may result in a magnetic that would be significantly smaller with no increase in total losses. This should be discussed with your magnetics vendor. Also, because modern high-performance ferrites tend to have very low losses at moderate frequencies like 50 to 100KHz, you may wish to divide the total power loss differently, say 40% core, 60% copper. This can also reduce the cost of the inductor without increasing its size. This probably will *not* work if the clock frequency of the converter is 200KHz or more.

Leakage Inductance

The final thing you need to specify with regard to the magnetic is a maximum leakage inductance. Leakage inductance is a measure of the amount of flux generated by one winding in a magnetic assembly that is not coupled to the other winding(s) by the core and winding structure. For a flyback converter it is a measure of how much of the energy taken into the input winding is incapable of being transferred to the output winding when the switch turns OFF. This energy appears as a voltage spike on the drain of the MOSFET each time it turns off and must be dissipated either by the MOSFET directly, or in a snubber circuit. A reasonable value for leakage inductance is 1% to 2% of nominal inductance, but this is highly variable and depends on the intended operating frequency, size, and efficiency of the magnetic being developed. An actual maximum value should be discussed with your magnetics vendor before it is cast in concrete, and that maximum value should be used later for the development of a snubber, if a snubber appears to be worthwhile. *(See Figure 3.)*

Next, we select the output capacitors. Two criteria need to be met. First, the minimum capacitance must satisfy the standard capacitance definition $I = C\ dV/dt$ where I is in Amperes, C in Farads, delta $t = t_{ON}$ and delta $V \approx 25\%$ of the allowable output ripple. Second, and almost inevitably harder, the Equivalent Series Resistance (ESR) of the capacitor(s) must provide no more than the part of the ripple (75% in this case) not provided from the first criteria, in accordance with

$$E_{ripple} = I_{peak} \bullet ESR$$

where I_{peak} is the peak current from the output inductance during discharge. (This is because when the main switch turns OFF, the current in the filter capacitor switches, effectively instantaneously, from an outbound current I_{out}, to an inbound current, $(I_{peak} - I_{out})$. The reason for splitting the allowable ripple between the two criteria is that in the final converter they will tend to add. The reason for the asymmetrical split of the allowable ripple is that the ESR-caused ripple limit is the more difficult criteria to meet. In some instances a more drastic partitioning (5 or more to 1 in favor of the ESR ripple) may be better.

For the 5V output these criteria calculate out as follows:

$$C = 8A \div ((.25 \bullet .025V)/10\mu sec) = 12{,}800\mu F$$

and

$$ESR = (.75 \bullet .025V) \div 19.59A = 957\mu\Omega$$

Based on Mallory type THF capacitor (330µF, 6 WVDC, ESR ≤ 0.04Ω) (a typical good output filter capacitor). This works out to 42 pieces in parallel to satisfy ripple from an ESR standpoint, and 39 pieces to satisfy ripple from a capacitance standpoint. Close enough. Note that the capacitor chosen is a tantalum capacitor, If you wish to use aluminum capacitors to perform the same service you can ignore ripple from capacitive droop and assign 100% of the ripple to ESR. Sizing an aluminum capacitor strictly from ESR will generally provide one with 40 to 100 times more capacitance than is needed. This will slow down the transient response of the converter, but it means that you will rarely, if ever, encounter stability problems.

Aside

Based on the price of Mallory THFs, the stated stolution may not be an optimum solution to the problem. A better solution might be to change the effective ripple specification from ≤0.025V to ≤0.250V and add an additional stage of LC filtering from the nominal output to the "real" output seen by the load. This means that instead of 42 capacitors we can use 4, but these must be followed by an LC filter with 10:1 attenuation (20dB) at 50KHz. This implies a corner frequency, f_C, of 5KHz, which means it won't be a small filter, but there is no necessity of using a high performance capacitor on this second filter stage. The other difficulty with a second-stage filter is that the DC resistance of the inductor is not cancelled by the feedback loop, and consequently the variation in output voltage with load current can exceed the specifications for the power supply. To hold the ± 1% regulation specification on the 5V line we would need an inductor with ≈ .003Ω resistance.

A second alternative would be to use a combination of electrolytic and film capacitors in parallel with the electrolytics sized solely to the load current ripple criterion and the film capacitors sized solely to the ESR ripple criterion. In this instance, ESR and capacitive droop should divide the ripple about 50-50. *(See Figure 4.)*

Next we define the filter capacitors for the 12V output in the same way:

$$C \geq 0.7A \div \left(\frac{.25 \bullet .5V}{10\mu sec}\right), \text{ therefore } C \geq 56\mu F$$

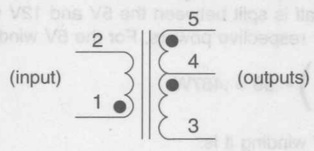
$$ESR \leq (.75 \bullet .5) \div 1.715A, \text{ therefore } ESR \leq 0.219\Omega$$

This is a much easier capacitor to find. A Sprague type 676, 900µF 12WVDC, aluminum electrolytic (the smallest 12V capacitor in this series) will work well. A 56µF, 15V, Mallory type THF will also work.

Next we define the divider resistors which will be used to feed back a sample of the 5V output to the error amplifier in the PWM.

Coupled Inductor Specification

(Preliminary)



Schematic

Nominal Operating Frequency: 50 to 60 KHz

WDG 1–2: L = 12.7µH ± 5% with 8.9 A DC Flowing
DCR ≤ 0.045 Ohm
Leakage Inductance 1–2 with 3–4 shorted: ≤ 200nH

WDG 3–4: L = 2.2µH ± 5% with 19.6 A DC Flowing
DCR ≤ 0.0075 Ohm

WDG 3–5: Voltage ratio of 3–5 to 3–4 12.8: 5.8 ± 2%
DCR ≤ 0.19 Ohm

Polarization: Starts must be as shown on schematic (pins 1, 4, 5)

Insulation: Vacuum impregnate in class A thermosetting varnish

Interwinding Insulation: Not applicable

Expected Thermal Rise: <45°C in 40°C ambient

Mounting: Through-hole PCB

Figure 3

Output Filters for Equivalent Ripple

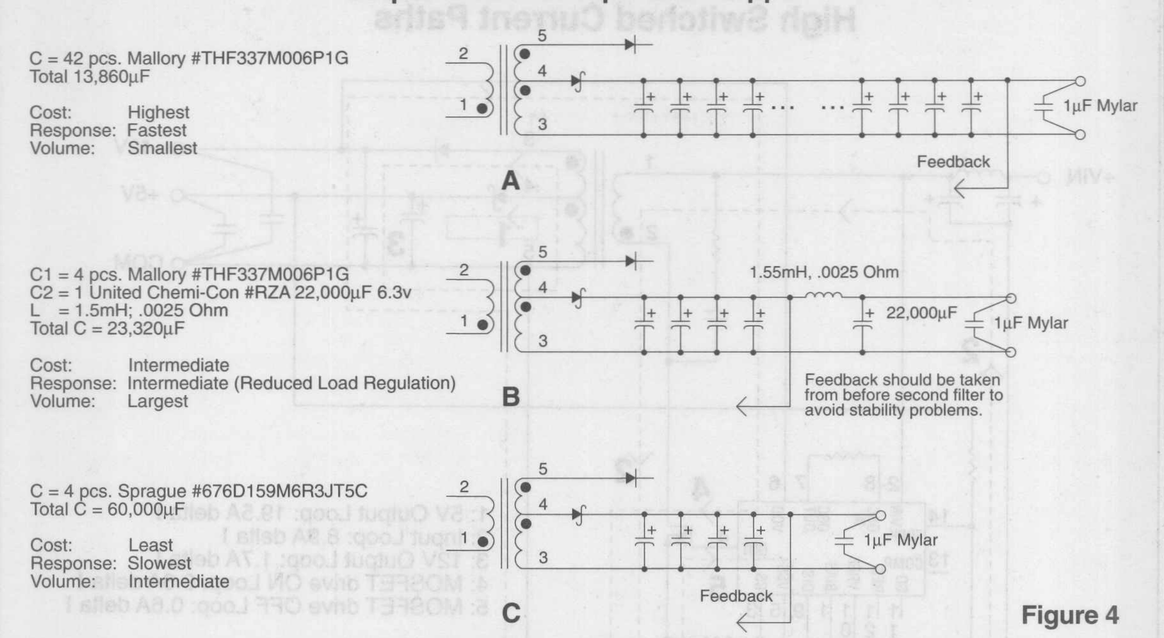


Figure 4

Because the error amp in the HV9110 is CMOS, its input bias current is negligible, and the divider string can carry a very small current; 100µA is plenty. The feedback terminal of the HV9110 (the inverting terminal of the error amplifier) is satisfied by 4.00V ±1%. If we use a 100µA divider, the lower resistor should be

4.00V ÷ .0001A = 40kΩ

The closest real value is 40.2KΩ. To produce exactly 4.00V with 40.2KΩ we need an actual divider string current of

4.00V ÷ 40200Ω = 99.50µA

Dividing the 1V remaining between 4V and our intended output of 5V by our actual divider string current, gives a value of

1.00 ÷ .00009950 = 10,050Ω

The closest value is 10.0K.

Normally, the next and final step in the design process would be stability analysis. However, it turns out that one of the advantages of discontinuous-mode, current-mode flyback converters with a maximum duty cycle of < 50%, with output capacitors (especially if they are aluminum electrolytics) sized to ripple requirements, is that they are usually stable "as is." As a matter of prudence, checking the loop response of a new power supply on a network analyzer or Venable machine is always a good idea, but for supplies of this nature this writer no longer considers full analysis mandatory. For this reason, and because including stability analysis in this application note would probably double its length, analysis is omitted. For those desirous of performing a full mathematical analysis of every loop, the following texts[5] on the subject are recommended:

DC to DC Switching Regulator Analysis
Dan Mitchell, McGraw-Hill, ISBN 0-07-042597-3

Switch Mode Power Conversion
K. Kit Sum, Marcel Dekker, ISBN 0-8247-7234-2

Modeling, Analysis and Design of PWM Converters, vol. 2
VPEC staff, VPEC[2], ISBN (none)[3]

Advances in Switched-Mode Power Conversion, vol. I and II
R. D. Middlebrook and S. Cúk, Teslaco, ISBN (none)[4]

Dynamic Analysis of Switching-Mode DC to DC Converters
Nathan Sokal, Andre Kislovski, and Richard Redl, Van Nostrand Reinhold, ISBN 0-442-21396-4

Modern DC to DC Switchmode Power Converter Circuits
R. Severns and G.E. Bloom, Van Nostrand Reinhold, ISBN 0-442-21396-4

Accessory Circuits

1. The snubber circuit for the MOSFET drain switching spike should be sized to absorb the energy taken into the magnetic that is not coupled to the output. The available energy is 1/2 L • I^2 where L is the leakage inductance of the primary and I is the peak input side current. Using a reasonable estimate of 2% for leakage inductance gives a value of 250nH. Spike energy then is:

1/2 (250nH • 8.93A^2) = 10.1µJ

Multiplying this by the maximum repetitions per second (which occurs at maximum frequency) gives

10.1µJ • 67,000Hz = .679W,

which is the amount of power to be dissipated either in the MOSFET or the snubber.

To dissipate it in the snubber it must be captured in the snubber capacitor without exceeding the drain breakdown of the FET.

Minimum FET breakdown: 100V

Maximum circuit-supplied voltage on FET drain: 78.9V

Maximum voltage for snubber cap: 21.1V

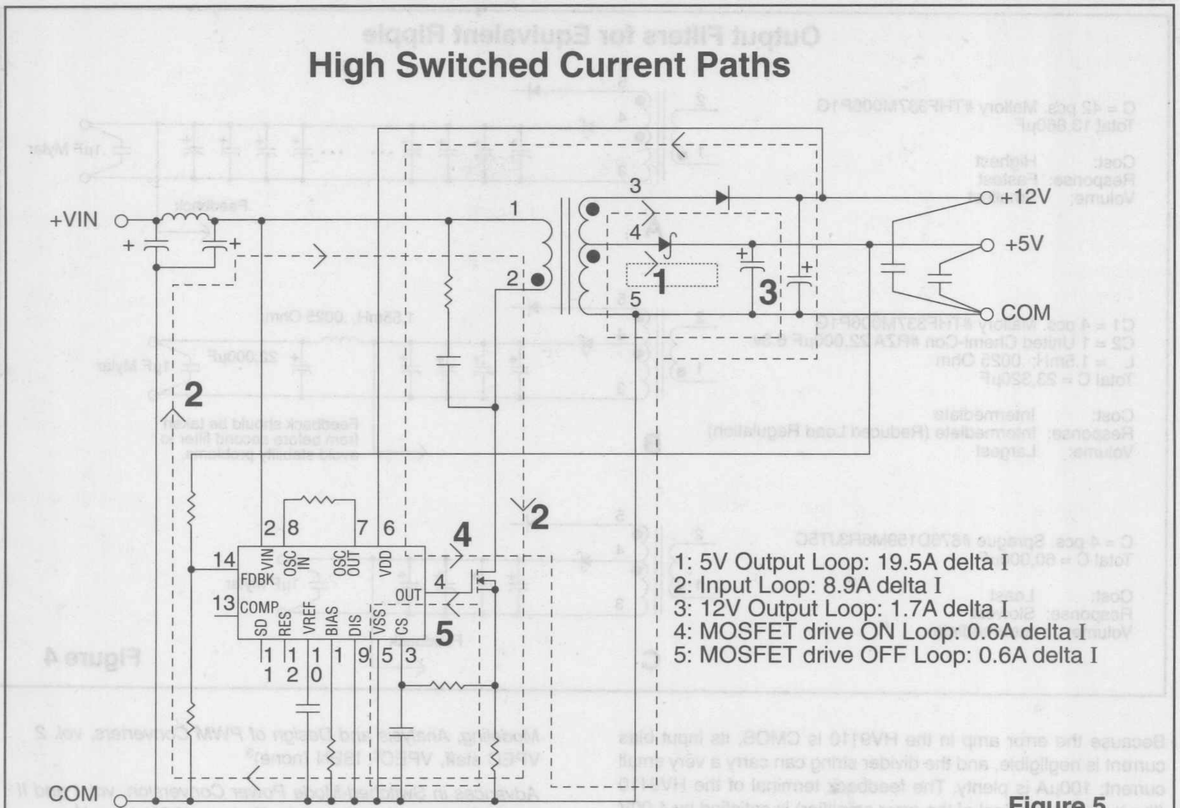


Figure 5

To calculate the size of the snubber capacitor we convert the 1/2 L • I² energy previously calculated to 1/2 C • V² energy, and divide by the maximum voltage we desire on the capacitor:

$$(2 \bullet 10.1\mu J) \div 21.1V^2 = 0.045\mu F$$

Using the next larger real capacitor (.047 in this case) assures us that the voltage spike will not be large enough to break down the MOSFET. The resistor in series with the snubber capacitor must have a low enough value to allow the capacitor to discharge in the minimum on-time of the switch, which for a HV9110 will be about 200nsec. Because the discharge distance (62.5V max) is much greater than the charge distance (21.1V) declaring 400nsec = RC will work. Thus

$$400nsec \div 47nF = 8.51\Omega$$

The catch here is that, except when the switch is on for the minimum time, the capacitor will reverse charge to

$$V_{IN} - (V_{FET} + V_{current\ sense})\text{ or }62.5V.$$

It is this energy which must be dissipated in the resistor:

$$1/2\ (62.5V^2 \bullet 47nF) \bullet 67KHz = 6.15W$$

So a 10W resistor will be necessary. To save 679mW in the FET, this hardly seems worthwhile, but it can be done if desired.

2. If a snubber is used, an RC filter network should be added between the current sense resistor and the current sense terminal of the HV9110 to prevent the higher-than-usual leading edge spike on the current waveform from shutting the switch off prematurely. The RC time constant of this filter should be approximately 20% of the snubber time constant, but never more than ≈100 nsec. (Otherwise authentic fault current spikes may be slowed down too much.) The R for the current spike filter can be a lot larger, and the C much smaller, because the load presented by the HV9110 is quite small (on the order of 3pF). Using a 1KΩ resistor and a 75pF capacitor should be sufficient for the snubber above.

3. Two small capacitors are shown in Fig. 2, connected directly at the converter outputs. These are 1µF stacked film capacitors with very good AC characteristics, intended for general noise suppression. They may not be necessary, but they are reasonable insurance.

4. An Input EMI filter will also be required under most circumstances. For conducted emissions, generally an asymmetrical pi-type filter is sufficient. The converter-side capacitor should be sized to convert the delta I caused by switching to a reasonably low delta voltage over t_{off}. The inductor and input side capacitor should be designed to have a corner frequency that complements the corner frequency of the regulator loop, to minimize susceptibility to outside noise coming in to the regulator.

In this case, from previous calculations, input switching current is known to be a maximum of 8.9A. Similarly, minimum t_{off} is 7.46µsec, and a reasonably low value for delta V is 250mV. Thus, from I = C dV/dt, the converter side capacitor calculates out to:

$$8.9A \div (.25V \div 7.6 \times 10^{-6}\text{ sec}) = 271\mu F$$

A good choice is 330µF. This capacitor can also serve to insure a minimum holdup time for short input dropouts.

The values of the inductor and the input side capacitor can be calculated from

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

once the corner frequency of the regulator loop is known. In this case the regulator loop is rather slow, due to the large output capacitors required by the ripple specifications, and an appropriate frequency to use is only 750Hz. This gives us a $\sqrt{LC} = 212 \times 10^{-6}$. This means that any combination of inductor and capacitor values whose product is 4.5×10^{-8} will provide an adequate filter. Generally, it is best to use a larger value of capacitor and a smaller value of inductor because inductors usually cost more. In this case using a 1000µF capacitor results in a 45µH inductor, 47 or 50µH is easily obtainable, small and inexpensive. The DCR should be low enough so that our previous calculations based on V_{IN} remain valid. Based on 3.6A maximum DC input current, a 0.5Ω DCR will give a 0.14V drop, which is well within allowable safety margins, and results in a cheap, small inductor.

On Layout and Noise (Radiated EMI)

Anyone using the HV9100, HV9110, or other parts in the same family, will end up switching current flow on and off. Sometimes, quite large currents are switched in short periods of time. In the current example, the dI/dt on the 5V secondary will be over 300 amps per microsecond! This is sufficient to cause significant radiated EMI if it is improperly handled.

Controlling EMI from a switchmode converter is neither difficult nor costly, provided attention is paid to the subject early enough in the design cycle.

There are no "tricks" to EMI control, only one basic rule: *Minimize the area of the loops around which switched currents circulate.* This is purely a mechanical constraint, and should be dealt with during PCB layout. Generally, unless you have a PCB layout person with prior experience with switching converters, the circuit designer will have to lead the board designer through the first few layouts, and even thereafter, will have to show the board designer where the switched current loops are in the circuit. *(See Figure 5.)*

Obviously, there are other constraints to a switchmode converter PCB as well, and these also affect system performance. Most converters should be laid out single-sided, with the second side of the PCB reserved for a ground plane. Also, high currents require wide lands, just to keep DC resistances low. First and foremost though, should be the effort to keep switched current loop area minimized. Loop length is also important, as long runs can have enough inductance to disrupt circuit operation. On the 9110/9120 this is only likely around the gate drive loops, which have relatively low delta I's, and the current sense resistor, where stray inductance can cause the overcurrent sensing to shut the main switch off prematurely, thereby limiting power output.

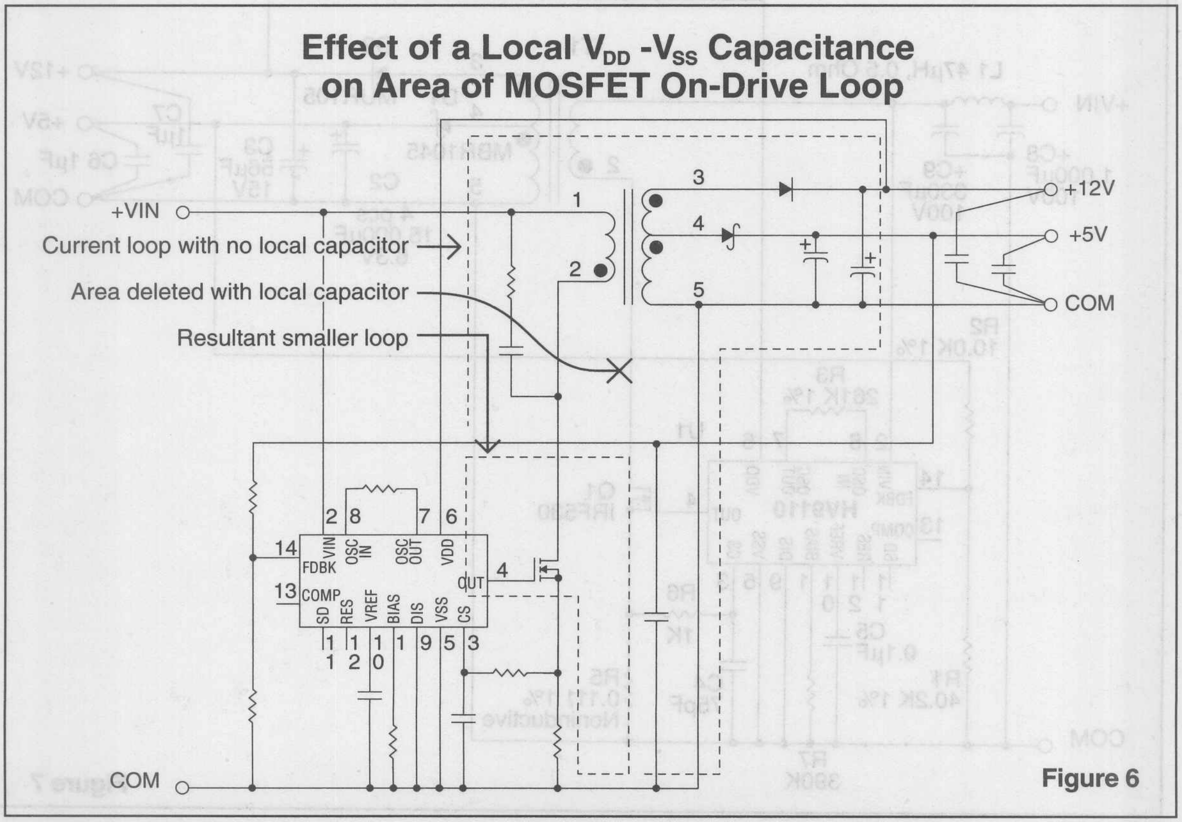


Figure 6

Board layout should proceed by taking the switched current loops in order of delta I, and laying the DC portions of the circuit out last. Using the first circuit as an example, this means starting with the 5V loop, (which includes only the coupled inductor, 5V diode, and output capacitors) taking the input loop next (coupled inductor, power MOSFET, current sense resistor, and input filter cap) and following those with the 12V output loop, and the MOSFET drive loops. In each instance, it is the *entire* loop that matters, *including the return path.* Assuming that the return path is good, even on boards with ground planes, is risky. Look at each loop carefully to see that its area is minimized. After the switched current loops are laid out, the DC sections can be fitted where they are convenient. They do not contribute noise, but they can convey it if it is generated elsewhere. The feedback loop is a special case. By itself, this is a DC loop, but it is susceptible to noise generated on other loops, and because it is, for the most part, a high-impedance path, not much energy is required to disrupt it. The feedback loop should also be laid out for minimum area, but it is more important that the path of its circuitry lies well away from, and where possible perpendicular to, the switched current loops. Generally, layout grows outward from the transformer, and careful choosing of which pins on the transformer connect to which windings can do a lot to make layout convenient.

There are a few things that can be done in designs with the HV91XX family that may make a specific layout more convenient: First, it should be remembered that the high current paths associated with the current sense resistor do not include the line from the junction of the resistor and the MOSFET to the current sense terminal of the IC. The sense lead to the IC is a very low current path, and can be comparatively long providing that the path from MOSFET to resistor to ground is short. The output lead from HV9110s and HV9120s however should be kept short, because it services both the charge and discharge paths from the MOSFET gate. Also, when a 10V or 12V winding on the transformer is used to power the HV91XX, it may help to split the filter capacitor into two pieces, one near the transformer and diode (to keep that current loop short) and a second near the HV91XX to keep the ON-drive current loop short. The V_{DD} and V_{SS} terminals of the HV91XX are adjacent to each other specifically to allow this. *(See Figure 6.)*

Inevitably, there will be some residual radiated EMI, and some of this will be picked up by the DC circuits and seen on the input and outputs as conducted EMI. The 1µF film capacitor previously noted should suffice to remove this from the outputs, and a small commercial line filter should suffice for the input. Most commercial EMI filter suppliers offer EMI lab services (sometimes free!) to assure that the end converter + filter meets whatever requirements are in force for your particular circumstances. Using these services as a final check is generally worthwhile.

There is only one additional noise control measure necessary. The reference pin of the HV91XX is a high impedance node, and is designed to work with a 0.01µF to 0.1µF capacitor between

The Final Design

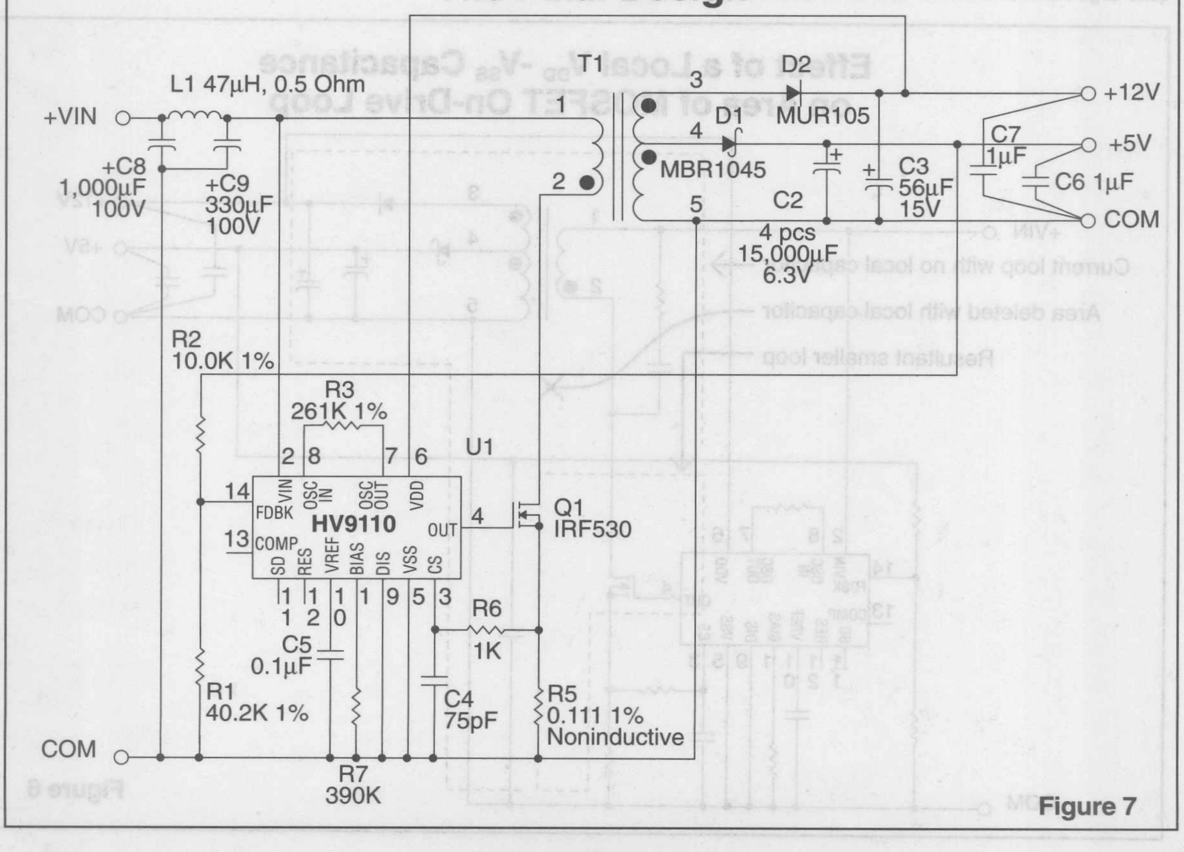


Figure 7

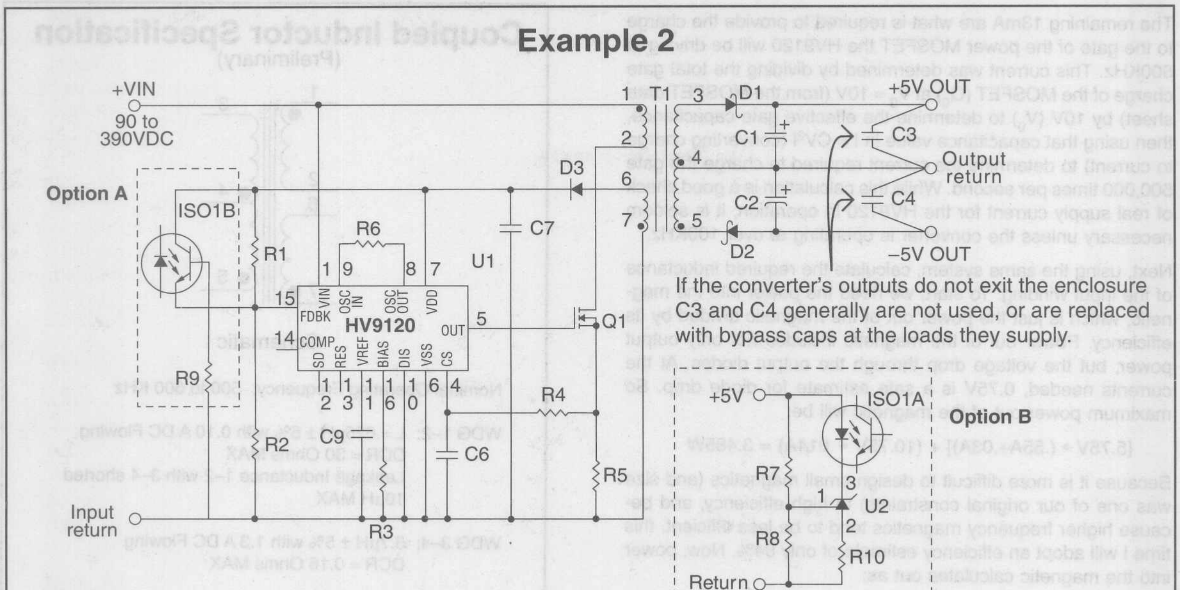


Figure 8

itself and V_{SS}. This capacitor should not be omitted. On the other hand, a capacitor between the bias pin and V_{SS} should not be required. If a capacitor from the bias pin to V_{SS} improves operation, the capacitor should be placed from V_{DD} to V_{SS}. As usual for any switching circuit, all noise filtration capacitors should be types with good high frequency performance: Stacked Mylar and ceramic multi-layer caps generally are best. *(See Figure 7.)*

Example 2

A 3W converter for a DPM. Size is to be as small as is consistent with low cost, input range is 65VAC to 240VAC, load is fairly constant.

As before, the first thing we need is specifications to design to:

Maximum Input Voltage: 390VDC {[(240 + 15%) • $\sqrt{2}$]-1.4}

Minimum Input Voltage: 90VDC [(65 • $\sqrt{2}$)-1.4]

Outputs: A: +5V ± 5%, 0.4 to 0.55A, ≤ 100mV ripple
B: -5V ± 5%, 30mA, ≤ 100 mV ripple
C: +10V ± 10%, 14mA, ≤ 100mV ripple

Maximum Output Wattage: 3.04W

Minimum Output Wattage: 2.29W

Operating Frequency: 500KHz (min)

An HV9120, which accepts input voltages up to 450VDC will be required. This time, even with the high operating frequency, sufficient dynamic range exists (13.2:1) so that the end supply should not exhibit cycle skipping. This minimizes the size of output filters. *(See Figure 8.)*

The Design

First, select a timing resistor. To assure that all units operate at 500KHz or above despite tolerance effects, a 16.5KΩ resistor should be sufficient. But, because parasitic capacitances associated with the PCB layout can have a serious effect on clock oscillator performance at high frequencies (the timing capacitance in the 9120 totals less than 10pF), the value of the timing resistor should be confirmed in the final assembly to assure desired performance.

Next, calculate minimum t_{off} and t_{on}. If minimum frequency is 500KHz, worst case maximum can be up to 600KHz, and at 600KHz, maximum duty cycle will be no greater than 46.5%. Thus, minimum t_{on} will be:

1667 nsec • .465 = 775 nsec

and minimum t_{off} will be:

1667 − 775 = 892 nsec

or 53.5% of total period. For peak current calculations (to follow) it will be sufficient to declare D (duty cycle) = 46.5%, and 1-D = 51.5%, leaving a 2% deadband to assure discontinuous-mode operation.

Next, translate the DC current of the output with the greatest percentage of the load (+5V this time) to a peak current using the same formula as in the previous example:

$$.55\text{A} \div \sqrt{\frac{.515}{3}} = 1.328\text{A } I_{peak}$$

This allows us to calculate the inductance of the secondary using E = L dI/dt. Remember that the voltage seen by the inductor includes the forward drop of the output diode, so the actual calculation works out to:

5.75V ÷ (1.328A ÷ 858nsec) = 3.72µH

The -5V winding will be equal in turns (thus also in voltage and inductance) to the +5V winding. The 10V winding, (which powers the HV9120) conducts at the same time as the main +5V winding, and thus has a turns ratio equal to its voltage ratio, (10.7 : 5.7) and no inductance calculation for it is necessary.

SIDE NOTE: The load stated above for the 10V winding (14mA) is considerably larger than the 1mA specification for the HV9120.

The remaining 13mA are what is required to provide the charge to the gate of the power MOSFET the HV9120 will be driving at 500KHz. This current was determined by dividing the total gate charge of the MOSFET (Q_g) at V_g = 10V (from the MOSFET data sheet) by 10V (V_g) to determine the effective gate capacitance, then using that capacitance value in $I = CV^2f$ (converting charge to current) to determine the current required to charge the gate 500,000 times per second. While this calculation is a good check of real supply current for the HV9120 in operation, it is seldom necessary unless the converter is operating at over 100KHz.

Next, using the same system, calculate the required inductance of the input winding. To start, we need the power into the magnetic, which is just the power out of the magnetic divided by its efficiency. Power out of the magnetic includes not only output power, but the voltage drop through the output diodes. At the currents needed, 0.75V is a safe estimate for diode drop. So maximum power out of the magnetic will be:

$$[5.75V \bullet (.55A + .03A)] + (10.75V \bullet .014A) = 3.485W$$

Because it is more difficult to design small magnetics (and size was one of our original constraints) to high efficiency, and because higher frequency magnetics tend to be less efficient, this time I will adopt an efficiency estimate of only 94%. Now, power into the magnetic calculates out as:

$$3.485W \div 0.94 = 3.707W$$

To obtain a DC input current, this wattage is divided by the minimum DC voltage across the input winding, which is just the minimum DC input voltage less the drop in the current sensing resistor and the power MOSFET. The maximum drop across the current sensing resistor again should be set to just under 1.0V (from the HV9120 spec.) and a reasonable estimate for drop in the MOSFET is 2.1V, (based on the use of a Supertex #VN0660N3, 600V, 20Ω MOSFET). So minimum input side voltage will be:

$$90 - (1 + 2.1) = 86.9V$$

and DC input current will be:

$$3.707W \div 86.9V = 42.7mA$$

Knowing DC input current and duty cycle we can now calculate peak input current, which will be:

$$0.0427A \div \sqrt{\frac{.465}{3}} = 0.108A$$

Knowing peak input current, minimum input voltage and smallest maximum t_{on}, we can now calculate input side inductance from $E = L\,dI/dt$. This works out to:

$$86.9V \div \left(\frac{.108A}{775nsec}\right) = 624\mu H$$

Next, we need to determine the DC resistances of the various windings of the magnetic. In this case, because of the operating frequency, copper losses and core losses probably *will* be approximately equal. Again, power loss in the magnetic is just $P_{in} - P_{out}$ or 222mW. Assuming half of this is copper loss gives a copper loss of 111mW. This should be divided among the various windings in proportion to their proportion of the total wattage.

Input winding: 50%, or 55.5 mW

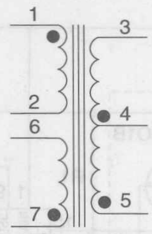
+5V output: 45.4% or 50.4 mW

–5V output: 2.5% or 2.75 mW

+10V output: 2.2% or 2.40 mW

Coupled Inductor Specification

(Preliminary)



Schematic

Nominal Operating Frequency: 500 to 600 KHz

WDG 1–2: L = 625μH ± 5% with 0.10 A DC Flowing
DCR = 30 Ohms MAX
Leakage Inductance 1–2 with 3–4 shorted
10μH MAX

WDG 3–4: 3.7μH ± 5% with 1.3 A DC Flowing
DCR = 0.16 Ohms MAX

WDG 5–4: Voltage ratio WDG 5–4 to WDG 3–4
1.00 : 1.00 ± 2%
DCR = 3.0 Ohms MAX

WDG 6–7: Voltage ratio WDG 6–7 to WDG 3–4
10.7 : 5.7 ± 2%
DCR = 12.5 Ohms MAX

Polarization: Starts must be as shown on schematic (pins 1, 4, 5, 7)

Insulation: Vacuum impregnate with class H thermosetting varnish

Interwinding Insulation: WDG 3–4–5 to WDG 1–2 and 6–7 min 1.5KVAC
WDG 1–2 to WDG 6–7 min 500VAC

Expected Thermal Rise: <60°C in 50°C ambient

Mounting: Through-hole PCB

Figure 9

Actually, this shortchanges the input winding somewhat, as it carries slightly more power than all outputs combined, but this is usually trivial. As before, DC current (NOT peak) is used to determine resistance knowing dissipation:

For the input winding: $.0555W \div .0427A^2 = 30\Omega$

For the +5V winding: $.0504W \div .55A^2 = .166\Omega$

For the -5V winding: $.00275W \div .030A^2 = 3.06\Omega$

For the 10V winding: $.0024W \div .014A^2 = 12.24\Omega$

This gives us enough information to complete a specification for the coupled magnetic. *(See Figure 9.)*

The value of the current sensing resistor can be determined once the peak input current is known. The sensing voltage levels for the HV9120 are the same as they were for the HV9110 in example 1. Thus

$$0.99V \div 0.108A = 9.16\Omega$$

The next lower resistor is 9.09Ω in 1% or 9.1Ω in 5%. As the last time, using a 5% resistor will probably result in very few (if any) units that do not allow full output power at low line. Wattage of the current sense resistor is calculated as I^2R using DC input current (42.7 mA). This calculates out to 16.6 mW based on a 9.1Ω resistor, so a 1/10 watt resistor (if you can find a noninductive one) can be used.

The drop across the main switch and its power loss should be calculated next. In this case we already selected a main switch (a Supertex VN0660N3) based solely on its being the smallest (and least expensive) 600V MOSFET available. The on-resistance of the VN0660N3 is 20Ω, which implies a peak-current voltage drop of 2.16V, and a power dissipation of 36mW, which is easily handled by the TO-92 version.

Using the "square root of inductances ratio" we can now determine the approximate voltages reflected across the coupled inductor to determine the actual voltages present on the main switch when it is off and the diodes when they are blocking. This time that works out to:

$$\sqrt{\frac{625 \times 10^{-6}}{3.7 \times 10^{-6}}}$$

or almost exactly 13:1. Thus when the main switch is off, it will see:

5.7V x 13 = 74V

added to the 390V present from the input, a total of 464V. The diodes, when blocking, can see a maximum of

390 ÷ 13 = 30V

added to the 5V present on the output capacitors. So 1A 40V Schottky diodes, such as the 1N5819, should work well for 5V output diodes.

If increased efficiency were required, 1N5822 three-amp Schottky diodes, and/or a 500V, 16Ω, VN0650N3 main switch could be substituted.

As with the first example, the next thing to do is to calculate the requirements for the output filter capacitors. This time the ripple specification is easier to meet (100mV vs 25) and the loads are smaller. The technique remains the same, and a 25%/75% division of ripple between capacitance and ESR should still hold. Thus, for the +5V output

$C = 0.55A \div (.025V \div 930 \times 10^{-9}sec) = 20.5\mu F$

Remember that for capacitor holdup, *maximum* rather than minimum t_{on} is used, as the time for which the capacitor must hold up is the maximum time the switch could possibly be on. ESR ripple is also done exactly as before:

$ESR = .075V \div 1.328A = .565\Omega$

This is a much easier capacitor to find. A Nichicon SF type 150µF, 6.3V would work fine. So would a Sprague 672D227H6R3CG3C (220µF, 6.3V aluminum) or a Sprague 199D336X96R3DA1 (33µF, 6.3V dipped tantalum).

The -5V secondary works the same way, except the current is only 30mA:

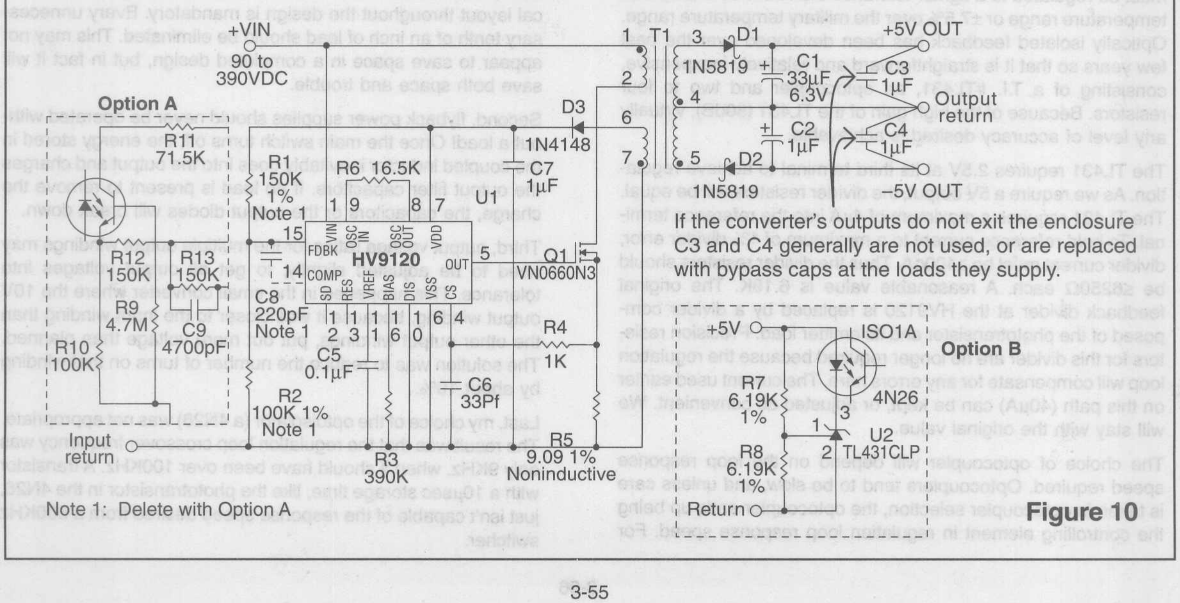
$C = 0.030A \div (.025V \div 930 \times 10^{-9}sec) = 1.1\mu F$

$ESR = .075V \div .073A = 1.0\Omega$

In this case, because the load current (and thus the capacitor) are so small, it is probably better to use a 1µF stacked film capacitor and ignore the ESR which will be orders of magnitude below requirements. A 1µF 50V Wima #MKS-2 (ESR ≈ .02Ω) would be fine. The same capacitor could also be used on the 10V output that feeds the HV9120 (14mA). This particular capacitor is also an excellent choice for the final noise filters on the regulator's outputs (as in example 1). But in this case the regulator's outputs will not go outside the enclosure and extra noise filters are probably unnecessary.

Feedback for this circuit is shown two ways: First, as just a resistive divider off the secondary that feeds the HV9120, and second as optical feedback, which requires additional circuitry. *(See Figure 10.)* For the regulation specifications given, (±5%) a resistive divider on a separate winding is sufficient over the

The Final Design



Note 1: Delete with Option A

If the converter's outputs do not exit the enclosure C3 and C4 generally are not used, or are replaced with bypass caps at the loads they supply.

Figure 10

industrial temperature range (-40°C to +85°C). Such a "divider on a separate output" relies on the magnetic coupling between windings on a common core to regulate the isolated windings. Within limits (accuracy, mostly) it works very well, but it would require an excellent transformer builder to be able to meet ±5% regulation of magnetically coupled outputs over a full -55°C to +125°C military temperature range.

The resistive divider, as in the previous example, can draw very little current, because the CMOS error amp in the HV9120 does not draw significant bias current. Because the last example used 100µA divider current this one will use 40µA. (Using much less than 20µA requires using high value precision resistors that are expensive.) Again, the feedback point of the HV9120 is internally trimmed to expect 4.00V at design output voltage. This time the design voltage of the winding directly coupled to the divider is 10V, so using a 40µA divider current, the lower resistor becomes 100KΩ, and the upper resistor becomes 150KΩ.

Accessory Circuits

1. No snubber circuit is shown on this converter, and none should be necessary. Maximum energy available to be snubbed, like last time, is just $L_{leakage} \times I_{peak}^2$, or 117nJ per switch-off. At 600KHz that works out to 70mW, which is easy to ignore. Also, the main switch chosen has 20pF of reverse transfer capacitance, which can absorb this much energy while only rising an additional 76V. This still leaves V_{drain} of the MOSFET below 90% of breakdown and should be safe.

2. Leading-edge spike suppression on the current sense resistor can be handled as it was in the first example, with a 1KΩ resistor between the top of the current sense resistor and the current sense pin on the HV9120, plus a capacitor between the current sense terminal and ground. For this regulator, leading edge spike suppression is probably *more* important than it was for the last one, because the peak gate drive current to the power MOSFET is actually greater than the load current! Because the gate capacitance of the FET is much smaller though, the capacitor's size should be reduced. 33pF is a good starting value.

3. Optical feedback is usually only used on isolated outputs that must be regulated to a tighter tolerance than ±5% over industrial temperature range or ±7.5% over the military temperature range. Optically isolated feedback has been developed over the past few years so that it is straightforward and relatively inexpensive, consisting of a T.I. #TL431, an optocoupler and two to four resistors. Because of the high gain of the TL431 (80dB), virtually any level of accuracy desired is achievable.

The TL431 requires 2.5V at its third terminal to achieve regulation. As we require a 5V output, the divider resistors will be equal. The TL431 requires a maximum of 4µA into the reference terminal. To hold reference current to a maximum of 1% divider error, divider current must be ≥400µA. Thus the divider resistors should be ≤6250Ω each. A reasonable value is 6.19K. The original feedback divider at the HV9120 is replaced by a divider composed of the phototransistor and its emitter load. Precision resistors for this divider are no longer required because the regulation loop will compensate for any errors here. The current used earlier on this path (40µA) can be kept, or adjusted as convenient. We will stay with the original value.

The choice of optocoupler will depend on the loop response speed required. Optocouplers tend to be slow, and unless care is taken in optocoupler selection, the optocoupler ends up being the controlling element in regulation loop response speed. For this example, I used a 4N26 because it was on hand. A 6N135 or similar high speed optocoupler would have given loop response more appropriate for a 500KHz converter. The resistor shown between the base of the optoisolator transistor and ground is a noise/leakage eliminator and should have a value between 1MΩ and 10MΩ, depending on the optocoupler used. For a 4N26, 4.7M works well.

Because there are now two op amps in the regulation loop, loop gain will be far more than necessary, and some of it must be done away with. Otherwise stabilization will be a problem. There are two simple ways to eliminate gain. Either convert the error amp in the HV9120 to a gain of −1 configuration with two equal resistors, or add a resistor between the anode of the TL431 and output return to reduce its gain to approximately 1. Both methods work equally well. The error amp in the HV9120 has a minimum guaranteed output sink current of 120µA, so any feedback resistor greater than 50K will allow full opposite swing. 150K gives plenty of margin, and reduces power a little.

Alternatively, a resistor between the anode of the TL431 and output return can be used as a gain-destroyer to reduce the gain of the TL431 (plus the optoisolator) to approximately 1. The value of the gain-destroyer resistor is dependent on the coupling "gain" of the optoisolator and the current required from the phototransistor. Using a 4N26, the current required from the phototransistor is approximately 40µA, and the LED current required to achieve it will be approximately 100µA. To adequately reduce the gain of the TL431 will require a delta V on its anode of about 50mV, so a 470Ω resistor should work.

Conclusion

To demonstrate functionality, both examples were assembled and tested by a technician at our facility. A few suggestions to avoid difficulties are as follows:

First, wire-wrap construction methods are, and always will be, completely incompatible with power supply construction. The light gauge wire will not carry the current, and the stray inductance caused by longer-than-necessary paths will disrupt the circuit and cause additional EMI. Seriously, the requirement for short, low-inductance, low-resistance paths and good mechanical layout throughout the design is mandatory. Every unnecessary tenth of an inch of lead should be eliminated. This may not appear to save space in a completed design, but in fact it will save both space and trouble.

Second, flyback power supplies should never be operated without a load! Once the main switch turns off, the energy stored in the coupled inductor inevitably goes into the output and charges the output filter capacitors. If no load is present to remove the charge, the capacitors or the output diodes will break down.

Third, output voltage ratios for the multiple output windings may need to be adjusted slightly, to get all output voltages into tolerance. This happened in the small converter where the 10V output winding, because it was closer to the input winding than the other output windings, put out more voltage than planned. The solution was to reduce the number of turns on that winding by about 10%.

Last, my choice of the optoisolator (a 4N26) was not appropriate. The result was that the regulation loop crossover frequency was only 9KHz, when it should have been over 100KHz. A transistor with a 10µsec storage time, like the phototransistor in the 4N26, just isn't capable of the response speed desired from a 500KHz switcher.

In summation, two different circuits have been developed to show the flexibility of flyback converters built with the HV91XX family PWM ICs, and the simplicity of their design and construction. Both circuits met their original design goals. The field of use for the HV91XX family is a lot broader than can be illustrated in a single application note. Many other forms of converters, which may be best suited for their particular purposes can also be built using the HV91XX PWM ICs. Contact Supertex for additional application notes.

1. Reference Data for Radio Engineers, 6th ed.
Howard Sams & Co., chapter 44, table 4.

2. Virginia Power Electronics Center,
Bradley Department of Electrical Engineering,
Virginia Polytechnic Institute and State University,
Blacksburg VA 24061.

3. Available from publisher or see footnote 5.

4. Only available from publisher: TESLAco,
10 Mauchly, Irvine CA 92718 (714) 727-1960.

5. Books with ISBN numbers can be ordered from any bookstore. All the books in this list except the TESLAco book can also be acquired from:
E.J. Bloom Assoc. Educational Division,
115 Duran Dr., San Rafael CA 94903-2317
(415) 492-1239. They generally have them in stock.

6. Magnetic assemblies for the converters were supplied by:
GFS Manufacturing, Inc.
140 Crosby Rd., Dover NH 03820-1409 (603) 742-4375.

Low Dropout 3.0 Volt Linear Regulator

by Jimes Lei, Applications Engineer

Introduction

Low dropout regulators are becoming increasingly important as more and more equipment utilizes 3 volt and 5 volt analog and digital circuits.

The main advantage of low dropout 3.0V linear regulators is full utilization of battery life which makes them desirable for battery-powered applications. The low dropout feature will allow for output regulation even when the input battery voltage is discharged close to its output regulated voltage. This will extend the operating input voltage range and allow circuits to operate at a lower battery voltage.

This application note discusses the advantages of using Supertex part number LP0701N3, which is a very low gate threshold voltage P-Channel MOSFET. This part has a guaranteed maximum threshold of -1.0V and a maximum $R_{DS(ON)}$ of 2.0 ohms at -3.0V drive. This performance is essential for designing an ultralow dropout, low voltage linear regulator.

Circuit Description

The low dropout 3.0V linear regulator shown on Figure 1 utilizes an LP07, an LM10, 4 resistors, and 3 capacitors. The LP07 is a 16.5V, 2.0 ohm, P-Channel MOSFET with a maximum threshold of -1.0V. The LM10 is a dual op-amp with a 0.2V reference. R1 is a potentiometer. R2, R3, and R4 are 5%, 1 / 4 watt resistors. C1, C2, and C3 can be either ceramic or electrolytic capacitors.

A1 is configured as a unity gain buffer for the 0.2V reference. The output of A1 is attenuated by R1 and R2 and is connected to the inverting input of A2. A2 is configured as a noninverting amplifier with a closed-loop gain of (R4 / R3 + 1). The LP07 is configured as a common source amplifier, which functions as a series pass transistor while contributing additional gain to the open-loop gain of A2. The output of A2 regulates the gate of the LP07 for a V_{OUT} of 0.2V x [R1 / (R1 + R2) x (R4 / R3 + 1)]. The resistor values are chosen (explained in detail in the design considerations section of this application note) and R1 adjusted for an output voltage of 3.0V. C3 is in parallel with R4 to reject external noise. C1 and C2 are bypass capacitors.

Any small decrease in V_{OUT} due to a load applied to the output is sensed by R3 and R4 which is fed back to the noninverting input of A2. The output of A2 will drive the gate of the LP07 to a lower potential thereby increasing the gate drive adequately to source current to the output load and maintain a constant output voltage.

Design Considerations

The objective is to implement a 3.0V linear regulator with the lowest possible voltage drop from input to output. The output transistor for a linear regulator can be designed with N-Channel or P-Channel MOSFETs or bipolar NPN or PNP transistors. Figures 2a to 2d (see page 2) show the four possibilities.

In figure 2a, the dropout voltage using an N-Channel MOSFET is too large since it cannot be better than the threshold voltage of the

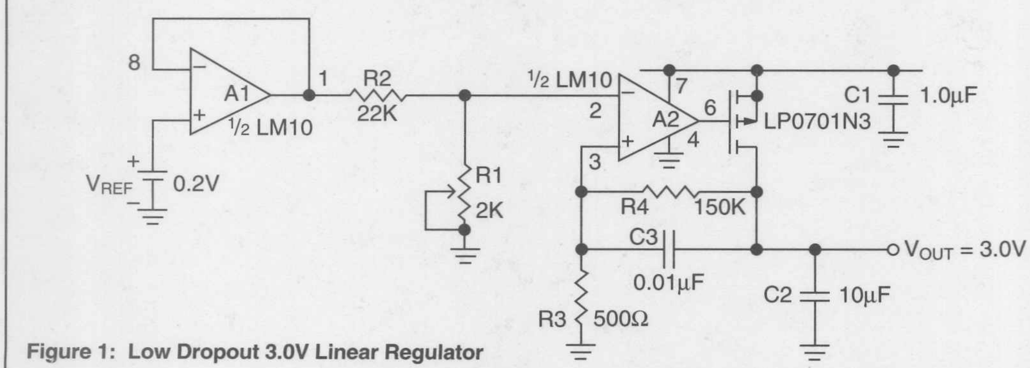


Figure 1: Low Dropout 3.0V Linear Regulator

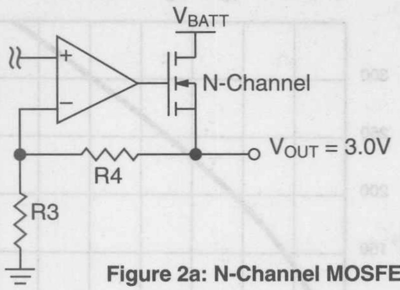


Figure 2a: N-Channel MOSFET

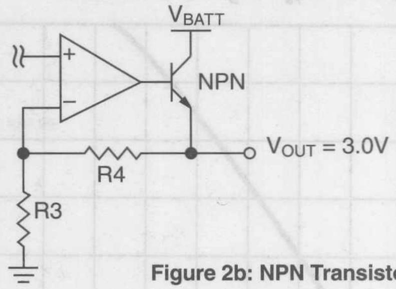


Figure 2b: NPN Transistor

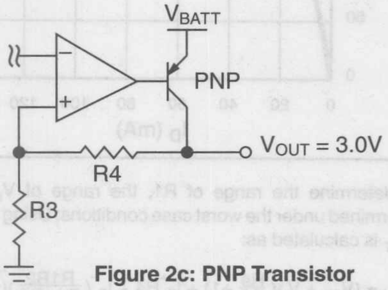


Figure 2c: PNP Transistor

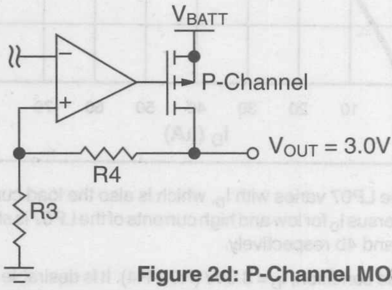


Figure 2d: P-Channel MOSFET

MOSFET, which is 1.0V to 4.0V, depending on the type of device used. In figure 2b, the dropout voltage using an NPN is lower but still fairly large. The dropout voltage is typically 0.7V, which is the V_{BE} rating of the transistor.

In figure 2c, the dropout voltage using a PNP transistor is limited by the $V_{CE(sat)}$ rating of the transistor, which is typically -200mV at low collector current. This approach also requires the output of the op-amp to operate 0.7V below its most positive rail at all times.

In figure 2d, the dropout voltage for the P-Channel MOSFET approach is determined by the on-resistance of the device times the load current. The device is driven by the battery voltage minus the minimum output voltage of the op-amp. Similar to the PNP approach, the op-amp is required to operate one threshold below the battery voltage during the no load condition. When the battery voltage is discharged close to 3.0V, the MOSFET chosen should have a very low threshold and a very low on-resistance at low V_{GS} ratings to achieve low dropout.

Conventional P-Channel MOSFETs have guaranteed maximum thresholds of -4.0V, which would require the supply voltage to be greater than 4.0V for adequate turn on. A low threshold, low on-resistance P-Channel MOSFET is ideal for this approach.

The Supertex LP07 has a guaranteed maximum threshold of -1.0V and guaranteed on-resistance at -2.0V, -3.0V, and -5.0V drives. The specifications are shown on the following table.

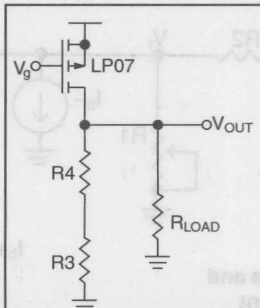
Parameter	Min	Typ	Max	Units	Conditions
$V_{GS(th)}$	-0.5	-0.7	-1.0	volts	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$R_{DS(ON)}$		2.0	4.0	ohms	$V_{GS} = -2V$, $I_D = -50mA$
		1.7	2.0	ohms	$V_{GS} = -3V$, $I_D = -150mA$
		1.3	1.5	ohms	$V_{GS} = -5V$, $I_D = -300mA$

At -3.0V, the on-resistance is 1.7 ohms typical and 2.0 ohms maximum, which helps achieve a low drain-to-source voltage drop. Since the LM10 can swing very close to ground i.e., 0V, the dropout voltage can be estimated to be 2.0 ohms x (I_{LOAD}). For a 50mA load, the dropout voltage is 0.1V which means the battery voltage can be 3.1V with the output still regulated at 3.0V.

Preventing Unwanted Oscillation

The LP07 acts as an additional gain stage to the open-loop gain of A2. The increase in open-loop gain causes the loop gain to be greater than 1 at low closed-loop gain conditions, which causes oscillation. Oscillation can be eliminated by setting the loop-gain to be less than 1. This can be achieved by setting ß(negative feedback) < 1 / gain contributed by the LP07.

The gain contributed by the LP07 is a function of the load and the transconductance, G_{FS}, of the LP07. Figure 3 shows an equivalent circuit of the open-loop gain of the LP07.



$$G_{FS} = \frac{\delta I_d}{\delta V_g}$$

$$V_{OUT} = I_d \left[\frac{(R3 + R4)(R_{LOAD})}{R3 + R4 + R_{LOAD}}\right]$$

$$\frac{V_{OUT}}{V_g} = G_{FS} \left[\frac{(R3 + R4)(R_{LOAD})}{R3 + R4 + R_{LOAD}}\right]$$

Figure 3: LP07 Open-Loop Gain

Figure 4a: G_{FS} vs. I_D at Low Currents

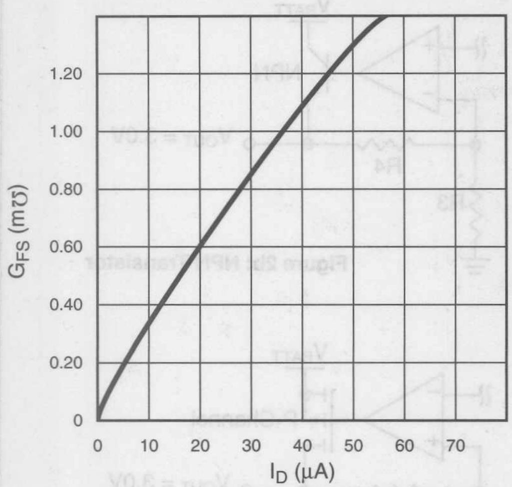
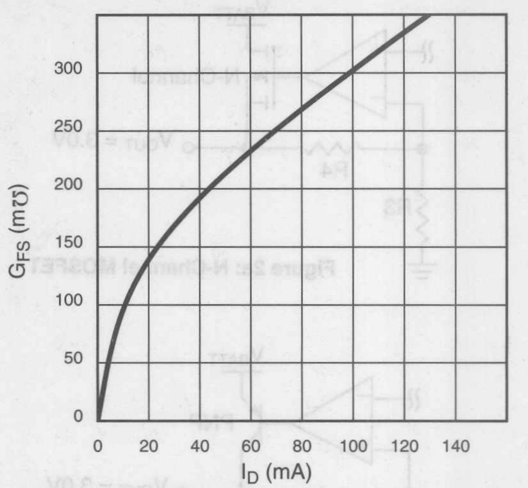


Figure 4b: G_{FS} vs. I_D at High Currents



The G_{FS} of the LP07 varies with I_D, which is also the load current. Typical G_{FS} versus I_D for low and high currents of the LP07 is shown on figure 4a and 4b respectively.

For the no load condition, $I_D = 3.0V / (R3 + R4)$. It is desirable have R3 + R4 large to minimize the amount of biasing current. The sum of R3 + R4 is chosen to be approximately 150K. From figure 4a, G_{FS} is 0.62m℧ for an I_D of 20µamps. V_{OUT} / V_G is calculated as (0.62m℧)(150K) = 93.

For a load current of 100mA, $R_{LOAD} = 3.0V / 100mA$. Using figure 4b, V_{OUT} / V_G is calculated as (310m℧)(30ohms) = 9.3. The open-loop gain varies with load and is at its maximum during the no load condition. The negative feedback, ß, is R3 / (R3 + R4) and should be set less than or equal to $1 / (V_{OUT} / V_G)$.

It is desirable to set ß<<1 / 93 since 1 / 93 is a typical value. R3 and R4 are chosen to be 500 ohms and 150K respectively for a ß of 1 / 301, providing an adequate safety margin.

Calculations

The offset voltage, V_{OS}, input biasing current, I_B + and I_B-, and tolerances of the external resistors will affect the output voltage. R1 is used to adjust V_{OUT} to 3.0V. Figure 5 is an equivalent circuit showing V_{OS}, I_B +, and I_B-.

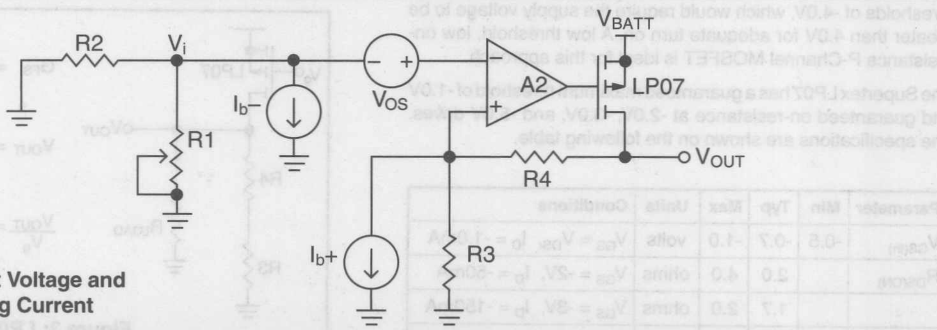


Figure 5: Offset Voltage and Input Biasing Current

To determine the range of R1, the range of V_I needs to be determined under the worst case conditions. Using superposition, V_{OUT} is calculated as:

$$V_{OUT} = (V_{OS} + V_I)(\frac{R4}{R3} + 1) + I_B^+ R4 + I_B^- (\frac{R1R2}{R1+R2})(\frac{R4}{R3} + 1)$$

The LM10 guarantees V_{OS} = 4.0mV max and I_B = 30nA max. R1 x R2 / (R1 + R2) is set at 2K.

For minimum Vi:

$$3.0V = (V_I + 4.0mV)(\frac{157.5K}{475} + 1) + 30nA\ (157.5K) + 30nA(2K)(\frac{157.5K}{475} + 1)$$

3.0V = 3332.6Vi + 1.330V + 4.725mV + 19.95mV

Vi(min) = 4.947mV

For maximum Vi:

$$3.0V = (V_I - 4.0mV)(\frac{142.5K}{525} + 1) - 30nA\ (142.5K) - 30nA(2K)(\frac{142.5K}{525} + 1)$$

3.0V = 272.4Vi-1.090V-4.275mV-16.35mV

Vi(max) = 15.09mV

Figure 6: Dropout Voltage

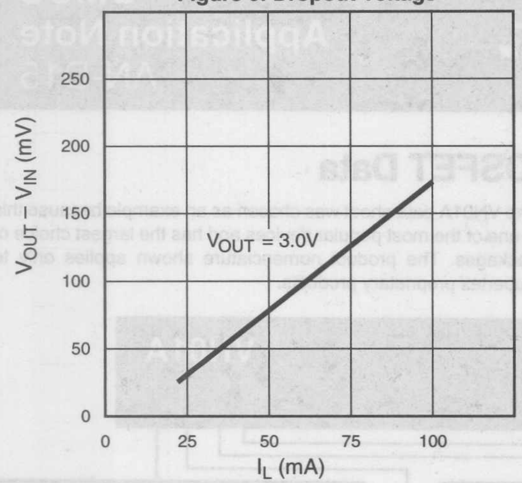
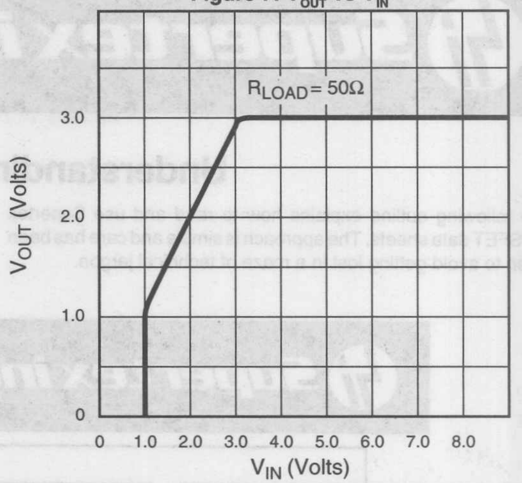


Figure 7: V_{OUT} vs V_{IN}



The range for R1 is:

$$\frac{R1}{R1+R2}(200mV) = Vi$$

$$R1 = \frac{R2}{39.40} \text{ to } \frac{R2}{12.25}$$

Choosing R1 to be a 2K potentiometer, R2 = (2K)(12.25) = 24.5K. R2 should be less than 24.5K so under the worst case conditions, R1 would not operate at its maximum value of 2K. R2 is chosen to be 22K. The range of R1 is calculated as:

R1 = 22K(0.95) / 39.4 to 22K(1.05) / 12.25

R1 = 531 ohms to 1.89K ohms

Measurements

Actual measurements were recorded and are shown on figures 6 and 7. Figure 6 shows the dropout voltage at different load currents. Figure 7 shows the output voltage regulation versus the decrease in battery voltage with a fixed load.

5V Regulators

The low dropout 3.0V regulator in figure 1 can be easily modified to a 5.0V or adjustable low dropout regulator by changing R1 to a 5K potentiometer. Using a voltage controlled resistor for R1 will allow for a programmable low dropout regulator.

Conclusion

Low dropout 3.0V linear voltage regulators are ideal for portable battery operated applications to help extend battery life. The low dropout voltage allows the battery powered equipment to operate at a lower battery voltage.

In addition to the other advantages discussed, MOSFETs increase the efficiency of the circuit because of the current required to drive the gate is virtually zero as it is usually in the sub nanoampere area. Bipolars need base current and this is undesirable especially when battery energy is at a budget. LP07 is ideal for linear applications requiring high efficiency because of its low threshold voltage and low guaranteed on-resistances at 2V, 3V and 5V drives.

Supertex inc.

DMOS Application Note
AN-D15

Understanding MOSFET Data

The following outline explains how to read and use Supertex MOSFET data sheets. The approach is simple and care has been taken to avoid getting lost in a maze of technical jargon.

The VN01A data sheet was chosen as an example because this is one of the most popular devices and has the largest choice of packages. The product nomenclature shown applies only to Supertex proprietary products.

Supertex inc. VN01A

Device Structure

V: Vertical DMOS (discretes & quads)

D: Vertical Depletion-Mode DMOS discretes

T: Low threshold vertical DMOS discretes

A: Lateral DMOS arrays

L: Lateral DMOS discretes

Type of Channel

- N-Channel, or
- P-Channel

Design

Supertex Family number

Voltage Range

Suffix	Min BV_{DSS} volts
U:	18
L:	20, 40
A:	40, 60, 90, 100
C:	160, 200, 240
D:	350, 400
E:	450, 500
F:	550, 600

- Some A range devices not available in 40, 90 & 100V
- Some C range devices not available in 240V

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speed are desired.

This section outlines main features of the product

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

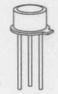
BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package: TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	DICE
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109ND

Drain to source breakdown voltage & drain to gate breakdown voltage

Maximum resistance from drain to source when device is fully turned on

Minimum drain current when device is fully turned on

Package Options

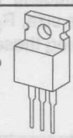
TO-39

Hermetic metal can
- Moderate power dissipation
- Industrial/Military applications

TO-92

Plastic
- Low power
- Mainly commerical applications
- Cost effective

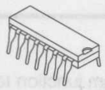
TO-52

Hermetic metal can
- Low power Industrial/ Military applications

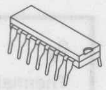
TO-220

Plastic
- High power
- Commerical/Industrial applications

Ordering Information

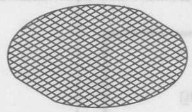
BV_{DSS}/ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-92	TO-52	TO-220	Quad P-DIP	Quad C-DIP	DICE
40V	3Ω	2.0A	VN0104N2	VN0104N3	VN0104N9	VN0104N5	VN0104N6	VN0104N7	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N3	VN0106N9	VN0106N5	VN0106N6	VN0106N7	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N3	VN0109N9	VN0109N5	—	—	VN0109ND

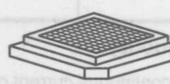

14-Lead DIP

Dual in line plastic
- 4 dice in one package
- Commerical/Industrial applications


14-Lead DIP

Dual in line ceramic
- 4 dice in one package for Industrial/Military requirements


NW: Die in wafer form
- 4 inch diameter wafers
- Reject die are inked


ND: Die in waffle pack

Die can be visually inspected to commercial (standard) or military visual criteria (specify while ordering)

Absolute Maximum Ratings

Extreme conditions a device can be subjected to electrically and thermally. Stress in excess of these ratings will usually cause permanent damage.

Drain-to Source Voltage	BV_{DSS}
Drain-to-Gate	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature	300°C

Ratings given in product summary.

V_{GS}
- Most Supertex FETs are rated for ±20V
- ± voltage handling capability allows quick turn off by reversing bias.
- External protection should be used when there is a possibility of exceeding this rating. Stress exceeding ±20V will result in gate insulation degradation and eventual failure.

Maximum allowable temperature at leads while soldering, 1.6mm away from case for 10 seconds.

- All Supertex devices can be stored and operated satisfactorily within these junction temperature (T_J) limits.
- Appropriate derating factors from curves and change in parameters due to reduced/ elevated temperatures have to be considered when temperature is not 25°C.
- Operation at T_J below maximum limit can enhance operating life.

Thermal Characteristics

Device characteristics affecting limits of heat produced and removed from device. Die size, $R_{DS(ON)}$ and packaging type are the main factors determining these thermal limitations.

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	0.8A	2.5A	3.5W	125	35	0.8A	2.5A
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-52	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-220	1.5A	2.5A	15.0W	70	8	1.5A	2.5A
Plastic DIP Ceramic DIP		See DMOS Arrays & Special Functions section					

I_D (continuous)

Maximum continuous current carrying capability of device.

- Depends mainly on:
  - A. $R_{DS(ON)}$ - on state resistance
  - B. P_D - maximum power dissipation for package
  - C. Die size
  - D. Maximum junction temperature

I_D (pulsed)

Maximum non-continuous pulse current carrying capability for a 300 µS 2% duty cycle pulsed.

- Depends mainly on :
  - A. $R_{DS(ON)}$
  - B. P_D max
  - C. Diameter of bonding wire
  - D. Die size
  - E. Maximum junction temperature

Power Dissipation

- Maximum power package can dissipate when case temperature is 25°C.
- When case temperature is higher than 25°C, use P_D vs. T_C curve to determine dissipation permissible.

θ_{ja}

Thermal resistance from junction to air.

- Depends mainly on package and die size

θ_{jc}

Thermal resistance from junction to case.

- Depends mainly on package and die size
- To determine T_J use equation $T_J = P_D \times \theta_{jc} + T_A$

I_{DR}

Continuous current handling capability of drain to source diode.

- Factors affecting value same as I_D (continuous)

I_{DRM}

300 µS, 2% duty cycle pulsed. Current handling capability of drain source diode.

- Factors affecting this parameter same as I_D (pulsed)

Electrical Characteristics

The following DC parameters are 100% tested with 300µS, 2% duty cycle pulsed at 25°C, BV_{DSS}, $V_{GS(TH)}$, I_{DSS}, $I_{D(ON)}$ & $R_{DS(ON)}$.

- $\Delta V_{GS(TH)}$ and $\Delta R_{DS(ON)}$ are guaranteed by design ie., when device is functional for other DC parameters, these two parameters will not deviate from published values.
- Since a representative sample is adequate to assure consistency of specs, A.C. parameters are sample tested on a lot/batch basis.
- High temperature testing on sample basis when requested with hi-rel processing.
- Refer to section 3 "power MOS structures" for test circuits used for measurement.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	$V_{GS}=0$, $I_D = 1mA$
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS}=V_{DS}$, $I_D=1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS}=V_{DS}$, $I_D=1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS}=0$, $V_{DS}=$ Max Rating
					100		$V_{GS}=0$, $V_{DS}=0.8$ Max Rating $T_A=125°C$
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	$V_{GS}=5V$, $V_{DS}=25V$
			2.0	2.5			$V_{GS}=10V$, $V_{DS}=25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	$V_{GS}=5V$, $I_D=250mA$
				2.5	3		$V_{GS}=10V$, $I_D=1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1	%/°C	$V_{GS}=10V$, $I_D=1A$
G_{FS}	Forward Transconductance		300	450		m℧	$V_{DS}=25V$, $I_D=0.5A$
C_{ISS}	Input Capacitance			45	60	pF	
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD}=25V$ $I_D=1A$ $R_{GEN}=25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS}=0$, $I_{SD}=1.0A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS}=0$, $I_{SD}=1.0A$

BV_{DSS}

- Please see product summary (part I)
- Positive temperature coefficient. See curve BV_{DSS} vs. T_J.

$V_{GS(TH)}$

- Voltage required from gate to source to turn on device to certain I_D current value given in "condition" column.
- I_D measurement condition is low for small die and higher for larger die.

$\Delta V_{GS(TH)}$

- Threshold voltage reduces when temperature increases and vice versa.
- Value at temperature other than 25 °C can be determined by $V_{GS(TH)}$ (normalized) vs. T_J curve.

I_{GSS}

- Since the gate is insulated from the rest of device by a silicon dioxide insulating layer, this parameter depends on thickness/integrity of layer and size of device.
- Measured at maximum permissible voltage from gate to source: ±20V.
- Values of this parameter are often tens/hundreds of times less than published maximum value. Electrical screening is done at 100nA since test equipment functions slowly at lower values, which is not practical for mass production. Consult factory for screening lower values.

I_{DSS}

- This is the leakage current from drain to source when device is fully turned off.
- Measured by applying maximum permissible voltage between drain and source (BV_{DSS}) and gate shorted to source ($V_{GS} = 0$)
- Special electrical screening possible at lower values since max. published values are higher to achieve practical testing speeds.

$I_{D(ON)}$

- Defined as the minimum drain current when device is turned on.
- Supertex measures $I_{D(ON)}$ min. at two test conditions:

  V_{GS} = 5V and V_{GS} = 10V, to give the designer a look at both logic level turn on and full turn on

  Although Supertex specifies a typical value of $I_{D(ON)}$, the designer should use minimum value as the worst case.

$R_{DS(ON)}$

- Drain to source resistance measured when device is partially turned on at V_{GS} = 5V, and fully turned on at V_{GS} = 10V.
- Designers should use maximum values for worst case condition.
- When better turn on characteristics (ie., low $R_{DS(ON)}$) is required for logic level inputs, Supertex's low threshold TN & TP devices may be used.
- Typical value of $R_{DS(ON)}$ can be calculated at various V_{GS} conditions by using output characteristics or saturation characteristics family of curves (I_D vs. V_{DS}).
- $R_{DS(ON)}$ increases with higher drain currents. $R_{DS(ON)}$ curve has a slight slope for low values of I_D, but rises rapidly for high values.

$\Delta R_{DS(ON)}$

- Positive temperature coefficient.
- Enhances stability due to current sharing during parallel operation.

Switching Characteristics

- Extremely fast switching compared to bipolar transistors, due to absence of minority carrier storage time during turn off.
- Switching times depend almost totally on interelectrode capacitance, R_S (source impedance) and R_L (load impedance) as shown on test circuit.

G_{FS}

- Represents gain of the device and can be compared to H_{FE} of a bipolar transistor.
- Value is the ratio of change in I_D for a change in V_{GS}

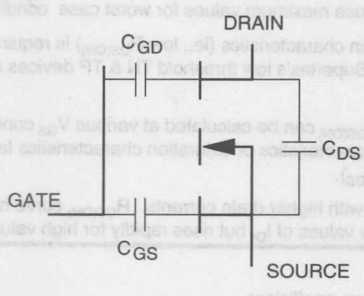
$$G_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$$

- Rises rapidly with increasing I_D, and then becomes constant in the saturation region. See G_{FS} vs. I_D curve.

C_{ISS}, C_{RSS}, C_{OSS}

- Please see section 3 in Databook "Power MOSFET Electrical Performance" for interelectrode capacitances and equivalent circuit.
- Supertex interdigitated structures have lowest C_{ISS} in the industry for comparable die sizes and exhibit excellent switching characteristics.
- Values of these capacitances are high at low voltages across them. Please see capacitance vs V_{DS} curves for details.
- Negligible effect of temperature on capacitances.
- The following equation may be used for calculating effective value of C_{ISS} with "Miller Effect."

$$C_{ISS} = C_{GS} + (1+G_{FS}\,R_L)\,C_{GD}$$



$$C_{ISS} = C_{GD} + C_{GS}$$
$$C_{OSS} = C_{GD} + C_{DS}$$
$$C_{RSS} = C_{GD}$$

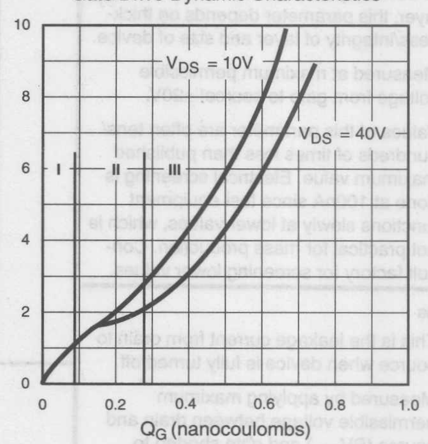
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	$V_{GS}=0$, $I_D = 1mA$
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS}=V_{DS}$, $I_D=1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS}=V_{DS}$, $I_D=1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
I_{DSS}	Zero Gate Voltage Drain Current				1	μA	$V_{GS}=0$, $V_{DS}=$ Max Rating
					100		$V_{GS}=0$, $V_{DS}=0.8$ Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	$V_{GS}=5V$, $V_{DS}=25V$
			2.0	2.5			$V_{GS}=10V$, $V_{DS}=25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	$V_{GS}=5V$, $I_D=250mA$
				2.5	3		$V_{GS}=10V$, $I_D=1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1	%/°C	$V_{GS}=10V$, $I_D=1A$
G_{FS}	Forward Transconductance		300	450		m℧	$V_{DS}=25V$, $I_D=0.5A$
C_{ISS}	Input Capacitance			45	60	pF	
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD}=25V$ $I_D=1A$ $R_{GEN}=25Ω$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS}=0$, $I_{SD}=1.0A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS}=0$, $I_{SD}=1.0A$

$T_{d(ON)}$

During this period, the drive circuit charges C_{ISS} up to $V_{GS(TH)}$. Since no drain current flows prior to turn on, V_{DS} and consequently C_{ISS} remain constant. Region I on the V_{GS} vs. Q_G curve shows linear change in voltage with increasing Q_G.

Gate Drive Dynamic Characteristics



Switching Characteristics (continued)

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	$V_{GS} = 0$, $I_D = 1mA$
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0$, $V_{DS} =$ Max Rating
					100		$V_{GS} = 0$, $V_{DS} = 0.8$ Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			2.0	2.5			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	$V_{GS} = 5V$, $I_D = 250mA$
				2.5	3		$V_{GS} = 10V$, $I_D = 1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1	%/°C	$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance		300	450		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			45	60	pF	
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = 25V$ $I_D = 1A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0$, $I_{SD} = 1.0A$

t_r

- When C_{ISS} is driven to a voltage exceeding $V_{GS(TH)}$, conduction from drain source begins. G_{FS} increases causing increase in C_{ISS} due to "Miller Effect" Charge requirements to Region II increase considerably. Gain stabilizes in Region III and "Miller Effect" is nullified, resulting in a linear change in V_{GS} for increase in Q_G.

$t_{d(OFF)}$

- The sequence of events now begins to reverse. C_{ISS} discharges through R_{GEN}. The rise of V_{DS} is initially slowed by increase of output capacitance.

t_f

- V_{DS} rises as the load resistor charges the output capacitance.

V_{SD}

- This is the forward voltage drop of the parasitic diode between drain and source.
- Diode my be used as a commutator in H bridge configurations or in a synchronous rectifier mode. Excessive fly back voltages may be clamped by this diode in a totem pole configuration.

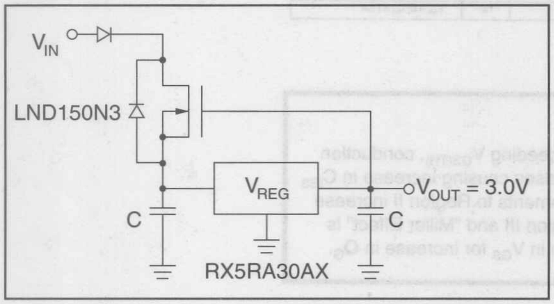
t_{RR}

- The reverse recovery time is the time needed for the carrier gradient, formed during forward biasing, to be depleted when the biasing is reversed.
- An external fast recovery diode may be connected from drain to source to improve recovery time.

Constant Current Sources and Depletion-Mode FETs

Depletion-mode MOSFETs can be used either as "normally closed" switches or current sources. This note shows circuits, utilizing depletion mode devices, that will benefit many applications. The main performance features of the circuits and examples of applications are listed. For more applications information on depletion mode MOSFETs, refer to other LND1 and DN25 series application notes.

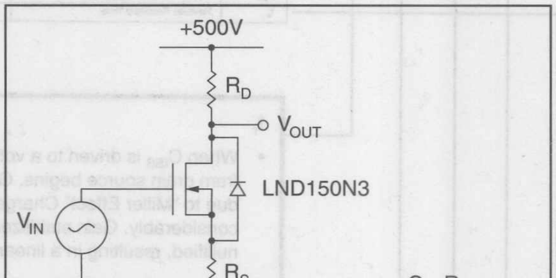
High Voltage Protected Regulator



- ☐ ±500V transient protection
- ☐ +5 to +500V operation
- ☐ Typically 800nA quiescent current
- ☐ See application note AN-D17 for details

Telecommunication, automotive, fax machines, off-line control circuits

Zero Bias Amplifier

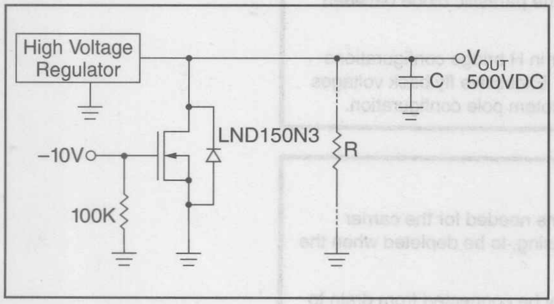


$$V_{OUT} = V_{DD} - \frac{G_{FS}R_D}{1+G_{FS}R_S} V_{IN}$$

- ☐ Very high input impedance
- ☐ Large output swing

Instrumentation amplifier for sensors/transducers

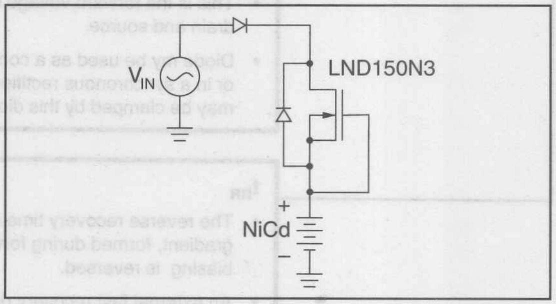
Switchable Bleed Resistor



- ☐ 500V operation
- ☐ Saves power

High voltage power supply, lab equipment

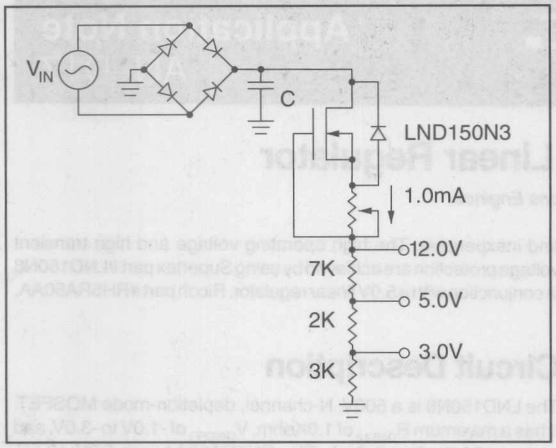
Off-Line Trickle Charger



- ☐ Suitable for single or multiple cells
- ☐ High compliance voltage

Hard-wired smoke alarms, burglar alarms, security systems

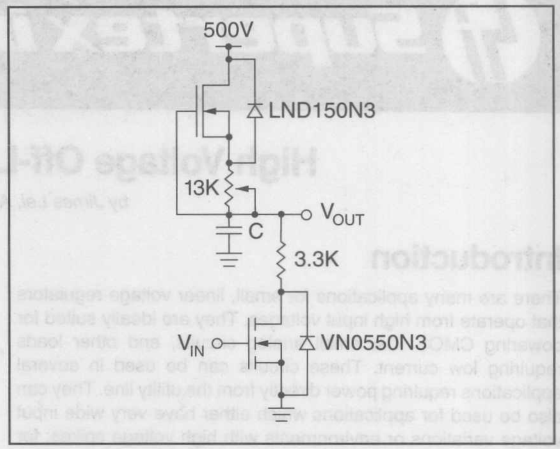
Off-Line Voltage Reference



- Universal input
- Resistor values determine voltage references
- See application note AN-D10 for details

Instrumentation, VCRs, televisions, ATEs

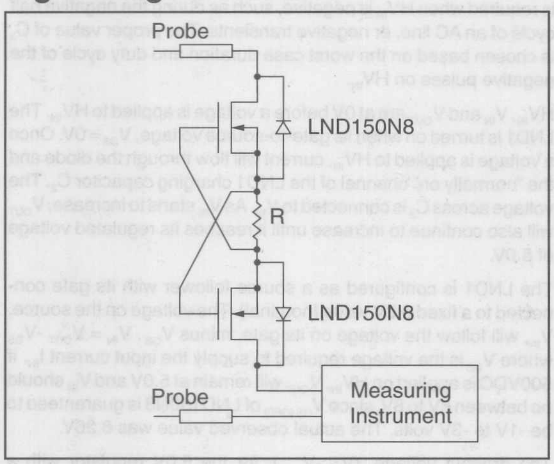
High Voltage Ramp Generator



- High linearity
- Adjustable slope
- See application note AN-D12 for details

Piezo transducer drivers, measuring instruments, soft start controls

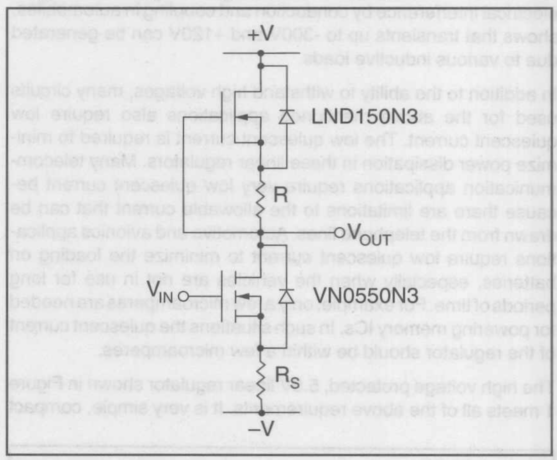
High Voltage Protection



- ±500V protection
- Stack for ±1000V or higher
- Current limiter
- See application note AN-D11 for details

Handheld meters, lab instruments, data communication lines, resettable fuses

High Voltage High Gain Amplifier



- High input impedance
- Up to 500 V operation
- Over 60dB gain

High voltage linear regulators, instrumentation amplifiers, piezo transducer drivers

High Voltage Off-Line Linear Regulator

by Jimes Lei, Applications Engineer

Introduction

There are many applications for small, linear voltage regulators that operate from high input voltages. They are ideally suited for powering CMOS ICs, small analog circuits, and other loads requiring low current. These circuits can be used in several applications requiring power directly from the utility line. They can also be used for applications which either have very wide input voltage variations or environments with high voltage spikes; for example, telecommunications, automotive, and avionics. This application note discusses several circuits which will benefit these applications.

Direct off-line applications require operation at 120VAC to 240VAC which corresponds to maximum peak voltages of ±340V. Applications in telecommunications, automotive, and avionics require immunity against very fast, high voltage transients. In telecommunications, the high voltage transients are caused by lightning or spurious radiations. In automotive and avionics they are caused by inductive loads such as ignition coils and electrical motors. International Standards Organization specification ISO/TR7637, for electrical interference by conduction and coupling in automobiles, shows that transients up to -300V and +120V can be generated due to various inductive loads

In addition to the ability to withstand high voltages, many circuits used for the above mentioned applications also require low quiescent current. The low quiescent current is required to minimize power dissipation in these linear regulators. Many telecommunication applications require very low quiescent current because there are limitations to the allowable current that can be drawn from the telephone lines. Automotive and avionics applications require low quiescent current to minimize the loading on batteries, especially when the vehicles are not in use for long periods of time. For example, only a few microamperes are needed for powering memory ICs. In such situations the quiescent current of the regulator should be within a few microamperes.

The high voltage protected, 5.0V linear regulator shown in Figure 1 meets all of the above requirements. It is very simple, compact and inexpensive. The high operating voltage and high transient voltage protection are achieved by using Supertex part #LND150N8 in conjunction with a 5.0V linear regulator, Ricoh part #RH5RA50AA.

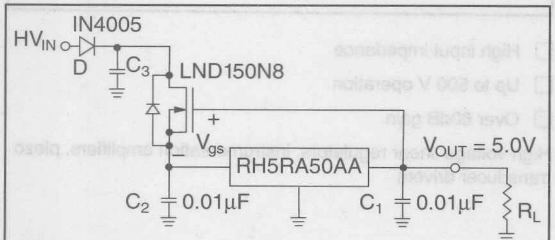


Figure 1: High Voltage Universal Off-Line Linear Regulator

Circuit Description

The LND150N8 is a 500V, N-channel, depletion-mode MOSFET. It has a maximum $R_{DS(ON)}$ of 1.0Kohm, $V_{GS(OFF)}$ of -1.0V to -3.0V, and an I_{DSS} of 1.0mA to 3.0mA. The RH5RA50AA is a 5.0V ±2.5% voltage regulator with a maximum quiescent current of 1.0µamp. Both these parts are available in the SOT-89 (TO-243AA) surface mount package.

The high voltage input, HV_{IN}, is connected to the anode of diode D. The cathode of the diode is connected to the drain of the LND1. The diode is used as protection against negative transient voltages and as a half-wave rectifier for off-line application. The LND1 is connected in the source follower configuration, with its gate connected to the output, V_{OUT}, and its source to the input of the 5.0V regulator, V_{IN}. Capacitors C_1, C_2 and C_3 are bypass capacitors. C_3 is required when HV_{IN} is negative, such as during the negative half cycle of an AC line, or negative transients. The proper value of C_3 is chosen based on the worst case duration and duty cycle of the negative pulses on HV_{IN}.

HV_{IN}, V_{IN} and V_{OUT} are at 0V before a voltage is applied to HV_{IN}. The LND1 is turned on when its gate-to-source voltage, V_{GS} = 0V. Once a voltage is applied to HV_{IN}, current will flow through the diode and the "normally on" channel of the LND1 charging capacitor C_2. The voltage across C_2 is connected to V_{IN}. As V_{IN} starts to increase, V_{OUT} will also continue to increase until it reaches its regulated voltage of 5.0V.

The LND1 is configured as a source follower with its gate connected to a fixed 5.0V value (nominal). The voltage on the source, V_{IN}, will follow the voltage on its gate, minus V_{GS}. $V_{IN} = V_{OUT} - V_{GS}$ where V_{GS} is the voltage required to supply the input current I_{IN}. If 500VDC is applied on HV_{IN}, V_{OUT} will remain at 5.0V and V_{IN} should be between 6V to 8V, since $V_{GS(OFF)}$ of LND150N8 is guaranteed to be -1V to -3V volts. The actual observed value was 6.26V.

The dropout voltage, ($V_{IN} - V_{OUT}$), for the 5.0V regulator with a 1.0mA load is rated as 30mV. To maintain regulation, V_{IN} must be equal to or greater than 5.03V. As I_{IN} increases, V_{IN} decreases and thereby increases the gate-to-source voltage on the LND1 to meet the I_{IN} requirement. The transfer characteristics of the LND1 gives a good indication of V_{GS} vs. I_{IN}.

Advantages of the LND1

The important parameters of the LND1 are its 500V breakdown voltage, 1.5pF output capacitance and 1.0Mohm dynamic output

impedance. Supertex utilizes a proprietary design and fabrication process to achieve very flat output characteristics which gives this device its very high dynamic impedance, r_O. The RH5RA50AA has an absolute maximum input voltage rating of 13.5V. The high breakdown voltage of the LND1 extends the maximum input operating voltage range from 13.5V to 500V. The low output capacitance and high dynamic impedance prevent the input voltage of the RH5RA50AA from exceeding its absolute maximum value of 13.5V when very fast high voltage transients are present. The ripple rejection ratio is also improved by several orders of magnitude.

LND1 improves the performance of the 5.0V linear regulator in the areas listed below. Observations and measurements were taken under three different loading conditions: no load, 10Kohm, and 5.0Kohm.

a) DC operation extended from 13.5V to 500V

b) High voltage transient protection

c) Greatly improved ripple rejection ratio

d) Eliminates power-up transients

DC Operation

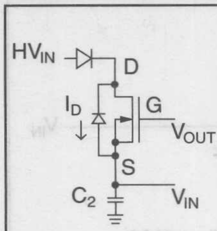
The LND1 increases the maximum operating voltage range from 13.5VDC to 500VDC. In order for the output to maintain regulation, the voltage difference (V_{IN}-V_{OUT}), must be greater than the regulator's specified dropout voltage of 30mV at 1.0mA load current. The measurements are shown below.

HV_{IN}	I_{IN}	V_{IN}	V_{OUT}	Conditions
10V to 500V	770nA	6.26V	5.02V	No load
10V to 500V	503µA	5.56V	5.02V	10Kohm
10V to 500V	1.0mA	5.30V	5.02V	5.0Kohm

Since the LND150N8 is connected in a source follower configuration, the value of V_{IN} can be estimated as shown in Figure 2.

High Voltage Transient Protection

Positive and negative transient voltages were applied on HV_{IN}. The positive transient voltages are blocked by the LND1 and the negative transient voltages are blocked by the 1N4005 diode, which has a 600V PIV rating.



$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$V_{GS} = V_{OUT} - V_{IN}$$

$$V_{IN} = V_{OUT} - V_{GS(OFF)}\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

Figure 2: V_{IN} Calculation

Figure 3 shows the test conditions used for simulating transient voltages. Positive 300V pulses with a pulse width of 500nsec, a rise time of 10nsec, and a duty cycle of 1.0% are superimposed on the 10VDC line of HV_{IN}. Figures 4a and 4b are waveforms showing HV_{IN}, V_{IN} and V_{OUT}.

The low drain-to-source capacitance, $C_{DS} = C_{OSS} - C_{RSS} = 1.5pF$, and high dynamic output impedance, $r_O = 1.0Mohm$, of the LND1 inherently give the LND1 excellent frequency response. The LND1 configured as a source follower will effectively protect high voltage

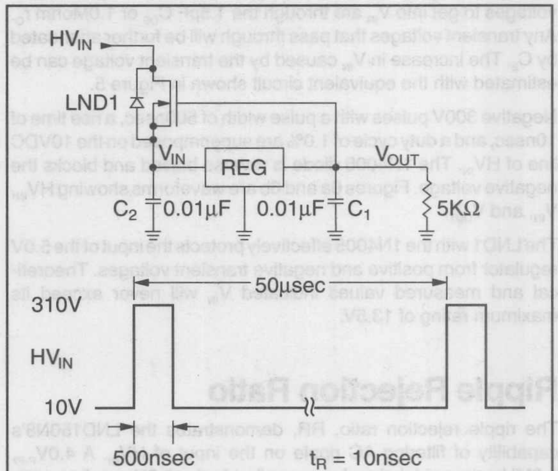


Figure 3: Positive Transient Test Condition

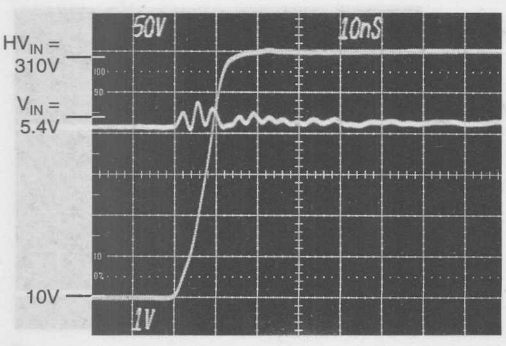


Figure 4a: HV_{IN} and V_{IN}

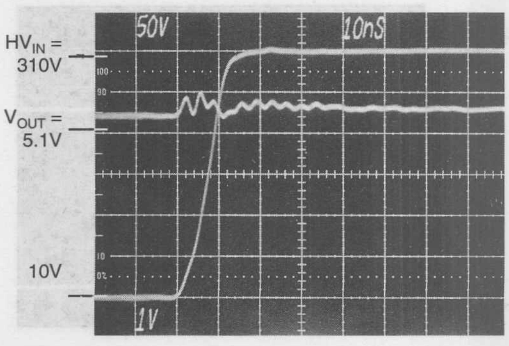
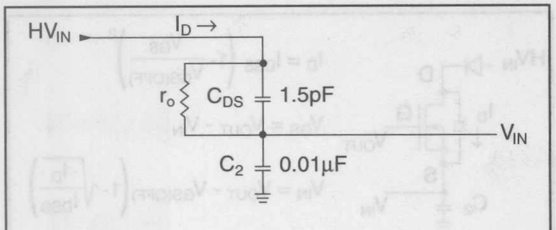


Figure 4b: HV_{IN} and V_{OUT}



r_o = AC resistance, typically 1.0MΩ (almost no effect on V_{IN})

$$I_D = C_{DS}\frac{dV}{dt} = 1.5pF\left(\frac{300V}{10nsec}\right) = 45mA$$

$$\Delta V_{IN} = \frac{I \bullet dt}{C_2} = \frac{(45mA)\,(10nsec)}{0.01\mu F}$$

$$\Delta V_{IN} = 45mV_{PEAK}$$

Figure 5: Estimate V_{IN} Increase due to Transients

transients on HV_{IN} from affecting V_{IN}. The only paths for transient voltages to get into V_{IN} are through the 1.5pF C_{DS} or 1.0Mohm r_O. Any transient voltages that pass through will be further attenuated by C_2. The increase in V_{IN} caused by the transient voltage can be estimated with the equivalent circuit shown in Figure 5.

Negative 300V pulses with a pulse width of 500nsec, a rise time of 10nsec, and a duty cycle of 1.0% are superimposed on the 10VDC line of HV_{IN}. The 1N4005 diode is reverse biased and blocks the negative voltage. Figures 6a and 6b are waveforms showing HV_{IN}, V_{IN}, and V_{OUT}.

The LND1 with the 1N4005 effectively protects the input of the 5.0V regulator from positive and negative transient voltages. Theoretical and measured values indicated V_{IN} will never exceed its maximum rating of 13.5V.

Ripple Rejection Ratio

The ripple rejection ratio, RR, demonstrates the LND150N8's capability of filtering AC ripple on the input of HV_{IN}. A $4.0V_{P-P}$, 1.0MHz sinusoidal signal was applied to the 5.0V regulator with and without the LND1. Figure 7 shows the test conditions.

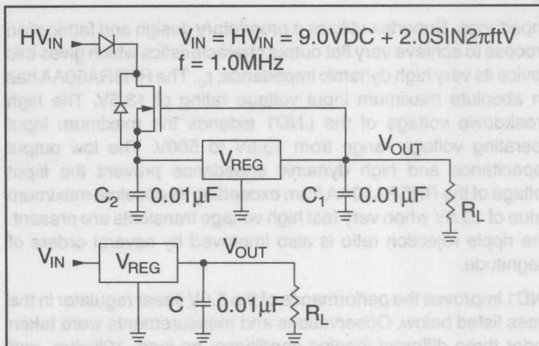


Figure 7: Ripple Rejection Test Conditions

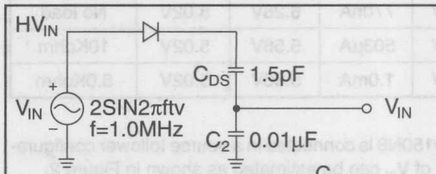
Measured results are as follows:

Peak-to-peak output AC voltage, $RR = 20\log\left|\frac{V_{OUT}}{4.0V}\right|$

V_{OUT} with LND1	V_{OUT} without LND1	Conditions
1.3mV, RR = -70dB	2.90V, RR = -2.8dB	No load
1.3mV, RR = -70dB	2.90V, RR = -2.8dB	10Kohm
1.3mV, RR = -70dB	2.90V, RR = -2.8dB	5.0Kohm

The amount of AC attenuation due to the LND1 can be estimated by the equivalent circuit and equations shown in Figure 8.

The ripple rejection ratio was improved by a factor of 1000. Such a high ripple rejection ratio is particularly useful for off-line applications. A typical 240VAC off-line application is shown in Figure 9a.



$$V_{IN} = \frac{C_{DS}}{C_{DS} + C_2} HV_{IN}$$

$$V_{IN} = \frac{1.5pF}{1.5pF + 0.01\mu F}(4.0V_{P-P})$$

$$V_{IN} = 600\mu V_{P-P}$$

Figure 8: Ripple Rejection Calculation

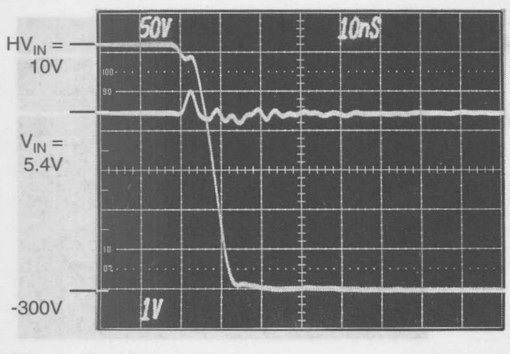


Figure 6a: HV_{IN} and V_{IN}

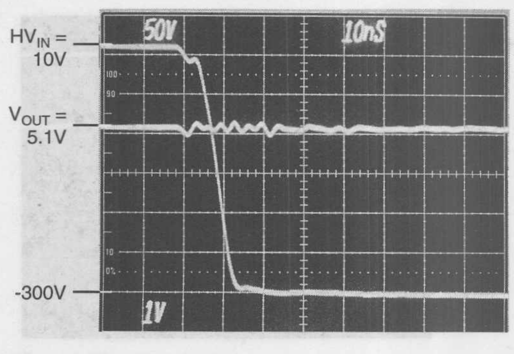


Figure 6b: HV_{IN} and V_{OUT}

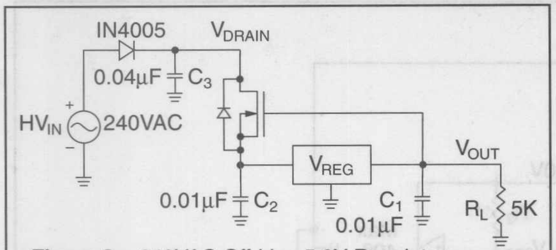


Figure 9a: 240VAC Off-Line 5.0V Regulator

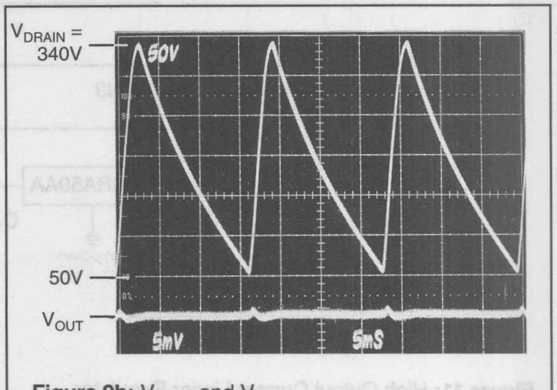


Figure 9b: V_{DRAIN} and V_{OUT}

Figure 9b shows the voltage waveforms at the drain, V_{DRAIN}, of the LND1 and the AC voltage at V_{OUT}. There were 290 Volts of AC ripple observed on V_{DRAIN} with less than 2.0millivolts of ripples on V_{OUT}.

C_3 is a high voltage holding capacitor. In order to minimize size and cost, more often than not it is desirable to select C_3 to be as small as possible. The high ripple rejection ratio helps in achieving a small size of C_3 because it allows for large AC input voltage with negligible AC output voltage.

Power-Up Transient Suppression

The circuits shown in Figures 10a and 10b are powered up from 0V to 10V in 100nsec. This test demonstrates the stability of the circuit, the amount of overshoot voltage on V_{OUT}, and the amount of time required for the output to settle. Large overshoot voltages on V_{OUT} may damage sensitive loads, such as CMOS circuits.

The test results were:

With LND1		Without LND1		Conditions
V_{PEAK}	t_r	V_{PEAK}	t_r	
0.0V	50µsec	7.6V	1.0µsec	No load
0.0V	60µsec	7.0V	1.0µsec	10Kohm
0.0V	80µsec	6.9V	1.0µsec	5.0Kohm

While there was a large overshoot voltage without the LND1, no overshoots were observed in the circuit employing the LND1. Loads prone to damage by overshoots can be effectively protected by using the LND1.

Conclusion

The high voltage protected, low power, 5.0V linear regulator in Figure 1 is a robust, compact, cost effective regulator. It can operate up to 500VDC, protect against ±500V transients, and has a maximum quiescent current of 1.0µamp. The electrical characteristics of the LND1 allow for the 500V operation and protection. Some examples are proximity controlled light switches, street lamp control, fax machines, modems, and power supplies for CMOS ICs in automotive, avionics and a variety of applications.

Other Application Ideas

The circuit in Figure 1 can be easily modified for higher current capability. The LND1 can be replaced by the Supertex DN2540N5, which is a 400V, 150mA depletion-mode MOSFET in a TO-220 package. In case the current is low and the worst case power dissipation for the DN25 is below 1Watt, the TO-92 version (part #DN2540N3) can be used to save space and cost. Figure 11 utilizes an op-amp and an enhancement-mode MOSFET for a much higher output current capability. Figure 12 is an off-line street lamp control where V_{SENSE} is the input voltage from a light sensing device.

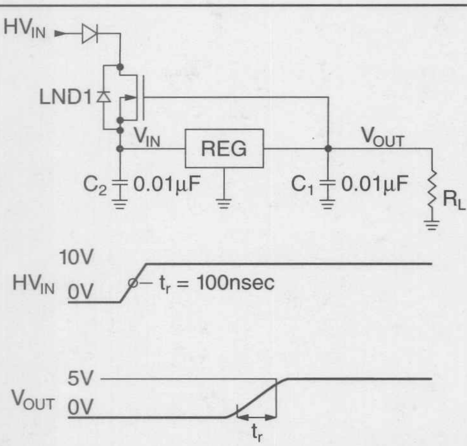


Figure 10a: Power Up Response with LND1

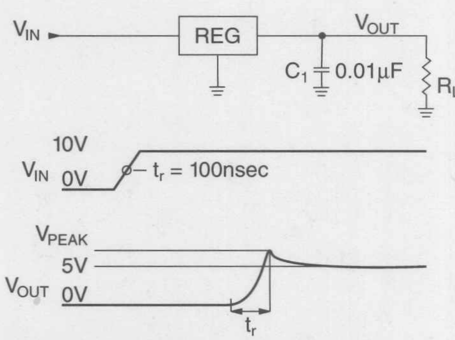


Figure 10b: Power Up Response without LND1

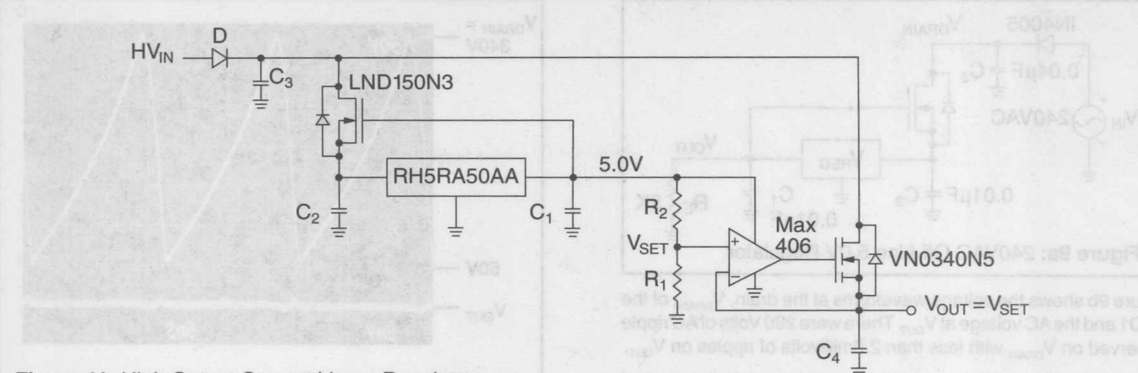


Figure 11: High Output Current Linear Regulator

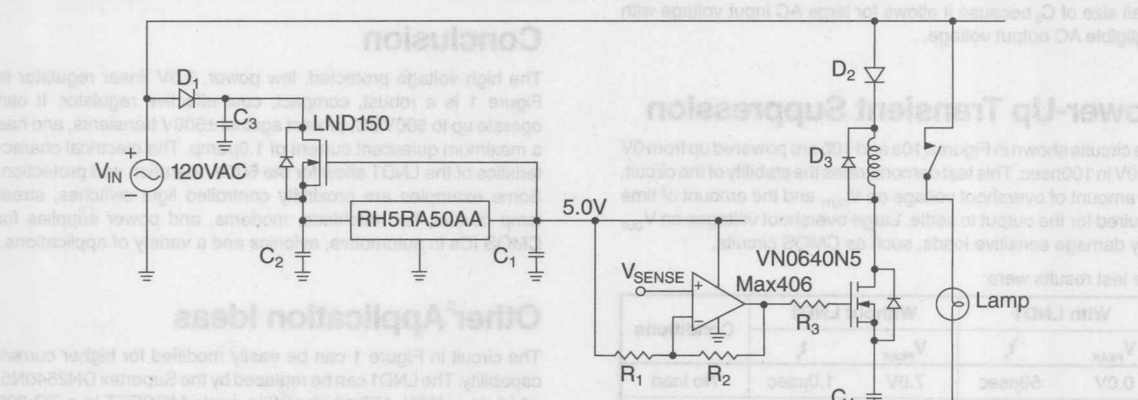
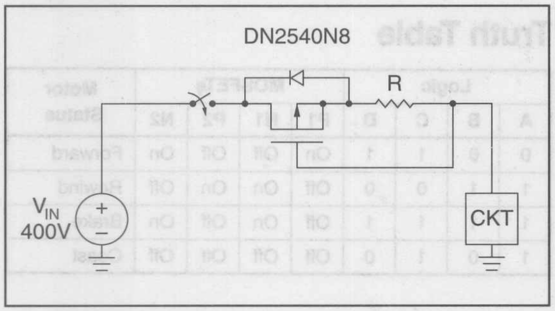


Figure 12: Off-Line Street Lamp Controller

Constant Current Sources and Depletion-Mode FETs

Depletion-mode MOSFETs can be used either as "normally closed" switches or current sources. This note shows circuits, utilizing depletion mode devices, that will benefit many applications. The main performance features of the circuits and examples of applications are listed. For more applications information on depletion mode MOSFETs, refer to other LND1 and DN25 series application notes.

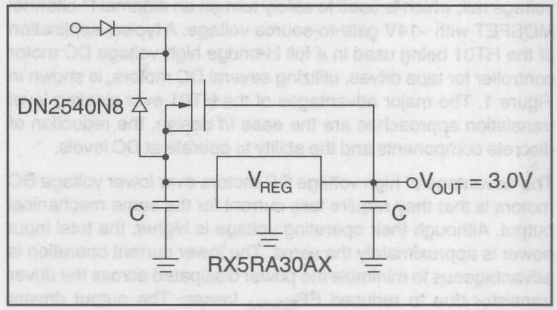
Current Surge Protection



- ☐ Current limit up to 150mA
- ☐ Back-to-back pair for bi-directional limiting

Inrush limiting for lamps/motors/capacitive loads, instrumentation, telecommunication

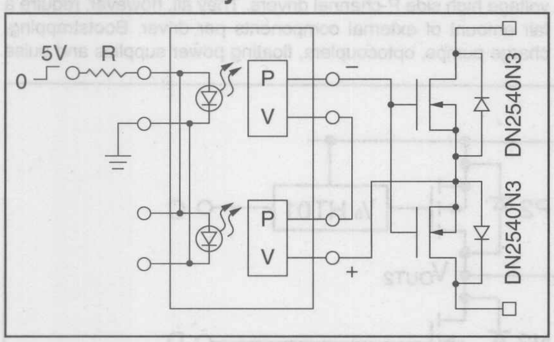
High Voltage Protected Regulator



- ☐ ±400V transient protection
- ☐ +5V to +400V operation
- ☐ Typically 800nA quiescent current

Telecommunication, automotive, fax machines, off-line control circuits

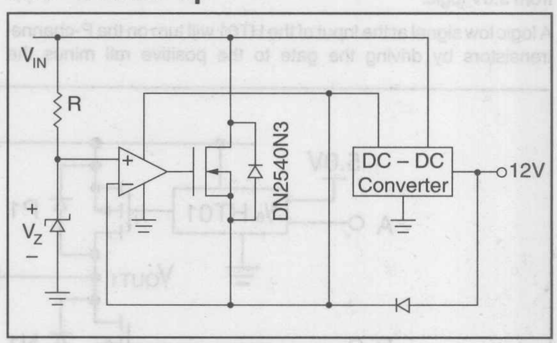
Solid State Relay



- ☐ Normally on
- ☐ ±400V blocking
- ☐ Low C_{IN} for fast switching

Telecommunication, instrumentation, fax machines, modems, data line diagnostics

SMPS Start-Up



- ☐ Off-line capability
- ☐ Switchable to save power
- ☐ Improves efficiency

Switchmode power supply

High Voltage Level Translator for Motor Drives

by Jimes Lei, Applications Engineer

Introduction

The Supertex HT0130 is a 300V 8-channel high voltage level translator designed to drive and control the gates of eight independent high voltage P-channel MOSFETs via low voltage CMOS logic control signals. A logic low on one of the inputs of the HT01 will cause the corresponding output to drop typically 14V below the high voltage rail, which is used to safely turn on an external P-channel MOSFET with –14V gate-to-source voltage. A typical application of the HT01 being used in a full H-bridge high voltage DC motor controller for tape drives, utilizing several DC motors, is shown in Figure 1. The major advantages of the HT01 over existing level translation approaches are the ease in design, the reduction of discrete components and the ability to operate at DC levels.

The advantage of high voltage DC motors over lower voltage DC motors is that they require less current for the same mechanical output. Although their operating voltage is higher, the total input power is approximately the same. The lower current operation is advantageous to minimize the power dissipated across the driver transistor due to reduced $I^2R_{DS(ON)}$ losses. The output drivers therefore need not have low on-resistance.

Circuit Description

The DC motor shown in Figure 1 is used for industrial tape drives. A full H-bridge configuration is required for bi-directional capability used for tape rewinding and forwarding. The full H-bridge consists of the Supertex TQ3001N6 low threshold complementary quad N- and P-channel MOSFETs operating from a 35V line. The N-channel transistors are low threshold MOSFETs and can be driven directly from 5.0V logic.

A logic low signal at the input of the HT01 will turn on the P-channel transistors by driving the gate to the positive rail minus the guaranteed clamp voltage of the device, V_{PP}–V_Z. The N-channel transistors are driven directly from the CMOS logic.

To forward wind the tape, P1 and N2 are on and P2 and N1 are off. To rewind, P2 and N1 are on and P1 and N2 are off. To brake, N1 and N2 are on and P1 and P2 are off. The logic truth table showing the different states is as follows:

Truth Table

Logic				MOSFETs				Motor Status
A	B	C	D	P1	N1	P2	N2	
0	0	1	1	On	Off	Off	On	Forward
1	1	0	0	Off	On	On	Off	Rewind
1	1	1	1	Off	On	Off	On	Brake
1	0	1	0	Off	Off	Off	Off	Coast

It is desirable to brake the motor during transitions between forwarding and rewinding. This will avoid stretching and possibly breaking the tape. Braking between transitions will also eliminate the possibility of having both transistors on the same leg "on," thereby shorting the V_{PP} line to ground creating high crossover current.

Advantages in Using the HT01

The designer can choose from many different techniques for high voltage high side P-channel drivers. They all, however, require a fair amount of external components per driver. Bootstrapping, charge pumps, optocouplers, floating power supplies and pulse

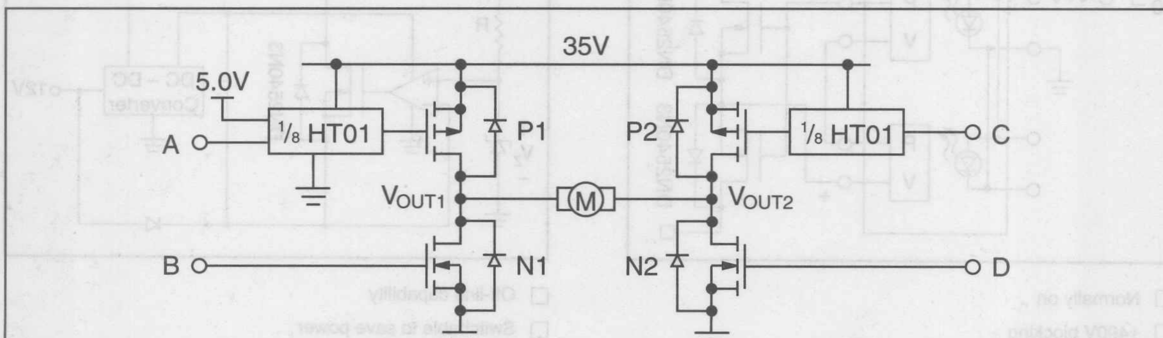


Figure 1: H-Bridge Motor Driver

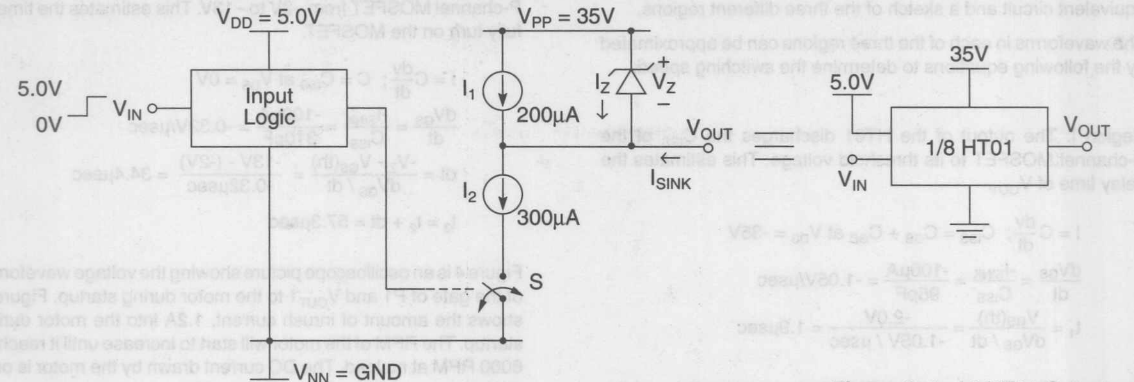


Figure 2: 1 of 8 HT01 Output

transformers are a few examples. The HT01, which is available in a single 20 pin DIP will drive eight independent P-channel MOSFETs with no external components required. Applications for this device include motor drivers, solenoid drivers, and high side DC switches. The HT01 will also operate with a DC input to keep the P-channel MOSFET continuously "on" as required in this application. Other techniques such as the use of bootstrapping capacitors and pulsed transformers cannot operate at DC because these schemes require periodic charging.

The HT01 is guaranteed to operate at logic levels from 4.75V to 15.0V, making it compatible with both TTL and CMOS logic. The outputs are designed with constant current sources that can sink and source 100µamps and 200µamps, respectively. The outputs can be easily paralleled for higher current capability. Output voltages will swing from V_{PP} to V_{PP}-V_Z where V_Z is guaranteed to be between 11V min and 17V max when V_{PP} is between 12V to 275V.

HT01 Output

The HT01 outputs are designed to drive capacitive loads. A simplified internal schematic of 1 of 8 HT01 output is shown in Figure 2. I_1 and I_2 are constant current sources. A logic low on V_{IN} will close switch S. I_2 will sink 300µamps to V_{NN} and is equal to $I_1+I_Z+I_{SINK}$. V_{OUT} is therefore discharged by I_{SINK} to V_{PP}–V_Z. A logic high on V_{IN} will open switch S. I_2 will have no current path to V_{NN} and therefore will appear effectively as a series resistor with the opened switch S. I_1 will charge V_{OUT} to V_{PP} with a constant current of 200µamps. As V_{OUT} charges close to V_{PP}, I_1 will effectively appear as a resistor between V_{OUT} and V_{PP}.

HT01 Switching Speed

The switching speed will depend on the input capacitance of the MOSFETs driving the motor. The following explains various factors to be considered in order to understand the charging and discharging requirements of the input capacitance. The calculated values are based on a single channel driving the P-channel MOSFET of the TQ3001N6. Faster switching speeds can be obtained by connecting multiple HT01 outputs in parallel.

During the forward mode, the HT01 will try to discharge the gate of P1 to V_{PP}–V_Z = 22V through a constant current sink of 100µamps. The gate-to-drain, C_{GD}, and gate-to-source, C_{GS}, capacitances will start to discharge to 22V. As the voltage on the gate reaches the threshold of the device, the device will start to turn on and the voltage on the drain will increase to V_{PP}. This will cause the voltage on the gate V_g to increase due to the capacitive coupling of C_{GD}. This results in a plateau on the gate of P1.

This additional discharging of C_{GD} is often referred to as Miller effect. Once V_{OUT1} reaches 35V, the gate will continue to discharge

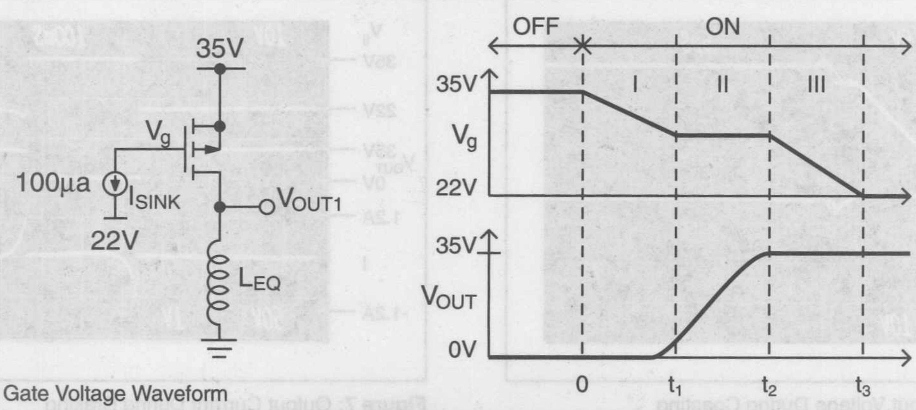


Figure 3: Gate Voltage Waveform

Region I: The output of the HT01 discharges the C_{ISS} of the P-channel MOSFET to its threshold voltage. This estimates the delay time of V_{OUT}.

$$I = C\frac{dv}{dt};\quad C_{ISS} = C_{GS} + C_{GD} \text{ at } V_{DS} = -35V$$

$$\frac{dV_{GS}}{dt} = \frac{-I_{SINK}}{C_{ISS}} = \frac{-100\mu A}{95pF} = -1.05V/\mu sec$$

$$t_1 = \frac{V_{GS}(th)}{dV_{GS} / dt} = \frac{-2.0V}{-1.05V / \mu sec} = 1.9\mu sec$$

Region II: The output of the HT02 discharges the C_{RSS} of the P-channel MOSFET by 35V. This estimates the rise time of V_{OUT}.

$$I = C\frac{dv}{dt};\quad C_{RSS} = C_{GD} \text{ at } V_{DS} = -35V \text{ to } 0V$$

$$dt = \frac{C_{RSS} \bullet dV}{-I_{SINK}} = \frac{(60pF)\,(-35V)}{-100\mu A} = 21\mu sec$$

$$t_2 = t_1 + dt = 22.9\mu sec$$

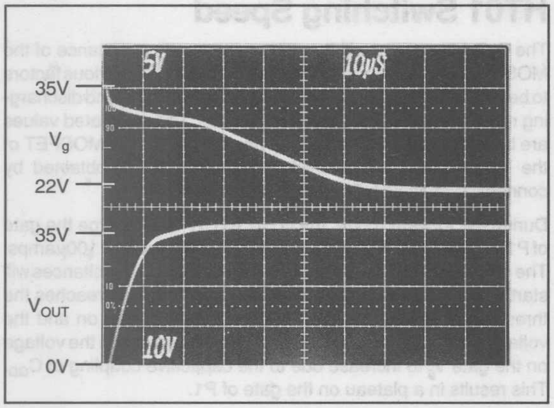


Figure 4: Output Voltage During Startup

$$I = C\frac{dv}{dt};\quad C = C_{ISS} \text{ at } V_{DS} = 0V$$

$$\frac{dV_{GS}}{dt} = \frac{-I_{SINK}}{C_{ISS}} = \frac{-100\mu A}{310pF} = -0.32V/\mu sec$$

$$dt = \frac{-V_Z - V_{GS}(th)}{dV_{GS} / dt} = \frac{-13V - (-2V)}{-0.32\mu sec} = 34.4\mu sec$$

$$t_3 = t_2 + dt = 57.3\mu sec$$

Figure 4 is an oscilloscope picture showing the voltage waveforms of the gate of P1 and $V_{OUT}1$ to the motor during startup. Figure 5 shows the amount of inrush current, 1.2A into the motor during startup. The RPM of the motor will start to increase until it reaches 6000 RPM at no load. The DC current drawn by the motor is only 11.0mA.

The continuous total power dissipation on the TQ3001N6 for a no load condition is $(11.0mA)^2 \bullet (1.5 + 2.0) = 424\mu W$. The total peak power dissipation is $(1.2A)^2 \bullet (1.5 + 2.0) = 5.04W$. The 1.2A peak is below the pulsed current rating of the TQ3001N6 which is 3.0A for both the N- and P-channels.

Figure 6 shows the gate of P1 and V_{OUT1} during turn-off. Because the back EMF holds V_{OUT1} to 35V, there is very little Miller effect on

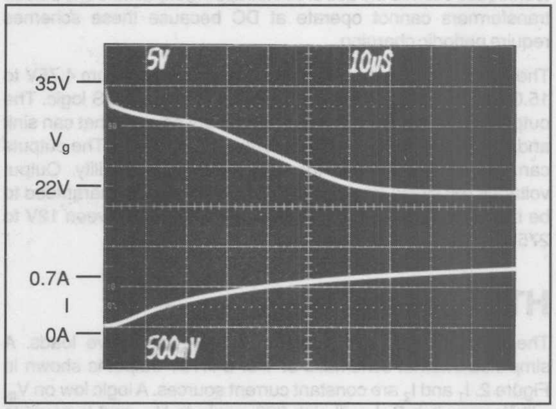


Figure 5: Peak Current During Startup

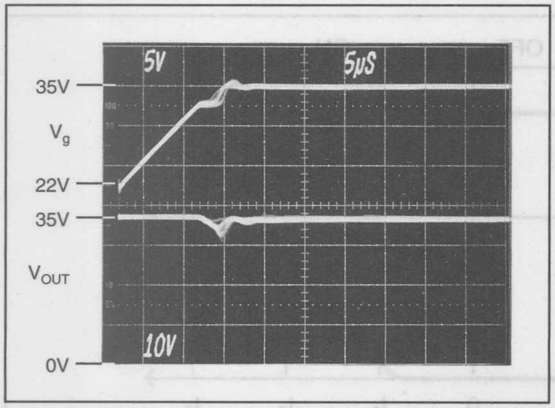


Figure 6: Output Voltage During Coasting

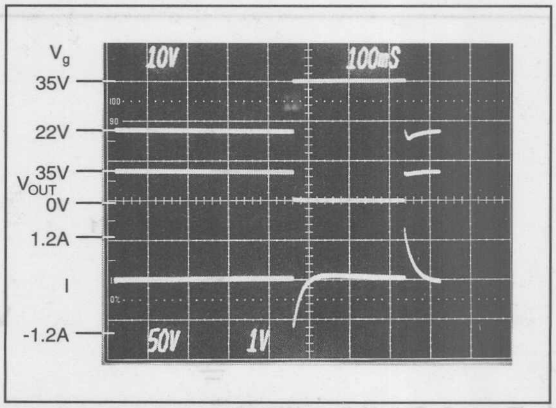


Figure 7: Output Current During Braking

the gate. The gate voltage plateaus for only 2 to 3µsec. Figure 7 shows the gates of P1 and N1 and the current through the motor when it is braking. Both N1 and N2 are on for 300ms discharging the energy stored in the motor to ground. The peak current measured was 1.2A.

Other Applications

The HT01 can also be used for solenoid drivers and high side switches for power management. Figure 8 is an example to show the ease of using the HT01 for multiple loads. It is being used as four separate high side switches and four separate solenoid drivers controlled by 5.0V logic signals.

Depending on the number of loads to be driven, one could use either an eight-channel array (e.g., Supertex part #AP0130NA or AP0132WG) or discrete MOSFETs (e.g., VP05, VP06, or VP03 products) available in various packages.

Conclusion

The HT01 simplifies gate driver designs on high voltage P-channel MOSFETs. Eight independent channels are available in a single 20 pin package. A considerable amount of board space can be saved as compared to discrete approaches. Its wide operating high voltage and logic voltage operating ranges allow for easy logic interfacing with high voltage P-channel driver applications up to 275V.

The outputs can be connected in parallel for faster switching speeds for the output MOSFET.

The HT01 can operate even when the control signal is held constant at a DC level, i.e., a static condition. It does not have the disadvantage of other capacitively or inductively coupled schemes, where the control signal has to vary with time.

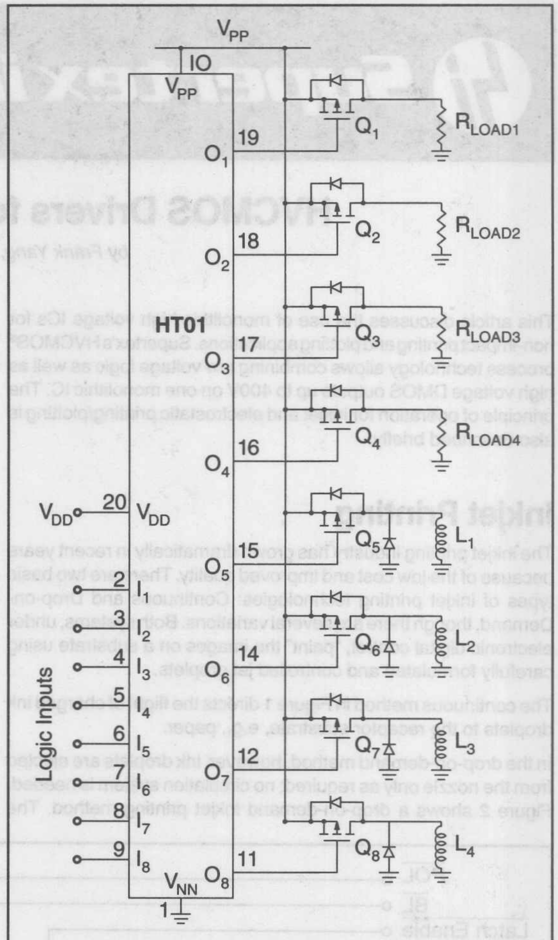


Figure 8: High Side Switches and Solenoid Drivers

HVCMOS Drivers for Non-Impact Printing

by Frank Yang, Applications Engineer

This article discusses the use of monolithic high voltage ICs for non-impact printing and plotting applications. Supertex's HVCMOS® process technology allows combining low voltage logic as well as high voltage DMOS outputs up to 400V on one monolithic IC. The principle of operation for inkjet and electrostatic printing/plotting is also described briefly.

Inkjet Printing

The inkjet printing industry has grown dramatically in recent years because of the low cost and improved quality. There are two basic types of inkjet printing technologies: Continuous and Drop-on-Demand, though there are several variations. Both systems, under electronic digital control, "paint" the images on a substrate using carefully formulated and controlled jet droplets.

The continuous method in Figure 1 directs the flight of charged ink droplets to the receptor substrate, e.g., paper.

In the drop-on-demand method, however, ink droplets are ejected from the nozzle only as required; no circulation system is needed. Figure 2 shows a drop-on-demand inkjet printing method. The expulsion of droplets from the nozzle is controlled by an internal change in pressure caused by a piezoelectric transducer.

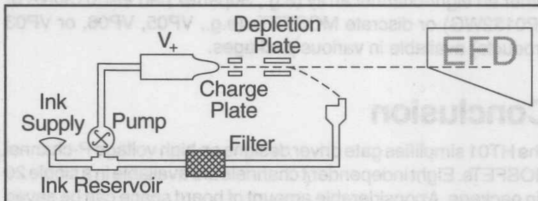


Figure 1: Continuous Method

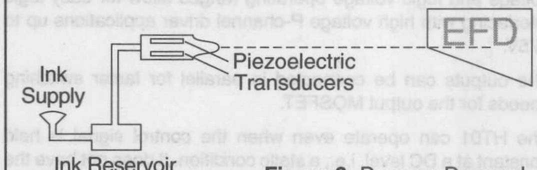


Figure 2: Drop-on-Demand

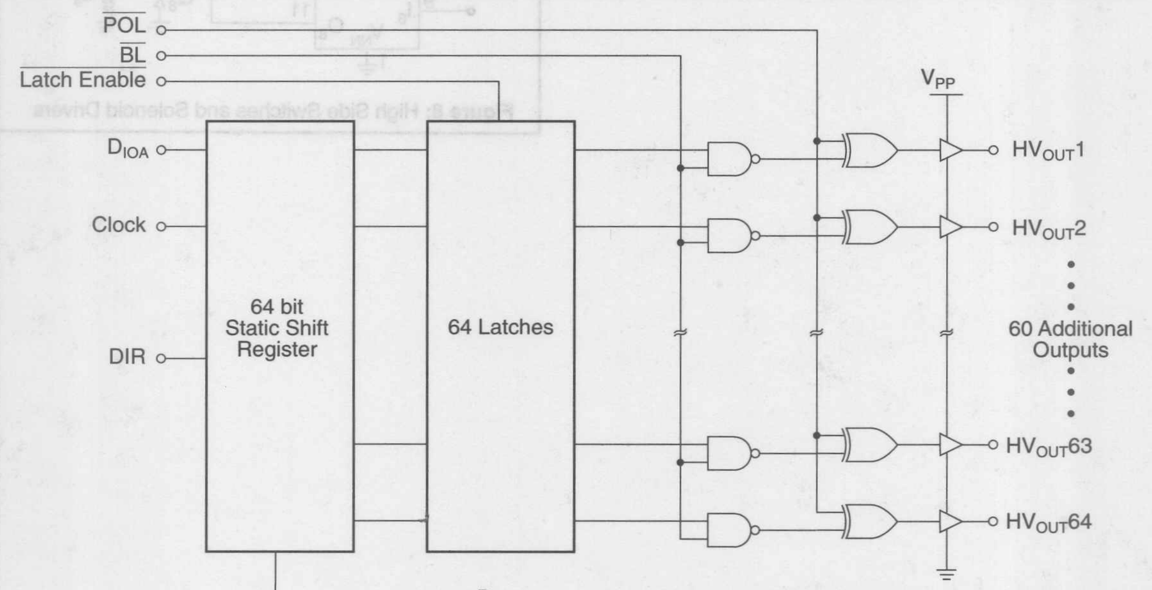


Figure 3: HV34 Functional Block Diagram

High Voltage Drivers for Inkjet Printers

Supertex HV34, which was designed for driving the deflection plates to control the path of charged ink particles, can help optimize performance and cost.

The HV34 is a low voltage serial input to high voltage parallel output converter with 64 push-pull outputs at up to 180V. Figure 3 shows a functional block diagram of the HV34. This device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of the data shift through the device. Data output buffers are provided for cascading multiple devices. The low voltage logic section of the HV34 can be operated either at a 5V or 12V logic supply voltage. The corresponding maximum data shift frequency possible with these logic supply voltages is 6Mhz or 12MHz respectively. The user can therefore choose the appropriate V_{DD} voltage to suit the application requirements.

Normally, the load on the outputs of the drivers is capacitive. Since the output has a true complementary MOS configuration, either the P-channel or N-channel MOSFET can be turned on at a time. When the output P-channel FET is turned on, the capacitive load starts to charge and its voltage increases until it reaches V_{PP}.

One can calculate how fast a certain value of the capacitive load can be charged up, as explained in the following example. Assuming the voltage on the load is at zero volt and a DC voltage of 100V is applied to the V_{PP} terminal of the IC. As soon as the P-channel transistor turns on, the load starts to charge up. Initially, the drain-to-source voltage is at maximum value, because V_{OUT} = 0V and $V_{DS} = V_{PP} - V_{OUT}$. This P-channel transistor operates in saturation and delivers maximum possible current to charge the capacitor. The dV/dt is calculated as

$$dV/dt = I/C$$

where I is the source current of the P-channel transistor and C is the load capacitance. Assuming a capacitive load of 1nF, the output source current of the HV34 is 5mA, so the dV/dt is

$$dV/dt = I/C = 5 \times 10^{-3}/1\times10^{-9}$$

$$= 5V/\mu s$$

Since the V_{PP} is at 100V, the time required to charge the load to 90% of the V_{PP} is $90\%V_{PP}$ / (dV/dt) = 18µs. The dV/dt to charge the load for the remaining 10% of the V_{PP} will be slower. This is due to decrease in the V_{DS} voltage of the P-channel transistor as the voltage on the load increases. The transistor finally gets out of saturation and operates in the linear region, thereby causing a reduction in the output current.

In the above example, the output of the IC was "hot switched." The term "hot switch" means that a high voltage DC supply is applied to device V_{PP} at all times even when the high voltage outputs are being switched. On the other hand, "cold switch" means that the high voltage supply is brought to a much lower voltage, sometimes to zero volt depending on the application, while the high voltage outputs are being switched. After switching the outputs, the high voltage supply is brought up to the desired voltage level.

Cold switching may be necessary on some ICs as this prevents possible damage to the device due to large crossover current during transition from the high-side transistor to the low-side transistor and vice versa. In a hot switching system, only a DC high voltage power supply is needed; this is simpler than the cold switch system where an extra high voltage switch or a high voltage ramp circuit is necessary.

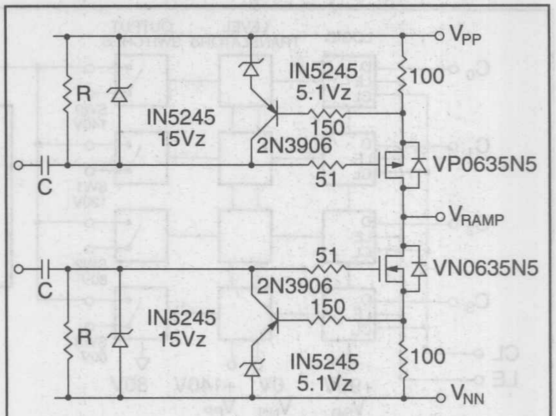


Figure 4: Ramp Generator

When the load connected to the output of the IC is very large, the risk of damage to the output transistors is not only from the crossover current but also because the safe operating area of the device may be exceeded. This risk is eliminated by ramping the V_{PP} which minimizes the drain-to-source voltage drop across the device by controlling the slew rate of the ramping voltage. Ramped high voltage supplies are not only less strenuous to the output of the ICs, but have the following additional advantages:

a. Lower power dissipation in the high voltage IC.

b. Reduced switching noise, which has several disadvantages, e.g., malfunction of logic, latch-up, etc.

The rise and fall time of the output voltage is determined by the output sink and source current of the device and the size of the load. The slew rate of ramp voltage can be designed to closely follow the rising load voltage to minimize the drain-to-source voltage drop. Figure 4 shows a typical ramp generator circuit.

The above circuit utilizes Supertex high voltage DMOS transistors VP0635N5 and VN0635N5. The T0-220 package was chosen to handle a large power dissipation. If the output current required is low, the T0-92 version of these parts, the VN0635N3 and VP0635N3, may be used to save component cost and board space. The 15V zener diodes provide extra protection for the gate of the DMOS transistors. The value of the R and C is chosen in such a way that the time constant of this RC is much greater than the output pulse width of the ramp generator. V_{NN} and V_{PP} are fixed voltages available from the system's main power supply. If a negative voltage is not needed, the V_{NN} can be kept at zero volt.

The input A and B are connected to 5V or 12V logic IC outputs. Care must be taken to ensure that either VP0635N5 or VN0635N5 is on at a time to avoid large crossover currents flowing through both transistors at the same time, which may cause catastrophic failure.

In applications where different V_{PP} voltages are required to be applied to the deflection plates, a Supertex HV1016P can be used to connect the V_{PP} pin of the IC to the appropriate high voltage. Figure 5 shows the block diagram of HV1016P , which is used to supply 4 different voltages to the V_{PP} of the HV34 by controlling the SW0, SW1, SW2 and SW3 turned-on time.

Piezoelectric transducers can also be driven by Supertex high voltage push-pull drivers. The high voltage output of the driver forces the interspace of the piezoelectric transducer to expand,

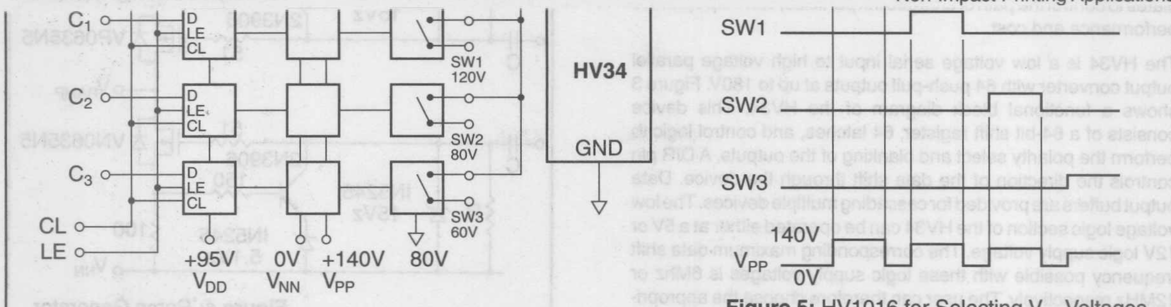


Figure 5: HV1016 for Selecting V_{PP} Voltages

thereby sucking liquid ink into the nozzle. Then, when a high voltage of reverse polarity is applied to the transducer while the nozzle is filled with ink, the ink will be expelled and deposited on the paper.

Electrostatic Printing/Plotting

The electrostatic method of printing/plotting is relatively new. Electrostatic printers and plotters produce images by converting vector data into raster data and applying dots to the medium. This allows them to lay down the image across the entire width of the media simultaneously and thus increase printing speed.

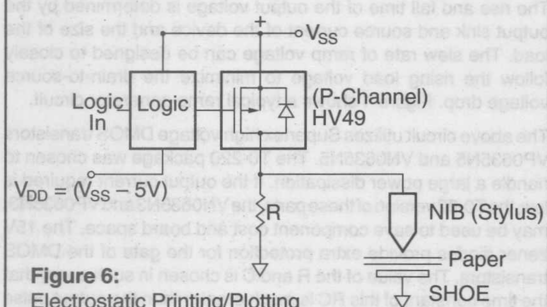


Figure 6:
Electrostatic Printing/Plotting
Open Drain Configuration

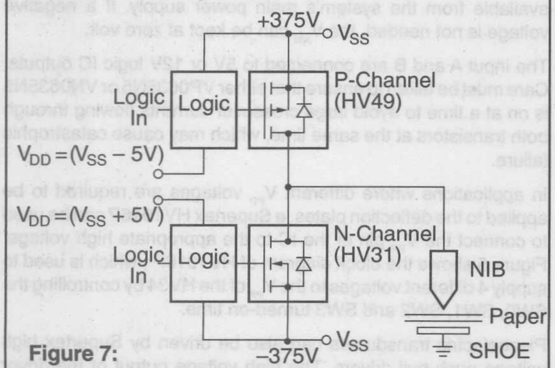


Figure 7:
Electrostatic Printing/Plotting
Push-Pull Configuration

The electrostatic printing/plotting process typically uses a toner and a paper that will hold charge. The paper is passed over the print head which contains a stylus array (NIB) that lays down negative charges on the paper. The higher the charge voltage across the paper (i.e., between the print head NIB and the SHOE), the better the image definition.

To implement electrostatic printing technology requires very high-voltage driver circuits for the stylus arrays either in an open drain configuration as shown in Figure 6 or, preferably in a push-pull configuration for better efficiency as shown in Figure 7. The current required, however, is relatively low, typically below 1mA.

High Voltage Drivers for Electrostatic Printer/Plotter HV31 and HV49

Supertex HV31 and HV49 are ideally suited for electrostatic printer/plotter applications.

The HV31 is a low voltage serial input to high voltage parallel output converter with 64 N-channel open-drain outputs with a 375V rating. Figure 8 shows a functional block diagram of the HV31. This device consists of a 64 bit shift register, 64 latches and logic control to perform the output enable function. A direction (DIR) pin controls the data shift through the device, which can be clockwise or counter-clockwise as desired. Since many devices are often used in one system, data output buffers are provided for cascading purposes.

The HV31 allows up to 6Mhz data shift frequency with logic supply voltage of 5 volts, which is convenient to interface with microcomputers directly without the need for voltage shifting circuits.

The HV49 is a high voltage open-drain P-channel device that can be operated up to -375V. The functional block diagram of the HV49 is the same as for HV31 except that the output section consists of open drain P-channel MOSFETs. Being a P-channel device, the polarity of all the voltages are reversed.

For high performance systems, a 375V push-pull configuration can be formed using the combination of the HV31 and HV49 (Figure 7). In this configuration, level shifting of the logic signal is required because the input logic voltages for both the HV31 and

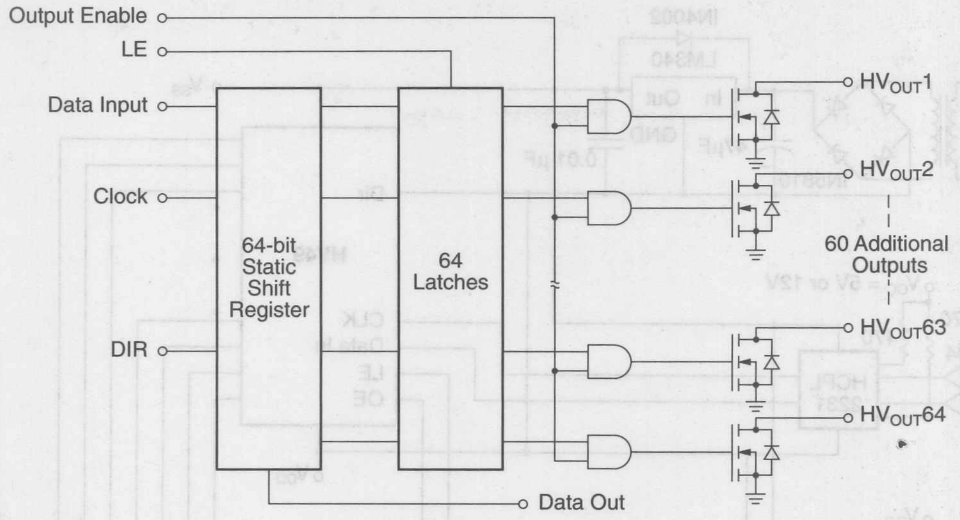


Figure 8: HV31 Functional Block Diagram

HV49 are referenced to V_{SS}. The circuit shown in Figure 9, utilizing opto-couplers, may be used to achieve the desired level shifting and isolation.

Assume that the logic input signals coming from the TTL logic to the opto-couplers are 0 to 5V. The power needed to run the opto-couplers is taken from the two floating power supplies. The logic signals coming out of the opto-couplers are referenced to the floating power supplies. The V_{SS} voltage normally is ramped, as discussed earlier, to minimize the voltage drop across the output transistor of the device. The two floating power supplies are formed by using a transformer, the primary winding of which is connected to the 120V AC utility power line. There are two secondary windings on the transformer; the outputs will be rectified by the bridge rectifiers and stabilized by LM340 linear regulators.

Since a very high voltage is used for electrostatic printers and plotters, arcing can occur between the NIB or stylus and the SHOE due to pin holes or cracks in the paper. High current during this arcing will be destructive to the driver IC, and adding circuitry for protection becomes necessary. Some protection for a short duration is afforded by the saturation current of the HV31 and HV49 , which typically is around 2 to 4mA . However this is really not adequate because considerable heat may be generated for durations longer than a few milliseconds. Current limiting resistors are required to lower the current further.

HV46 and HV55

In some applications such as electrostatic plotters where much higher current is desired, Supertex HV46 and HV55 can be used.

The HV46 offers 32 P-channel open drain outputs similar to the HV49. The output voltage and current of the HV46 is -300V and 60mA respectively. The HV55 is an 32 output, N-channel open drain device similar to the HV31, and has a 300V, 100mA rating.

These devices can be used in either an open drain (Figure 6) or, preferably, in a push-pull configuration (Figure 7). Short circuit protection by limiting the current will be necessary. The driving scheme for the HV49 and HV31 can also be used to drive these devices.

HV32

The HV32 offers 64 channel push-pull outputs with 250V rating. The uniqueness of this device is that the output current can be programmed by a resistor network and a reference voltage.

Figure 10 shows a functional block diagram and Figure 11 shows the bias circuit for programming the output sink and source current. R_{INT} is an internal resistor of 20Kohms, the Vx is an internal reference voltage of 1.3V. I_1 and I_2 are the source and sink current respectively. For example, if the V_{PP} is 200V, $V_{REF} = V_{PP} - 12V =$ 188V; and the current to be programmed is 100µA, R_1 will be calculated as

$$R_1 = [(V_{REF} - 1.3V)/100 \times 10^{-6}] - R_{INT}$$
$$= [(188-1.3)/100 \times 10^{-6}] - 20 \times 10^3$$
$$= 1.8 \text{ Mohm}$$

The similar calculation can be done for the sink current. For example, if a 100µA sink current is desired, R_2 is calculated as,

$$R_2 = [(V_{REF} - 1.3V)/100 \times 10^{-6}] - R_{INT}$$
$$= [(12V - 1.3V)/100 \times 10^{-6}] - 20 \times 10^3$$
$$= 87 \text{ Kohm}$$

The range for the programmed output currents is from 25µA to 250µA. Since the P_{CTL} and N_{CTL} are all common for 64 outputs, the sink and source current of each individual output cannot be programmed independently.

The output current programmability gives users the flexibility to drive different sizes of print heads. Only one resistor network is needed for programming the current for the whole integrated circuit.

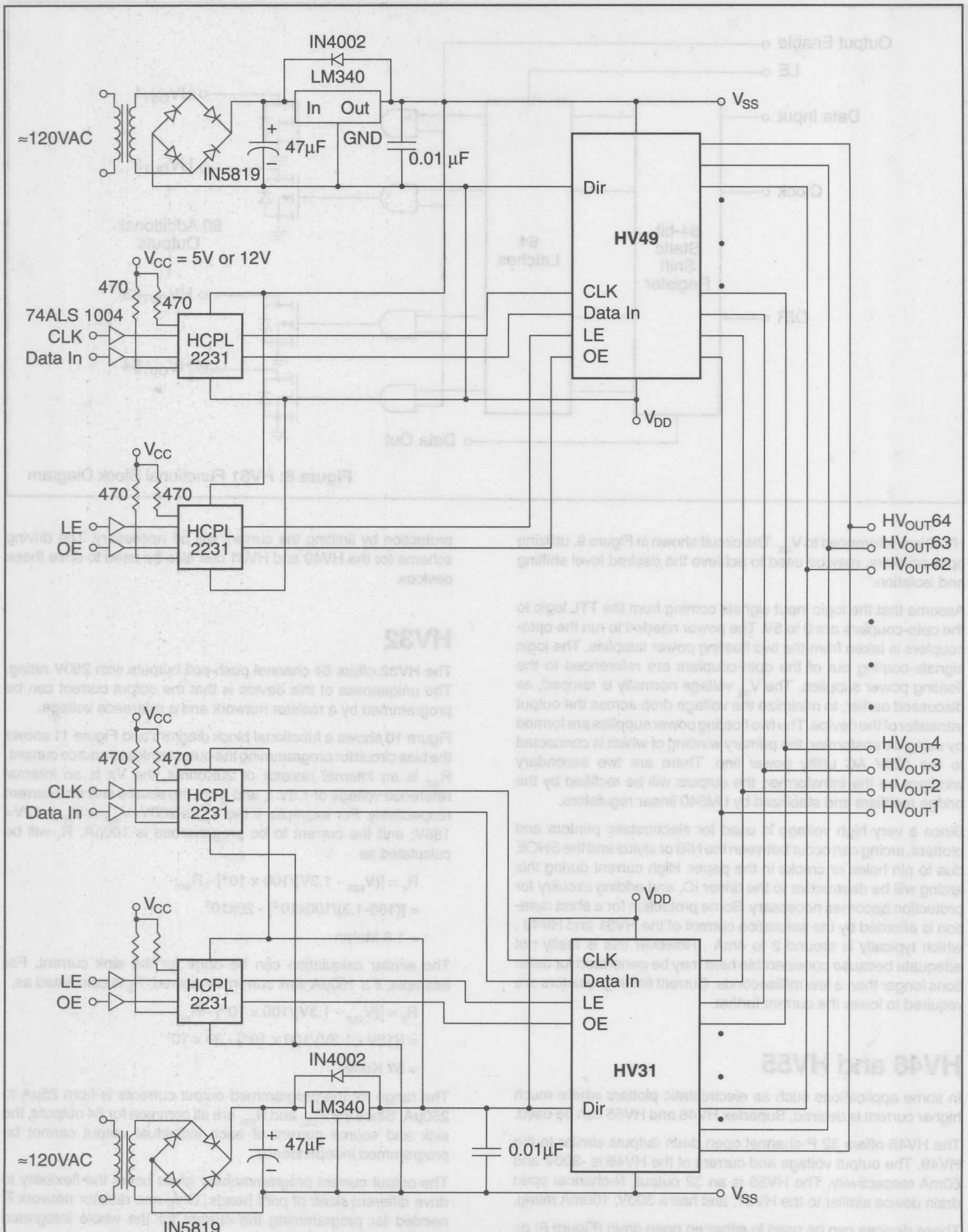


Figure 9: Level Translation using Opto-couplers

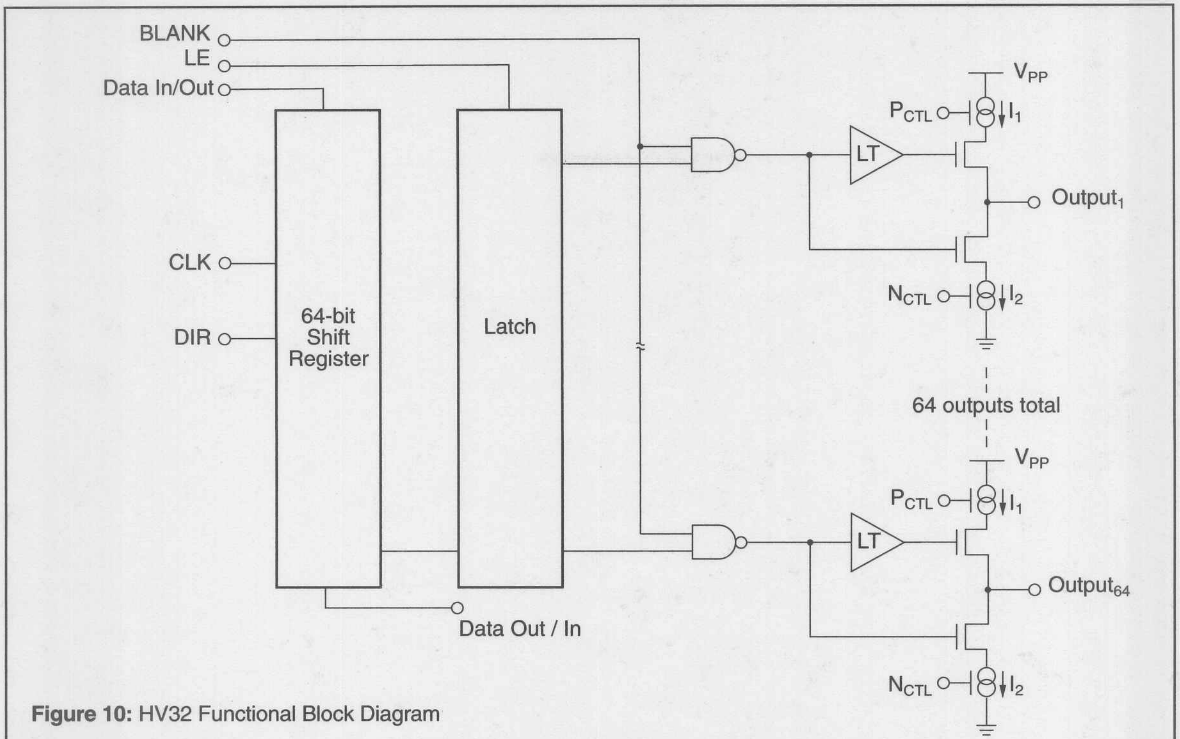
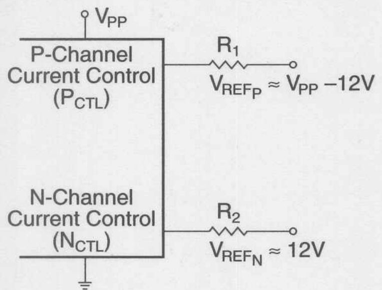


Figure 10: HV32 Functional Block Diagram



$$R_1 + R_{INT} = \frac{V_{REF_P} - V_{X1}}{I_1}$$

$$R_2 + R_{INT} = \frac{V_{REF_N} - V_{X2}}{I_2}$$

$V_X \approx 1.3V$ (Nominal)

$R_{INT} \approx 20K$ (Nominal)

Figure 11: Typical Current Programming Circuitry

Conclusion

Multichannel high voltage ICs provide practical solutions for driving printer/plotter heads utilizing inkjet and electrostatic technologies. High density solutions, which require a low unit area per output channel, save printed circuit board space and costs. The high voltage devices mentioned in this application note are also available in die form suitable for mounting the chips on circuit boards or “flip chip” on suitable substrates.

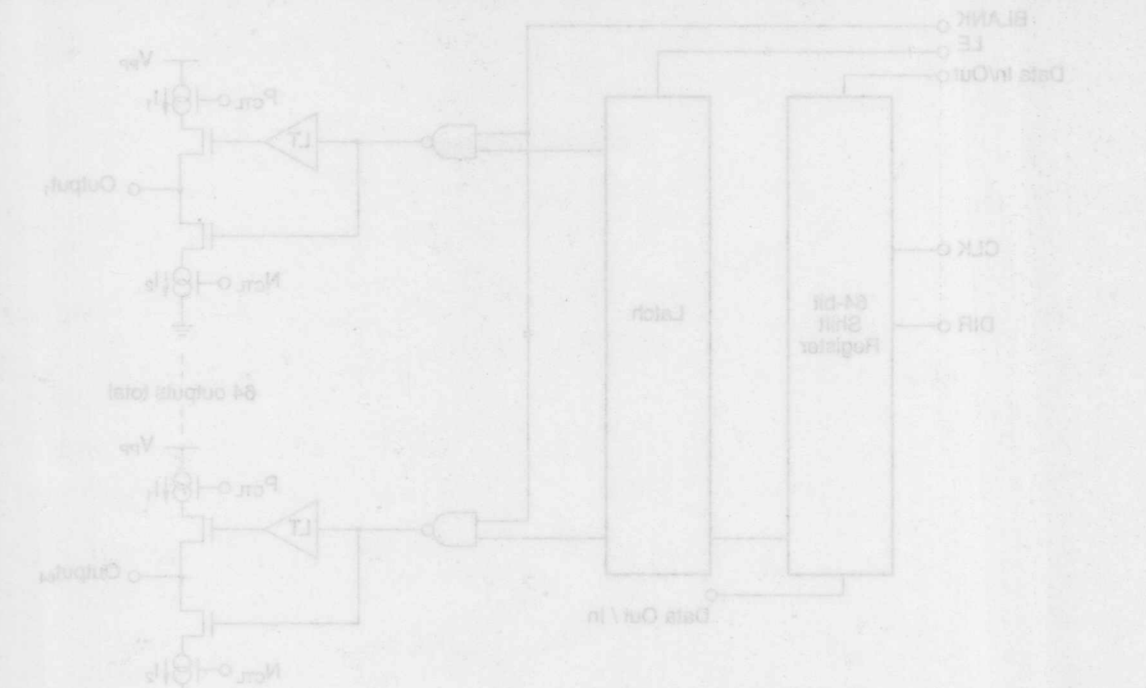


Figure 10: HV32 Functional Block Diagram

$$R_1 + R_{INT} = \frac{V_{REF_P} - V_{X1}}{I_1}$$

$$R_2 + R_{INT} = \frac{V_{REF_N} - V_{X2}}{I_2}$$

$V_X = 1.3V$ (Nominal)

$R_{INT} = 20K$ (Nominal)

Figure 11: Typical Current Programming Circuitry

Conclusion

Multichannel high voltage ICs provide practical solutions for driving printer/plotter heads utilizing inkjet and electrostatic technologies. High density solutions, which require a low unit area per output channel, save printed circuit board space and costs. The high voltage devices mentioned in this application note are also available in die form suitable for mounting the chips on circuit boards or "flip chip" on suitable substrates.

Supertex inc.

Static Handling and Testing Techniques For MOS Devices

4

CAUTION MUST BE USED WHEN HANDLING AND TESTING MOS DEVICES. STANDARD PROCEDURES SHOULD INCLUDE THE FOLLOWING TECHNIQUES IN ORDER TO AVOID POSSIBLE STATIC DAMAGE:

1. MOS devices must be stored in containers such as bags or tubes made of conductive and/or static dissipative material (DOD-HDBK-263).
2. The person handling the device should wear a wrist-strap grounded through a resistor of 1MΩ ±10%
3. Workstations should have grounded conductive mats over non-conducting surfaces.
4. All conductive surfaces and equipment must be connected to earth ground.
5. Rubber gloves, finger cots and clothing that are recommended to be worn by any person handling parts must be the type which does not generate electrostatic charges.
6. All parts should be handled by their packages and not by the leads.
7. Relative room humidity should be kept between 45 to 60% since static generation increases exponentially as humidity decreases.
8. Work, testing and storage areas should be mopped monthly with staticide solution or equivalent.
9. For further details refer to DOD Handbook 263 and DOD Standard 1686.

FOR YOUR CONVENIENCE, THE FOLLOWING IS A PARTIAL LIST OF COMPANIES THAT SUPPLY ANTISTATIC PRODUCTS:

3M Nuclear Products 3M Center St. Paul, MN 55101	Conductive Bags, Grounding Mats, Tote Bins and Other Material
Wescorp/DAL Industries, Inc. 1155 Terra Bella Ave. Mountain View, CA 94043	Wrist Straps
Biggam Enterprises, Inc. 2124 Bering Dr. San Jose, CA 95131	Wrist Straps, Staticide and Other Antistatic/Conductive Material
Free-Flow Packaging Corp. 2500 Middlefield Rd. Redwood City, CA 94063	Anti-Static Packaging Material
SpectraScan 1110A Elkton Dr. Colorado Springs, CO 80907	Static Control Monitors

Supertex inc.

Quality Assurance

The Management of Supertex, Inc. is committed to the continued enhancement of product excellence and service through the dynamics of its Reliability and Quality Assurance System, through the integrity of its people, and through the many professional disciplines engaged in new product development and process innovation.

It is the chartered responsibility of the Reliability and Quality Assurance Manager to oversee and ensure enforcement of Supertex's Quality System. A formal yearly review is undertaken to ensure continued development of a Quality System that maintains a competitive stance with the marketplace and meets customer requirements.

Primary Job Charter of the R & QA Departments

In-Process QC – The primary responsibilities of the Quality Control Department are to establish and maintain effective controls for monitoring manufacturing processes and equipment; to provide real time feedback of information concerning the state-of-control; and to initiate statistically valid techniques to further improve quality and reliability levels. This concept is used extensively in, but not limited to, the following major Quality Control functions:

- Incoming Raw Materials
- In-process Wafer Fabrication
- In-process Assembly

Quality Assurance (Standard and Hi-Reliability) – The primary responsibilities of the Quality Assurance Department are to assure that the delivered product meets workmanship standards imposed for standard or hi-reliability products and/or special customer requirements. This is accomplished through a program of process controls and gate inspections designed so that all devices are properly tested and sampled prior to shipment. Real time feedback, concerning control/inspection data, keeps all relevant personnel fully informed on the quality level of product going through final test operations. Major Quality Assurance functions include:

- Incoming Contract Subassemblies
- Outgoing Wafer Electrical and Visual Inspection
- Product Assurance Electrical Test
- Plant Clearance

Reliability – The primary responsibility of the Reliability function is to assure that a high and consistent level of product reliability is continually being produced. The Reliability Department establishes, defines and maintains evaluation programs to determine process/product reliability. Major Reliability activities include:

- Failure Analysis
- Hi-Reliability Program
- Process/Product Qualification
- New Product Design Evaluations
- Reliability Assurance Monitors

Document Control – The primary responsibilities of the Document Control department are to translate and format internal operating procedures and customer requirements into a system of regulatory written instructions. Document Control functions to ensure documentation integrity by establishing and maintaining procedures for:

- Initiating, revising, approving, distributing, recalling, and archiving documents.

Organization

The Manager of Quality Assurance/Quality Control reports directly to executive staff level of Management.

Reliability Assurance Management maintains a dual level of reporting; with direct report to the R & QA Manager for R & QA program coordination and by dotted line to the Product Vice President respective of product service for Reliability Assurance support.

It is the responsibility of the R & QA Manager to administer the planning, organization, execution, surveillance, appraisal, corrective action and documentation of Quality Programs. The character, responsibility and authority vested with the R & QA Manager will establish the means to attain the necessary quality and reliability objectives in all aspects of manufacturing within the accorded guidelines of this manual.

Quality programs administered by the R & QA Department support the following functions:

Operator Training – Supertex maintains a System of Operator Training and Qualification specific to the nature and complexity of each manufacturing operation, inspection, or test requirement. The basic training approach used by Supertex is supervised on-the-job training assisted by experienced/qualified personnel to provide a "buddy system" of training.

Training is typically performed with the same equipment and tools used in the normal manufacturing environment. The use of training aids, such as films, photographs and demonstrations of equipment and tools, is typical.

Each department manager is responsible for the training and evaluation of the workmanship performance to manufacturing norms.

The R & QA department maintains a system of audits/monitors for evaluating operator's adherence to specification and quality of workmanship.

Raw Material Procurement and Qualification – Supertex maintains a system that ensures economical control and conformance to detailed technical and quality requirements of purchased materials (direct and critical indirect). Material procurement is per-

formed through regulated specifications and drawings. R & QA functions within this system by providing the following services:

- Documented instructions for material evaluation, procedures, flow, workmanship standards, test methods and statistical sampling.
- Incoming inspection of raw materials.
- Identification and segregation of qualified and nonconforming material.
- Vendor qualification and ongoing vendor performance appraisal.
- Feedback of inspection results and informing suppliers of new design changes on raw materials.
- Formal review for disposition of nonconforming materials.

Equipment Calibration – Supertex maintains a Calibration System that ensures measurement accuracy of equipment used to determine product workmanship and acceptability.

The Calibration System conforms to MIL-STD-45662. Major provisions of the R & QA program are described as follows:

- Qualification of external calibration services.
- Traceability of references to National Institution of Standards and Technology. Identifications of measurement and test equipment (electrical, mechanical, and optical) for type and frequency of calibration.
- Document file certifying equipment calibration and recall history.
- Management report on recall status.
- R & QA audits of equipment calibration (date stickers and recall designation).

Manufacturing Flow, Inspection, and Test Points – Supertex maintains Flow Charts that describe the sequential steps of semiconductor processing and associated documentation for Wafer Fabrication, Assembly, and Post Assembly Finishing through Final Outgoing Plant Clearance. Flow charts are prepared for each product family and associated manufacturing technology.

Flow charts that delineate Fabrication processing are regarded as proprietary and are not available for external dissemination without prior approvals from the R & QA Manager and respective Product/Operations Vice President. Applicable Assembly Packaging Flow Charts are available upon request.

Flow charts for Customer Hi-Reliability Products are documented by a detailed lot traveler which defines all sequential operations, manufacturing inspection points, Customer Source Inspection points, and Quality Assurance product sample acceptance points.

In-Process Quality Control — Quality Control is a system of measurement and surveillance. The System is comprised of visual, dimensional, structural, and electrical characterization of material from incoming receipt of raw goods to outgoing finished product. Information obtained provides management with an overview on the state-of-the-process by specifically quantifying position of product yield, quality, and reliability.

Major elements found in Supertex's Quality Control Program are summarized by, but not limited to, the following:

- Environmental monitors (Airborne Particle counts, % RH and temperature).
- Routine Scanning Electron Micrography (SEM) of semiconductor devices.
- Specification compliance audits.
- Random monitor of wafers in-process.
- Electrostatic discharge prevention/monitor.
- Product lot sample qualification at critical manufacturing points.
- Wafer/die electrical sort monitor.
- Quality performance/trend data reporting.
- Return material analysis reporting.
- Monitoring of storage, handling, packaging, and identification of raw materials, of work-in-process, and of finished product.

Product Assurance Inspection – Supertex maintains a system of Product Qualification through inspection and test of finished product prior to customer shipment.

The Quality Assurance department provides inspection based on statistical sampling to ensure that outgoing product quality meets internal workmanship standards and customer procurement requirements.

The following process controls, inspections, tests, and documentation requirements are assured prior to submission of product to Customer Source Inspection and final Outgoing Plant Clearance:

- Test equipment correlation and qualification.
- Monitor manufacturing test operations.
- Ensure conformance of product lots to detailed customer test requirements (electrical, external visual, mechanical).
- Assure proper and complete documentation for each product lot, both in-process and at-plant clearance.

Reliability Assurance – At Supertex the Reliability Concept is introduced at the design phase of all new products. The factors that may affect product reliability are: compatibility of fabrication process, circuit layout and characteristics, assembly process, package materials, and application. Hence, Reliability Engineering is involved in evaluating all critical factors of reliability, starting with the design and first prototype functional circuit. From analysis, modification of design, wafer fabrication, and assembly, process changes can be implemented to enhance the reliability of the product. Approval is given for the release of new product to manufacturing only after the reliability of the product is established as acceptable within standard norms.

The Reliability Department provides the Product Group with a number of programs to define product reliability levels. Among these programs are: 1) Qualification, 2) Reliability, 3) Failure Analysis, and 4) Data Collection and Presentation.

Qualification Program of New Products and Processes

- Procedures for qualification of new product designs require Reliability participation and approval in design reviews, documentation, characterization, and reliability stress studies.
- New package qualification is approved and released for production by Reliability after prescribed environmental tests have been successfully completed.
- Qualification of a new product is granted only after Quality and Reliability have completed evaluation of process control studies. Significant modifications to existing processes are treated as new processes for the purpose of qualification.
- Proper documentation of all changes to process steps and procedure, and of any new or improved designs or material, is assured by Reliability's approval.

Reliability Monitor Programs

- Device and Package Reliability Monitor Programs are effected for all packages using a variety of device types to maximize data usefulness and to evaluate cost effectiveness of equipment.

but are not limited to, the following general tests, using the appropriate conditions specified in MIL-STD-883, Class B, Method 5005:

Condition	Method
Operating Life (HTRB)	1005
Steam Pressure (Molded packages)	N/A
Temperature Cycling	1010
Package Hermeticity	1014
Intermittent Opens (Molded package)	N/A
Salt Atmosphere (Initial Qual, only)	1009
Constant Acceleration	2001
Mechanical Shock (Initial Qual, only)	2002
Solderability	2003
Lead Integrity	2004
Vibration (Initial Qual, only)	2007
Biased Temperature Humidity (Molded packages)	N/A

- Accelerated Stress Monitor Programs are conducted to obtain timely feedback for process evaluations, as well as for ultimate device capability studies.

Failure Analysis

- It is the policy of Supertex to perform analysis of defective product and utilize the resulting findings to improve product yield and integrity.
- Reliability Engineering also performs failure analysis in mode and the mechanism of all failures (both from routine reliability tests and customer returns).

Failure Analysis Support Activities include:

- Qualification of existing products for new applications.
- Customer Qualifications. Reliability is responsible for review and acceptance of all customer requirements. When qualification programs or special testing is required, Reliability designs and implements appropriate test plans and coordinates with customer.
- Failure analysis, in support of In-Process Quality Control monitors, is handled by Reliability through Failure Report Requests. This support includes such services as visual inspection, metalography, thickness measurements, selective etching, and die probing.
- Customer's requests for failure analysis are filled by Reliability, which coordinates all replies to customers and approves all correspondence outside the Company.
- Where Reliability has determined that corrective action is necessary prior to the release of product for shipment, or to proceed further in production processing, a Corrective Action Request is generated by Reliability. No shipment may occur if the integrity of product reliability would be jeopardized.

Reporting and Publication of Data

Qualification test reports are prepared and distributed by Reliability for all certified products and processes which have been formally qualified and released for manufacturing.

Presently, the In-house Reliability Assurance testing is supplemented by testing done at outside Test Laboratories that have been approved by DESC for performing MIL-STD testing.

In addition, Reliability Assurance maintains a routine monitor of commercial grade finished product to evaluate reliability attributes against internally published norms. Products and packages are deliberately selected to represent typical characteristics and conditions of manufacturing – with the following considerations given:

- Design complexity and fabrication processing technology.
- Package type/assembly construction and materials.
- Assembly plant location.

Supertex reliability data for standard product is published for internal use. Specific reliability information is made available to customers upon request.

Plant Clearance Inspection – Supertex maintains a Final Outgoing Inspection on Finished assembled/tested product to ensure that all conditions of processing have been satisfied and that support documentation, as specified by contract, is maintained for each shipped lot.

Provisions for the control of shipped product during the Outgoing Plant Clearance Final Acceptance Program are structured to ensure product workmanship guarantees are met.

Summary

Supertex maintains R & QA Programs at critical operations to assure that products are manufactured under a documented and controlled system for consistency in workmanship standards (fit, form, function, and reliability).

The following Standards and Specifications have been integrated into Supertex's manufacturing operations and process control programs:

- FED-STD-209 — Clean Room and Work Station Requirements, Controlled Environments.
- DOD-HDBK-263 — Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment
- DOD-STD-1686 — Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment.
- MIL-M-38510 — Microcircuits, General Specification For.
- MIL-Q-9858 — Quality Program Requirements.
- MIL-I-45208 — Inspection Systems.
- MIL-S-19500 — Semiconductor Devices, General Specification For.
- MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes.
- MIL-STD-750 — Test Methods for Semiconductor Devices.
- MIL-STD-883 — Test Method and Procedures for Microelectronics.
- MIL-STD-202 — Test Methods for Electronic and Electrical Component Parts.
- MIL-STD-45662 — Calibration System Requirements.
- Special Customer Specifications

DMOS /HVCMOS Standard Product Flow

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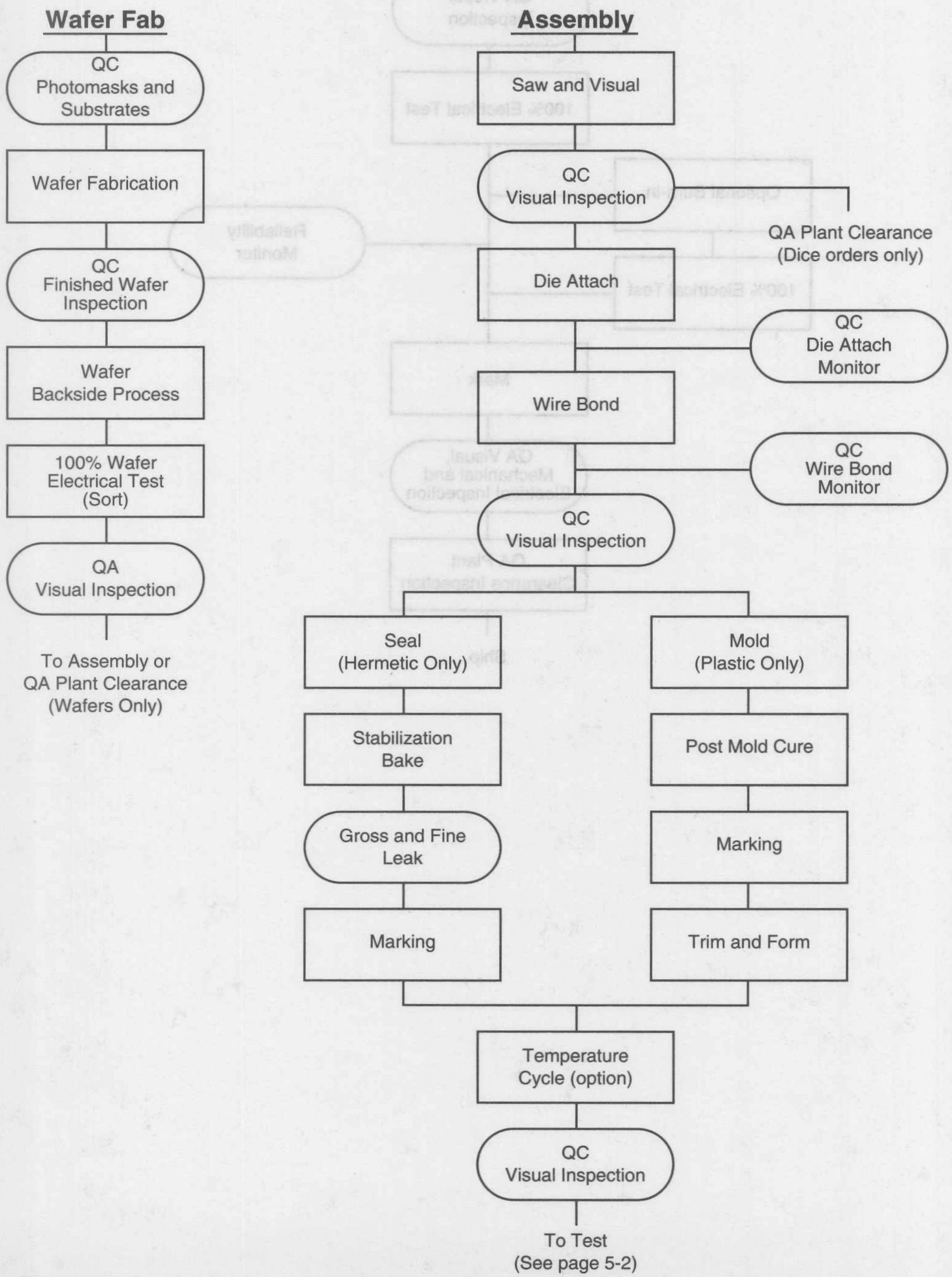
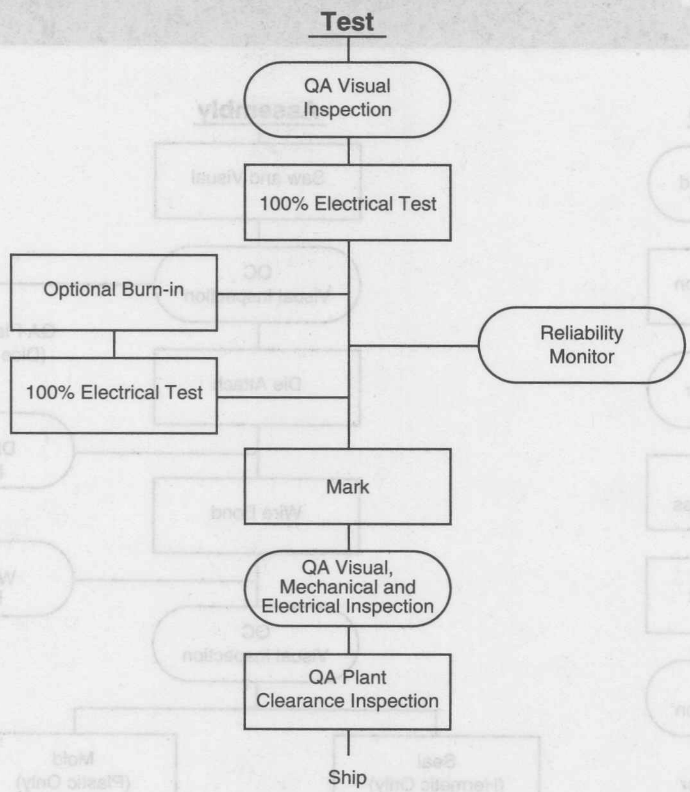


DMOS /HVCMOS Standard Product Flow



RB PRODUCT FLOW
(SIMILAR TO MIL-STD-883 CLASS B)

1. Preseal Visual
   Method 2010, Condition B
2. Stabilization Bake
   Method 1008, Condition C,
   24 Hrs. @ 150°C
3. Temperature Cycle (2)
   Method 1010, Condition C,
   10 Cycles, -65°C to + 150°C
   10 min. Minimum @
   Temperature Extremes
4. Constant Acceleration (2)
   Method 2001, Condition D/E,
   Y_1 Axis Only
   20,000 G for 24-40 LD PKGS
   30,000 G for 8-20 LD PKGS
5. Fine Leak (2)
   Method 1014, Condition A_1
   or B,
   5 x 10^{-8} atm cc/sec
6. Gross Leak (2)
   Method 1014, Condition C1
7. Trim and Mark (4)
8. External Visual
9. Electrical Test (4)
   100% Go/No-Go,
   Static and Functional
   Tests @ Max Rated
   Temperature
10. Dynamic/HTRB Burn-in
    Method 1015, Condition C,
    160 Hrs. @ 125°C
11. Electrical Test
    100% Go/No-Go
    Static Dynamic and
    Functional Tests @ 25°C
12. Electrical Test
    100% Go/No-Go
    Static and Functional
    Tests @ Max. Rated
    Temperature
13. Group A
    25°C Tests LTPD2
    Max. Rated Temp LTPD2
    Min. Rated Temp LTPD2
14. Group B Sample (3)
    Per MIL-STD-883

RC PRODUCT FLOW

1. Preseal Visual
   Method 2010, Condition B
2. Stabilization Bake
   Method 1008, Condition C,
   24 Hrs. @ 150°C
3. Temperature Cycle (2)
   Method 1010, Condition C,
   10 Cycles, -65°C to + 150°C
   10 min. Minimum @
   Temperature Extremes
4. Constant Acceleration (2)
   Method 2001, Condition D/E,
   Y_1 Axis Only
   20,000 G for 24-40 LD PKGS
   30,000 G for 8-20 LD PKGS
5. Fine Leak (2)
   Method 1014, Condition A_1
   or B,
   5 x 10^{-8} atm cc/sec
6. Gross Leak (2)
   Method 1014, Condition C1
7. Trim and Mark (4)
8. External Visual
9. Electrical Test (4)
   100% Go/No-Go,
   Static and Functional
   Tests @ Max Rated
   Temperature
10. Group A
    25°C Tests LTPD2
    Max. Rated Temp LTPD2
    Min. Rated Temp LTPD2
11. Group B Sample (5)
    Per MIL-STD-883

COMMERICAL PRODUCT FLOW

1. Preseal Visual
   Supertex Standard
2. Stabilization Bake
   Method 1008, Condition C,
   24 Hrs. @ 150°C
3. Fine Leak 1% AQL (2)
   Method 1014, Condition A_1
   or B,
   5 x 10^{-8} atm cc/sec
4. Gross Leak 1% AQL (2)
   Method 1014, Condition C1
5. Trim and Mark
6. External Visual
7. Optional Electrical Test
   100% Go/No-Go,
   Static and Functional
   Tests @ Max. Rated
   Temperature
8. Optional HTRB or
   Dynamic Burn-in
   Method 1015, Condition A
   or C,
   48 Hrs. @ 125°C
9. Electrical Test
   100% Go/No-Go
   Static and Functional
   Tests @ Max. Rated
   Temperature
10. Group A
    25°C Tests 0.65% AQL

Note 1: Processing consists of 100% screening and Group A. Generic group B, C and D data available on request.
Note 2: Hermetic packages only.
Note 3: Group C & D periodic lot sampling per MIL-STD-883.
Note 4: As required.
Note 5: No group C & D

All test methods are per MIL-STD-883 unless specified otherwise.

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DMOS Process Option Flow Chart

DMOS ARRAY RB FLOW[1] (SIMILAR TO MIL-STD-883 CLASS B)	SX FLOW (SIMILAR TO JAN TX) SXV FLOW[1] (SIMILAR TO JAN TXV) MIL-STD-750	SJ FLOW (SIMILAR TO JAN) MIL-STD-750	COMMERICAL BURN-IN SC FLOW MIL-STD-750	STANDARD PRODUCTS MIL-STD-750
Preseal Visual Method 2010, Condition B	Preseal Visual (6) Method 2072			
Stabilization Bake Method 1008, Condition C, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C	Stabilization Bake Method 1032, 24 Hrs. @ 150°C
Temperature Cycle Method 1010, Condition C, 10 Cycles, -65°C to +150°C 10 minutes minimum @ each temperature extreme	Temperature Cycle Method 1051 20 Cycles, -65°C to + 150°C 15 minutes minimum @ each temperature extreme			
Constant Acceleration (2) Method 2001, Condition E, Y_1 Axis Only -20,000 G	Constant Acceleration (2) Method 2006 Y_1 Axis only. TO-3 – 10,000 G, Others – 20,000 G			
Fine Leak (2) Method 1014, Condition A or B, 5 x 10^{-8} atm cc/sec	Fine Leak (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 – 5 x 10^{-7} atm cc/sec Others – 5 x 10^{-8} atm cc/sec	Fine Leak 1% AQL (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 = Cond. G 5 x 10^{-7} atm cc/sec Cond. H 1 x 10^{-7} atm cc/sec Others = 5 x 10^{-8} atm cc/sec	Fine Leak 1% AQL (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 = Cond. G 5 x 10^{-7} atm cc/sec Cond. H 1 x 10^{-7} atm cc/sec Others = 5 x 10^{-8} atm cc/sec	Fine Leak 1% AQL (2) Method 1071, Condition G or H, Maximum Leak Rate TO-3 = Cond. G 5 x 10^{-7} atm cc/sec Cond. H 1 x 10^{-7} atm cc/sec Others = 5 x 10^{-8} atm cc/sec
Gross Leak (2) Method 1014, Condition C_1	Gross Leak (2) Method 1071, Condition C	Gross Leak (2) Method 1071, Condition C	Gross Leak (2) Method 1071, Condition C	Gross Leak (2) Method 1071, Condition C
Electrical Test 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test (4) 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go, 25°C D.C. Parameters	Electrical Test 100% Go/No-Go, 25°C D.C. Parameters
HTRGB Burn-in (5) Method 1015, Condition A, 48 Hrs. @ 150°C	HTRGB Burn-in (3) Method 1042, Condition B, 48 Hrs. @ 150°C			
Electrical Test (5) 100% Go/No-Go 25°C D.C. Parameters	Electrical Test (4) 100% Go/No-Go, 25°C D.C. Parameters			
HTRB Burn-in Method 1015, Condition A, 80 Hrs. @ 150°C	HTRB Burn-in Method 1042, Condition A, 160 ±8 Hrs. @ 150°C		HTRB Burn-in Method 1042, Condition A, 96 Hrs. @ 150°C	
Electrical Test (Post burn-in) 100% Go/No-Go 25°C D.C. Parameters	Electrical Test (4) 100% Go/No-Go, 25°C D.C. Parameters		Electrical Test 100% Go/No-Go 25°C D.C. Parameters	
	Electrical Test 100% Go/No-Go, Group A, Subgroup 2			
Group A Subgroup 1 VIS/MEC, LTPD 5, Subgroup 2 D.C. @ 25°C LTPD 2, Subgroup 3 D.C. Min./Max. Temperature, LTPD 2, Subgroup 4 A.C. LTPD 2	Group A Subgroup 1 VIS/MEC, LTPD 5, Subgroup 2 D.C. @ 25°C LTPD2, Subgroup 3 D.C. Min./Max. Temperature, LTPD 2, Subgroup 4 A.C. LTPD2	Group A Subgroup 1 VIS/MEC, LTPD 5 Subgroup 2 D.C. @ 25°C, LTPD 2, Subgroup 3 D.C. Min./Max. Temperature, LTPD 2, Subgroup 4 A.C. LTPD 2	Group A Subgroup 1 VIS/MEC, LTPD 5, Subgroup 2 D.C. @ 25°C LTPD 5	Group A Subgroup A 0.65% AQL Subgroup 1 VIS/MEC, Subgroup 2 D.C. @ 25°C

Note 1: Processing consists of 100% screening and Group A only. Generic Group B, C, & D data available on request.
Note 2: Hermetic packages only.
Note 3: HTRGB-High temperature reverse gate bias.
Note 4: Read and Record with delta and percent values is optional.
Note 5: Optional.
Note 6: Preseal visual for SXV flow only. Not applicable for SX flow
All test methods are per MIL-STD-750 unless specified otherwise.

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DMOS High Reliability Products

The following products are available with High Reliability processing per test methods and flows of MIL-STD-750 and MIL-STD-883. For ordering purposes, add the process flow prefix to the device number as shown in the following examples:

Process Flow	Device Type	High Rel Part Number
SX	VN0104N2	SXVN0104N2
RB	VN0106N7	RBVN0106N7

Device Type	RB	SX	SXV	SJ	SC
2N6659		•	•	•	•
2N6660		•	•	•	•
2N6661		•	•	•	•
TN0102N2		•	•	•	•
TN0104N2		•	•	•	•
TN0106N2		•	•	•	•
TN0110N2		•	•	•	•
TN0520N2		•	•	•	•
TN0524N2		•	•	•	•
TN0602N2		•	•	•	•
TN0604N2		•	•	•	•
TN0606N2		•	•	•	•
TN0606N7	•				
TN0610N2		•	•	•	•
TN0620N2		•	•	•	•
TN0624N2		•	•	•	•
TP0102N2		•	•	•	•
TP0104N2		•	•	•	•
TP0602N2		•	•	•	•
TP0604N2		•	•	•	•
TP0606N2		•	•	•	•
TP0606N7	•				
TP0610N2		•	•	•	•
TP0616N2		•	•	•	•
TP0620N2		•	•	•	•
TQ3001N7	•				
VC0106N7	•				
VN0104N2		•	•	•	•
VN0104N7	•				
VN0104N9		•	•	•	•
VN0106N2		•	•	•	•
VN0106N7	•				
VN0106N9		•	•	•	•

Device Type	RB	SX	SXV	SJ	SC
VN0109N2		•	•	•	•
VN0109N9		•	•	•	•
VN0116N2		•	•	•	•
VN0120N2		•	•	•	•
VN0335N1		•	•	•	•
VN0335N2		•	•	•	•
VN0340N1		•	•	•	•
VN0340N2		•	•	•	•
VN0345N1		•	•	•	•
VN0345N2		•	•	•	•
VN0350N1		•	•	•	•
VN0350N2		•	•	•	•
VN0300B		Refer to TN0604N2			
VN0535N2		•	•	•	•
VN0540N2		•	•	•	•
VN0545N2		•	•	•	•
VN0550N2		•	•	•	•
VN0635N2		•	•	•	•
VN0640N2		•	•	•	•
VN0645N2		•	•	•	•
VN0650N2		•	•	•	•
VN10KN9		•	•	•	•
VN1106N2		•	•	•	•
VN1110N2		•	•	•	•
VN1116N2		•	•	•	•
VN1120N2		•	•	•	•
VN1204N2		•	•	•	•
VN1206N2		•	•	•	•
VN1210N2		•	•	•	•
VN1216N2		•	•	•	•
VN1220N2		•	•	•	•
VN1206B		Refer to TN0620N2			
VN1210B		Refer to TN0620N2			

DMOS High Reliability Products

Device type	RB	SX	SXV	SJ	SC
VN1304N2		•	•	•	•
VN1306N2		•	•	•	•
VN1310N2		•	•	•	•
VN1706B	Refer to TN0620N2				
VN1710B	Refer to TN0620N2				
VN2106NF	•				
VN2110NF	•				
VP0104N2		•	•	•	•
VP0104N7	•				
VP0104N9		•	•	•	•
VP0106N2		•	•	•	•
VP0106N7	•				
VP0106N9		•	•	•	•
VP0109N2		•	•	•	•
VP0109N9		•	•	•	•
VP0116N2		•	•	•	•
VP0120N2		•	•	•	•
VP0335N1		•	•	•	•
VP0335N2		•	•	•	•
VP0340N1		•	•	•	•
VP0340N2		•	•	•	•
VP0345N1		•	•	•	•
VP0345N2		•	•	•	•
VP0350N1		•	•	•	•
VP0350N2		•	•	•	•
VP0300B	Refer to TP0604N2				
VP0535N2		•	•	•	•

Device Type	RB	SX	SXV	SJ	SC
VP0540N2		•	•	•	•
VP0545N2		•	•	•	•
VP0550N2		•	•	•	•
VP0635N2		•	•	•	•
VP0640N2		•	•	•	•
VP0645N2		•	•	•	•
VP0650N2		•	•	•	•
VP0808B	Refer to TP0610N2				
VP1008B	Refer to TP0610N2				
VP1106N2		•	•	•	•
VP1110N2		•	•	•	•
VP1116N2		•	•	•	•
VP1120N2		•	•	•	•
VP1204N2		•	•	•	•
VP1206N2		•	•	•	•
VP1210N2		•	•	•	•
VP1216N2		•	•	•	•
VP1220N2		•	•	•	•
VP1304N2		•	•	•	•
VP1306N2		•	•	•	•
VP1310N2		•	•	•	•
VQ1000N7	•				
VQ1001P	•				
VQ1004P	•				
VQ2001P	•				
VQ2006P	•				
VQ3001N7	•				
VQ7254N7	•				

Chapter 6 – Selector Guides and Cross Reference

6

N-Channel Low Threshold Enhancement-Mode MOSFETs

Device Family	BV_{DSS} Min(V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min(A)	C_{ISS} Typ(pf)	$V_{GS(th)}$ Max(V)	Package Options TO-39	TO-92	TO-220	SOT89	Quad[1]	Die
TN01L	20, 40	1.8	2.0	45	1.6	•	•		•		•
TN01A	60, 100	3.0	2.0	50	1.6	•	•				•
TN05C	200, 240	10.0	0.3	45	1.5	•	•				•
TN05D	350, 400	22.0	0.25	48	2.0		•				•
TN06L	20, 40	0.75	4.0	100	1.6	•	•			•	•
TN06A	60, 100	1.50	3.0	100	1.6	•	•	•		•	•
TN06C	200, 240	6.0	1.0	110	1.6	•	•	•			•
TN06D	350, 400	10.0	1.0	105	1.8		•				•
TN07L	20	1.3	0.5	130	1.0		•				•
TN25L	20, 40	1.0	4.0	100	1.6				•		•
TN25A	60, 100	1.5	3.0	100	1.6				•		•
TN25C	200, 240	6.0	1.0	110	2.0				•		•
TN25D	350, 400	12.0	1.0	105	1.8				•		•
TN25U	18	2.5	0.25	110	0.8				•		•
TN26D	350, 400	5.0	2.0		2.0		•				•

Note: 1. Refer to Arrays and Special Functions section for packages available.

P-Channel Low Threshold Enhancement-Mode MOSFETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	$V_{GS(th)}$ Max (V)	Package Options TO-39	TO-92	TO-220	SOT89	Quad[1]	Die
LP07	-16.5	1.5	-1.2	120	-1.0		•				•
TP01L	-20, -40	4.0	-0.85	45	-2.4	•	•		•		•
TP06L	-20, -40	2.0	-2.0	100	-2.4	•	•			•	•
TP06A	-60, -100	3.5	-1.5	100	-2.4	•	•	•		•	•
TP06C	-160, -200	12.0	-0.75	100	-2.4	•	•	•			•
TP25L	-20, -40	2.0	-2.0	100	-2.4				•		•
TP25A	-60, -100	3.5	-1.5	100	-2.4				•		•
TP25C	-160, -200	12.0	-0.75	110	-2.4				•		•
TP25D	-350, -400	25.0	-0.4	100	-2.4		•		•		•

Note: 1. Refer to Arrays and Special Functions section for packages available.

N-Channel Depletion-Mode MOSFETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$V_{GS(OFF)}$ Gate to Source OFF Voltage Min (V)	Max (V)	I_{DSS} @ V_{GS} = 0V Saturated Current Min (mA)	Max (mA)	TO-39 N2	TO-92 N3	TO-220 N5	SOT-89 N8	Die ND
LND1	500	1000	-1.0	-3.0	1.0	3.0		•		•	•
DN25	350, 400	25	-1.0	-5.0	150	—	•	•	•	•	•

N-Channel Enhancement-Mode MOSFETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	Package Options						
					TO-3	TO-39	TO-52	TO-92	TO-220	Quad[1]	Die
VN01A	40, 60, 90	3.0	2.0	45		•	•	•	•	•	•
VN01C	160, 200	10.0	0.4	45		•		•	•		•
VN03D	350, 400	2.5	3.0	550	•	•			•		•
VN03E	450, 500	4.0	2.0	550	•	•			•		•
VN03F	550, 600	6.0	1.5	550	•				•		•
VN05D	350, 400	35.0	0.25	45		•		•			•
VN05E	450, 500	60.0	0.15	45		•		•			•
VN06D	350, 400	10.0	0.75	105		•		•	•		•
VN06E	450, 500	16.0	.50	125		•		•	•		•
VN06F	550, 600	20.0	0.25	85		•		•	•		•
VN11A	60, 100	0.7	8.0	240		•			•		•
VN11C	160, 200	3.0	2.0	280		•			•		•
VN12A	40, 60, 100	0.3	20.0	700		•			•		•
VN13A	40, 60, 100	8.0	0.50	25		•		•			•
VN21A	60, 100	3.0	0.5	45						•	•
VN22A	60, 100	0.35	8.0	400				•			•
VN22C	200, 240	1.25	5.0	300				•			•

Note: 1. Refer to Arrays and Special Functions section for packages available.

P-Channel Enhancement-Mode MOSFETs

Device Family	BV_{DSS} Min (V)	$RDS_{(ON)}$ Max (ohms)	$I_{D(ON)}$ Min (A)	C_{ISS} Typ (pf)	Package Options						
					TO-3	TO-39	TO-52	TO-92	TO-220	Quad[1]	Die
VP01A	-40, -60, -90	8.0	-0.50	45		•	•	•	•	•	•
VP01C	-160,-200	25.0	-0.35	50		•		•	•		•
VP03D	-350, -400	6.0	-1.5	600	•	•			•		•
VP03E	-450, -500	7.5	-1.0	500	•	•			•		•
VP05D	-350, -400	75.0	-0.20	45		•		•			•
VP05E	-450, -500	125.0	-0.10	45		•		•			•
VP06D	-350, -400	25.0	-0.40	105		•		•	•		•
VP06E	-450, -500	25.0	-0.20	95		•		•	•		•
VP11A	-60, -100	2.0	-5.0	300		•			•		•
VP11C	-160, -200	5.0	-1.5	300		•			•		•
VP12A	-40, -60, -100	0.8	-6.0	550		•			•		•
VP12C	-160, -200	2.5	-4.0	600		•			•		•
VP13A	-40, -60, -100	25.0	-0.25	25		•		•		•	
VP21A	60, 100	12.0	0.50	45				•			•
VP22A	-40, -60, -100	-0.9	4.0	450				•			•

Note: 1. Refer to Arrays and Special Functions section for packages available.

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DMOS Array Selector Guide

Low Voltage N-Channel Arrays

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
VN0104	4N	40	3	•	•			•
VN0106	4N	60	3	•	•			•
TN0604	4N	40	1.0			•		•
TN0606	4N	60	1.5	•	•			•
VN2106	4N	60	3				•	•
VN2110	4N	100	3				•	•
VQ1000	4N	60	5.5	•	•			•
VQ1001	4N	30	1		•			•
VQ1004	4N	60	3.5	•	•			•

Note 1: Excluding package suffix.

Low Voltage P-Channel Arrays

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
VP0104	4P	-40	8	•	•			•
VP0106	4P	-60	8	•	•			•
TP0604	4P	-40	2			•		•
TP0606	4P	-60	3.5	•	•			•
VQ2001	4P	-30	2		•			•
VQ2006	4P	-90	5		•			•

Note 1: Excluding package suffix.

Low Voltage Complementary Arrays

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options				
				Plastic Dip	Ceramic Dip	SOW-20	Ceramic LCC	Die
TC0604	2N + 2P	40	3.0[2]			•		•
VC0106	2N + 2P	60	11.0[2]	•	•			•
TQ3001	2N + 2P	40	3.0[2]	•	•		•	•
VQ3001	2N + 2P	40	3.0[2]	•	•		•	•
VQ7254	2N + 2P	20	3.0[2]	•	•			•

Notes:
1. Excluding package suffix.
2. One N-channel plus one P-channel.

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AN0120	8N	200	300	•		•
AN0130	8N	300	300	•		•
AN0140	8N	400	350	•	•	•
AN0420	8N	200	300	•		•
AN0430	8N	300	300	•		•
AN0440	8N	400	350	•	•	•
AP0120	8P	-200	600	•		•
AP0130	8P	-300	600	•		•
AP0140	8P	-400	700	•	•	•
AP0420	8P	-200	600	•		•
AP0430	8P	-300	600	•		•
AP0440	8P	-400	700	•	•	•

Notes:
1. Excluding package suffix.
2. Monolithic 8 Channel Array.

High Voltage Low Leakage Arrays [2,3]

Device No.[1]	Number of Channels/Type	BV_{DSS} Min (V)	$R_{DS(ON)}$ Max (Ω)	Package Options		
				Plastic Dip	SOW-20	Die
AN0116	8N	160	350	•	•	•
AN0132	8N	320	350	•	•	•
AN0416	8N	160	350	•	•	•
AN0432	8N	320	350	•	•	•
AN0516	8N	160	350	•	•	•
AN0532	8N	320	350	•	•	•
AP0116	8P	-160	700	•	•	•
AP0132	8P	-320	700	•	•	•
AP0416	8P	-160	700	•	•	•
AP0432	8P	-320	700	•	•	•
AP0516	8P	-160	700	•	•	•
AP0532	8P	-320	700	•	•	•

Notes:
1. Excluding package suffix.
2. Monolithic 8 Channel Array.
3. Low I_{DSS} Leakage (refer to data sheet for details).

High Voltage Level Translators

Device No.[1]	Number of Channels	V_{PP} Max (V)	I_{SOURCE} Min (mA)	I_{SINK} Min (mA)	Package Options			
					Plastic Dip	Ceramic Dip	SOW-20	Die
HT0130	8	300	0.2	0.1	•	•	•	•

Notes:
1. Excluding package suffix.

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High Voltage Driver/Interface ICs

High Voltage Source/Sink Outputs (Push-Pull)

Device Number	Out-puts	Logic Configuration	Output Operating Voltage	Output Current/ Channel	Similar Devices	Applications
HV04 HV06	64	Serial to parallel converter w/ latches, polarity and blanking	60V 80V	+10mA −20mA	—	EL column drivers, non-impact printers, LCD displays
HV04H HV06H	64	Serial to parallel converter w/ latches, polarity and blanking w/ hotswitch capability	60V 80V	+10mA −20mA	—	EL column drivers, non-impact printers, LCD displays
HV33	32 +22	Serial to parallel converter w/ strobe	36V	±4mA	—	Printhead driver
HV34	64	Serial to parallel converter w/ latches, polarity and blanking, V_{DD} = 5V	180V	±5mA	—	Electrostatic and ink-jet printers/plotters, PLZT drivers
HV35	64	Serial to parallel converter	275V	—	—	Electrostatic and ink-jet printers/plotters, PLZT drivers
HV36	4	Pin diode driver	220V	10mA	—	Pin diode driver
HV38	32	Gray shade column driver w/ 16 analog levels	60V	±15mA	—	Video and gray shade EL and LCD displays
HV53 HV54	32	Serial to parallel converter w/ latches, output enable	80V	±20mA	TI SN75555/75556 Sprague UCN5853/5854	EL column drivers and non-impact printers, LCD drivers
HV57 HV58	32	Serial to parallel converter w/ latches, polarity and blanking	80V	±20mA	TI SN75555/75556 Sprague UCN5853/5854	Non-impact printers/plotters, EL displays, LCD drivers
HV500	32	AC plasma driver w/ multi-plexed 8-bit shift register	100V	±15mA	TI SN75500/55500	AC plasma display drivers, printers
HV501	32	Serial to parallel AC plasma driver w/ shift register	100V	±15mA	TI SN75501/55501	AC plasma display drivers, printers
HV518	32	Serial to parallel converter w/ latch enable and strobe pins	80V	+50µA −25mA	TI SN75518 Sprague VCN5818-1	Plasma and vacuum fluorescent display driver
HV60	32	LCD driver w/ active return to ground	±40V	±15mA	None with return to GND capability	High voltage LCD displays
HV65	32	Serial to parallel converter w/ backplane output	60V	±5mA	TI SN75555/75556	EL column drivers, non-impact printers, LCD display drivers
HV6810	10	Serial to parallel converter w/ latches	80V	+100µA −25mA	TI TL4810 Sprague UCN5810	Vacuum fluorescent display drivers
HV70	34	Serial to parallel converter w/ polarity and output enable	230V	±70mA	TI SN755563 SN755564	Row driver for EL, plasma and other panels
HV72	40	Serial to parallel converter w/ polarity and output enable	250V	±70mA	NEC µPD16302	AC TFEL row drivers
HV77	64	Serial to parallel converter w/ four 16-bit shift registers	80V	±15mA	—	EL row drivers with high data throughput
HV78	64	Serial to parallel converter w/ two 32-bit shift registers	80V	±15mA	—	EL row drivers with high data throughput

High Voltage Source/Sink Outputs (Push-Pull) — Continued

Device Number	Out-puts	Logic Configuration	Output Operating Voltage	Output Current/ Channel	Similar Devices	Applications
HV701 HV711	40	Serial to parallel VF driver w/ shift register	220V	+0.5mA –3.0mA	TI 755701/711	Vacuum-fluorescent displays
HV702 HV712	40	Serial to parallel VF driver w/ shift register	220V	+2.5mA –10mA	TI 755702/712	Vacuum-fluorescent displays
HV83 HV84	32	Serial to parallel converter w/ latches, output enable, V_{DD} = 5V	80V	±20mA	TI SN75555/75556 Sprague UCN5853/5854	EL column drivers, non-impact printers, LCD displays
HV87 HV88	32	Serial to parallel converter w/ latches, polarity and blanking, V_{DD} = 5V	80V	±20mA –5mA	TI SN75555/75556 Sprague UCN5853/5854	EL column drivers, non-impact printers, LCD displays
HV93 HV94	32	Serial to parallel converter w/ latches, output enable, V_{DD} = 5V	80V	+5mA –20mA	TI SN75555/75556 Sprague UCN5853/5854	EL column drivers, non-impact printers, LCD displays
HV97 HV98	32	Serial to parallel converter w/ latches, polarity and blanking, V_{DD} = 5V	80V	+5mA -20mA	TI SN75555/75556 Sprague UCN5853/5854	Non-impact printers/plotters, EL displays, LCD drivers

High Voltage Sink-Only Outputs (Open Drain N-Channel)

Device Number	Out-puts	Logic Configuration	Output Operating Voltage	Output Current/ Channel	Similar Devices	Applications
HV03 HV05	64	Serial to parallel converter w/ latches, Supertex logic	220V 300V	+100mA	—	EL row drivers, non-impact printers/plotters
HV31	64	Serial to parallel converter w/ output enable	375V	+1mA	—	Electrostatic printers
HV51 HV52	32	Serial to parallel converter w/ output enable and strobe	225V	+100mA	TI 75551/75552 Sprague UCN5851/5852	EL row driver, non-impact printers/plotters
HV55 HV56	32	Serial to parallel converter latches, polarity and blanking	220V 300V	+100mA	TI 75551/75552 Sprague UCN5851/5852	Non-impact printers/plotters, EL row drivers

High Voltage Source-Only Outputs (Open Drain P-Channel)

Device Number	Out-puts	Logic Configuration	Output Operating Voltage	Output Current/ Channel	Similar Devices	Applications
HV41 HV42	32	Serial to parallel converter w/ output enable and strobe	–225V	–80mA	—	EL row drivers, non-impact printers
HV45 HV46	32	Serial to parallel converter latches, polarity and blanking	–220V –300V	-60mA	—	Non-impact printers/plotters, EL display row drivers
HV49	64	Serial to parallel converter	–375V	0.5mA	—	Electrostatic printers

High Voltage Analog Switches and Multiplexers

High Voltage Bilateral Switches

Device Number	Out-puts	Logic Configuration	Operating Voltage Supply	Operating Voltage Analog Signal	Output Current/ Channel	On-Resistance/ Channel	Applications
HV10	4	Parallel inputs, latches	160V	130V	±3.0A	30Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV12	8	Shift register, latches	160V	130V	±1.5A	35Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV14	8	Decoders, latches, chip select and data in	160V	130V	±1.5A	35Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV15	8	Decoders, latches and chip selects	160V	130V	±1.5A	35Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV16	8	Shift register, latches	160V	130V	±1.5A	35Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV18	8	Shift register, latches, and clear	160V	130V	±1.5A	35Ω	Medical ultrasound, HV multiplexers, ink-jet printers

Low-Power High Voltage Bilateral Switches

Device Number	Out-puts	Logic Configuration	Operating Voltage Supply	Operating Voltage Analog Signal	Output Current/ Channel	On-Resistance/ Channel	Applications
HV204	8	Shift register, latches, clear, low charge injection	200V	180V	±2.0A	27Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV21	8	Shift register, latches	160V	140V	±2.0A	27Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV22	8	Shift register, latches, and clear	160V	140V	±2.0A	27Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV217	8	Shift register, latches, and low noise	160V[1]	140V	±2.0A	25Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV218	8	Shift register, latches and low noise	160V[2]	140V	±2.0A	25Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV227	8	Shift register, latches, clear and low noise	160V[1]	140V	±2.0A	25Ω	Medical ultrasound, HV multiplexers, ink-jet printers
HV228	8	Shift register, latches, clear and low noise	160V[2]	140V	±2.0A	25Ω	Medical ultrasound, HV multiplexers, ink-jet printers

Notes:
1. V_{PP} = 40V to 80V and $V_{PP} - V_{NN}$ = 160V.
2. V_{PP} = 80V to 150V and $V_{PP} - V_{NN}$ = 160V.

High Voltage Analog Switches

Device Number	Switches	Switch Operating Voltage	Max Switch Resistance	Similar Devices	Applications
HV341	Dual SPST	100V P-P	110Ω	MAX 341	High voltage switching, mil electronics and instrumentation
HV343	Dual SPDT	100V P-P	110Ω	MAX 343	High voltage switching, mil electronics and instrumentation
HV345	Dual DPST	100V P-P	110Ω	MAX 345	High voltage switching, mil electronics and instrumentation
HV348	Dual SPST	100V P-P	55Ω	MAX 348	High voltage switching, mil electronics and instrumentation

High Voltage Power Supply ICs

High Voltage Switchmode PWM Controllers with MOSFET

Device Number	$+V_{IN}$ Min	$+V_{IN}$ Max	Max Feedback Voltage	Max Duty Cycle	MOSFET Switch B_{VDSS}	MOSFET Switch $R_{DS(ON)}$	Similar Devices	Applications
HV9100	10V	70V	±1%	49%	150V	5.0Ω	Siliconix SI9100 Teledyne TSC9100	DC/DC converters, distributed power systems
HV9101	10V	70V	±10%	49%	150V	5.0Ω	Siliconix SI9101 Teledyne TSC9101	DC/DC converters, distributed power systems
HV9102	10V	120V	±1%	49%	200V	7.0Ω	Siliconix SI9102	DC/DC converters, distributed power systems
HV9103	10V	120V	±1%	99%	200V	7.0Ω	—	DC/DC converters, distributed power systems
HV9105	10V	120V	±2%	49%	200V	5.0Ω	Siliconix SI9105 PWR-SMP400	DC/DC converters, distributed power systems
HV9106[1]	12V	450V	±2%	49%	600V	20.0Ω	PWR-SMP3 PWR-SMP210	DC/DC converters, distributed power systems
HV9108	10V	120V	±2%	99%	200V	5.0Ω	—	DC/DC converters, distributed power systems
HV9109[1]	12V	450V	±2%	99%	600V	20.0Ω	—	DC/DC converters, distributed power systems

Notes:
1. Consult factory for availability.

High Voltage Switchmode PWM Controllers

Device Number	$+V_{IN}$ Min	$+V_{IN}$ Max	Max Feedback Voltage	Max Duty Cycle	Similar Devices	Applications
HV9110	10V	120V	±1%	49%	Siliconix SI9110 Teledyne TSC9110	DC/DC converters, distributed power systems
HV9111	10V	120V	±10%	49%	Siliconix SI9101 Teledyne TSC9101	DC/DC converters, distributed power systems
HV9112	9V	80V	±2%	49%	Siliconix SI9122	DC/DC converters, distributed power systems
HV9113	10V	120V	±1%	99%	—	DC/DC converters, distributed power systems
HV9114[1]	11V	200V	±1%	49%	Siliconix SI9114	DC/DC converters, distributed power systems
HV9117[1]	11V	200V	±1%	99%	—	DC/DC converters, distributed power systems
HV9120	10V	450V	±2%	49%	Siliconix SI9120 Teledyne TSC9116 PWR-SMP520	DC/DC converters, distributed power systems
HV9123	10V	450V	±2%	99%	—	DC/DC converters, distributed power systems
HV9124[1]	12V	450V	±1%	49%	—	DC/DC converters, distributed power systems
HV9127[1]	12V	450V	±1%	99%	—	DC/DC converters, distributed power systems
HV9220[1,2]	10V	450V	±1%	49%	—	Two- and four-switch fixed frequency switchmode power converters

Notes:
1. Consult factory for availability.
2. Two-output device.

Supertex inc.

DMOS FETs Cross Reference*

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
2N6659	2N6659	2SK409	TN0620N5	BSS98	VN0106N3	D84DK2	VN1206N5
2N6660	2N6660	2SK411	VN0360N1	BST120	TP0104N8	D84DL2	VN1210N5
2N6661	2N6661	2SK428	VN1206N5	BST122	TP0104N8	IRF320	VN0340N1
2N6759	VN0335N1	2SK440	VN1220N5	BST70A	VN0109N3	IRF321	VN0335N1
2N6761	VN0345N1	2SK441	VN0650N2	BST72	VN1310N3	IRF322	VN0340N1
2N6781	VN1106N2	2SK680	TN0104N8	BST72A	VN1310N2	IRF323	VN0335N1
2N6782	VN1110N2	AM0610LL	TN0624N3	BST74	TN0620N3	IRF332	VN0340N1
2N7000	2N7000	AM10LM	VN0106N3	BST74A	TN0620N3	IRF333	VN0335N1
2N7007	2N7007	AM2222LL	VN0106N3	BST76	TN0620N3	IRF420	VN0350N1
2N7008	2N7008	AM2222LM	VN0106N3	BST76A	TN0620N3	IRF421	VN0345N1
2N7009	VN0550N3	AN0110NA	AN0116NA	BST84	TN2524N8	IRF422	VN0350N1
2N7010	VN2206N3	AN0120NA	AN0120NA	BST86	TN2524N8	IRF423	VN0345N1
2N7011	VN2206N3	AN0130NA	AN0130NA	BUZ20	VN1210N5	IRF432	VN0350N1
2N7014	VN1110N5	AN0140NA	AN0140NA	BUZ30	VN1220N5	IRF433	VN0345N1
2SJ101	VP1204N5	AP0120NA	AP0120NA	BUZ40	VN0350N5	IRF510	VN1210N5
2SJ102	VP1206N5	AP0130NA	AP0130NA	BUZ42	VN0350N5	IRF511	VN1206N5
2SJ117	VP0340N5	AP0140NA	AP0140NA	BUZ43	VN0350N1	IRF512	VN1210N5
2SJ121	VP1204N5	BS107	VN0120N3	BUZ46	VN0350N1	IRF513	VN1206N5
2SJ76	VP0116N5	BS107P	VN0120N3	BUZ60B	VN0340N5	IRF520	VN1210N5
2SJ77	TP0616N5	BS107PT	VN1320N3	BUZ63B	VN0340N1	IRF521	VN1206N5
2SJ78	VP1220N5	BS170	VN0106N3	BUZ72	VN1210N5	IRF522	VN1210N5
2SJ79	VP0120N5	BS170P	VN0106N3	BUZ72A	VN1210N5	IRF523	VN1206N5
2SJ79K	VP0120N5	BS229	TN0624N3	BUZ73A	VN1220N5	IRF530	VN1210N5
2SK196H	VN0116N2	BS250	VP0106N3	BUZ74	VN0350N5	IRF531	VN1206N5
2SK213	TN0620N5	BS250P	VP0106N3	BUZ74A	VN0350N5	IRF532	VN1210N5
2SK214	TN0620N5	BSR78	TP0604N3	BUZ76	VN0340N5	IRF533	VN1206N5
2SK215	TN0620N5	BSS100	TN0610N3	BUZ76A	VN0340N5	IRF710	VN0340N5
2SK216	TN0620N5	BSS101	TN0524N3	D80AK2	TN0606N3	IRF711	VN0335N5
2SK216K	TN0620N5	BSS110	VP0106N3	D80AL2	TN0610N3	IRF712	VN0340N5
2SK259	VN0335N1	BSS124	TN0640N3	D80AM2	TN0620N3	IRF713	VN0335N5
2SK260	VN0340N1	BSS125	VN0660N3	D80AN2	TN0620N3	IRF720	VN0340N5
2SK294	VN1210N5	BSS129	TN0624N3	D84BK2	VN1206N5	IRF721	VN0335N5
2SK295	VN1210N5	BSS135	VN0660N3	D84BL2	VN1210N5	IRF722	VN0340N5
2SK296	VN0335N5	BSS149	TN0624N3	D84BM2	VN1216N5	IRF723	VN0335N5
2SK298	VN0340N1	BSS192	TP2520N8	D84BN2	VN1220N5	IRF732	VN0340N5
2SK302	TN0104N8	BSS192	TP2520N8	D84BQ1	VN0335N5	IRF733	VN0335N5
2SK310	VN0340N5	BSS229	TN0624N3	D84BQ2	VN0340N5	IRF820	VN0350N5
2SK311	VN0345N5	BSS250	VP0106N3	D84CK2	VN1206N5	IRF821	VN0345N5
2SK319	VN0340N5	BSS295	VN2206N3	D84CL2	VN1210N5	IRF822	VN0350N5
2SK345	VN1204N5	BSS296	VN2210N3	D84CM2	VN1216N5	IRF823	VN0345N5
2SK346	VN1206N5	BSS297	TN0620N3	D84CN2	VN1220N5	IRF832	VN0350N5
2SK382	VN0350N5	BSS87	TN2524N8	D84CQ1	VN0335N5	IRF833	VN0345N5
2SK383	VN1210N5	BSS88	TN0624N3	D84CQ2	VN0340N5	IRF9510	VP1210N5
2SK402	VN0340N1	BSS89	TN0620N3	D84CR1	VN0345N5	IRF9511	VP1206N5
2SK408	TN0620N5	BSS92	TP0620N3	D84CR2	VN0350N5	IRF9512	VP1210N5

*The Supertex devices are a "form, fit, and function" replacement for the industry standard part types, but subtle differences in characteristics and/or specifications may exist.

Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
IRF9513	VP1206N5	MFE910	VN10KN9	MTP3N40	VN0340N5	RFL1P10	TP0610N2
IRF9520	VP1210N5	MFE9200	VN2406L	MTP4N08	VN1110N5	RFL2N05	VN1106N2
IRF9521	VP1206N5	MFE930	TN0604N2	MTP4N10	VN1110N5	RFL2N06	VN1106N2
IRF9522	VP1210N5	MFE960	TN0606N2	MTP5N05	VN1106N5	RFM3N45	VN0345N1
IRF9523	VP1206N5	MFE990	TN0610N2	MTP5N06	VN1206N5	RFM3N50	VN0350N1
IRF9532	VP1210N5	MFQ1000C	TN0606N7	MTP8N08	VN1210N5	RFM4N35	VN0335N1
IRF9533	VP1206N5	MFQ170P	TN0606N6	MTP8N10	VN1210N5	RFM4N40	VN0340N1
IRF9612	VP1120N5	MFQ6660C	TN0606N7	MTP8P08	VP1210N5	RFP12N08	VN1210N5
IRF9613	VP1116N5	MFQ6660P	TN0606N6	MTP8P10	VP1210N5	RFP12N10	VN1210N5
IRFF110	VN1210N2	MFQ6661P	VQ1006J	MXF350	TN2524N8	RFP15N05	VN1206N5
IRFF111	VN1206N2	MPF480	VN1310N3	MXF500	TN2524N8	RFP15N06	VN1206N5
IRFF112	VN1110N2	MPF481	VN1310N3	MXF930	TN0104N8	RFP1N35	VN0635N5
IRFF113	VN1106N2	MPF500	VN0550N3	MXF960	TN0104N8	RFP1N40	VN0640N5
IRFF120	VN1210N2	MPF6659	TN0604N3	MXF990	TN2524N8	RFP2N08	TN0610N5
IRFF121	VN1206N2	MPF6660	TN0606N3	PM1001L	TN0610N3	RFP2N10	VN1110N5
IRFF122	VN1210N2	MPF6661	TN0610N3	PM1002L	TN0610N3	RFP2N18	VN1120N5
IRFF123	VN1206N2	MPF910	VN0106N3	PM1003P	VN1110N5	RFP2N20	VN1120N5
IRFF130	VN1210N2	MPF9200	TN0620N3	PM1004P	VN1110N5	RFP2P08	TP0610N5
IRFF131	VN1206N2	MPF930	TN0604N3	PM1006P	VN1210N5	RFP2P10	TP0610N5
IRFF132	VN1210N2	MPF960	TN0606N3	PM1010P	VN1210N5	RFP3N45	VN0345N5
IRFF133	VN1210N2	MPF990	TN0610N3	PM1201L	TN0620N3	RFP3N50	VN0350N5
IRFF210	VN2220N2	MTM2N45	VN0345N1	PM503L	TN0606N3	RFP4N05	VN1106N5
IRFF211	VN2220N2	MTM2N50	VN0350N1	PM506L	TN0606N3	RFP4N06	VN1106N5
IRFF212	VN1120N2	MTM2P45	VP0345N1	PM509P	VN1206N5	RFP4N35	VN0335N5
IRFF213	VN2220N2	MTM2P50	VP0350N1	PM510P	VN1206N5	RFP4N40	VN0340N5
IRFF220	VN2220N2	MTM3N35	VN0335N1	PM512P	VN1206N5	RFP6P08	VP1210N5
IRFF221	VN2220N2	MTM3N40	VN0340N1	PM601L	VN0106N3	RFP6P10	VP1210N5
IRFF222	VN2220N2	MTP10N05	VN1206N5	PM602L	TN0606N3	RFP8P08	VP1210N5
IRFF223	VN2220N2	MTP10N06	VN1206N5	PM603L	TN0606N3	RFP8P10	VP1210N5
IRFF232	VN2220N2	MTP10N08	VN1210N5	PM604P	VN1106N5	SD1100CHP	VN0545ND
IRFF233	VN2220N2	MTP10N10	VN1210N5	PM605P	VN1206N5	SD1100HD	VN0545N2
IRFF310	VN0340N2	MTP12N05	VN1206N5	PM606L	TN0606N3	SD1101BD	VN0640N3
IRFF311	VN0335N2	MTP12N06	VN1206N5	PM608P	VN1206N5	SD1101CHP	VN0540ND
IRFF312	VN0340N2	MTP12N08	VN1210N5	PM609P	VN1206N5	SD1101HD	VN0640N2
IRFF313	VN0335N2	MTP12N10	VN1210N5	PM609R	VN1206N5	SD1102BD	VN0635N3
IRFF320	VN0340N2	MTP15N05	VN1206N5	PM610P	VN1206N5	SD1102CHP	VN0635ND
IRFF321	VN0335N2	MTP15N06	VN1206N5	PM612P	VN1206N5	SD1102HD	VN0635N2
IRFF322	VN0340N2	MTP1N45	VN0645N5	PM614P	VN1206N5	SD1104BD	TN0610N3
IRFF323	VN0335N2	MTP1N50	VN0350N5	PM801L	VN0109N3	SD1104DD	VN0109N9
IRFF332	VN0340N2	MTP1N55	VN0355N5	PM802L	TN0610N3	SD1104HD	TN0610N2
IRFF333	VN0335N2	MTP1N60	VN0360N5	PM805P	VN1210N5	SD1105BD	TN0610N3
IRFF420	VN0350N2	MTP20N08	VN1210N5	PM808P	VN1210N5	SD1105DD	VN0109N9
IRFF421	VN0345N2	MTP20N10	VN1210N5	PM814P	VN1210N5	SD1105HD	TN0610N2
IRFF422	VN0350N2	MTP2N35	VN0335N5	RFL1N08	TN0610N2	SD1106AD	VN0106N3
IRFF423	VN0345N2	MTP2N40	VN0340N5	RFL1N10	TN0610N2	SD1106CHP	VN0106ND
IRFG9113	TP0606N7	MTP2N45	VN0345N5	RFL1N12	VN2220N2	SD1106DD	VN0106N9
IRFS1Z0	TN2524N8	MTP2N50	VN0350N5	RFL1N15	VN2220N2	SD1107BD	TN0110N3
IRFS1Z3	TN0104N8	MTP2P45	VP0345N5	RFL1N18	VN1120N2	SD1107CHP	TN0110ND
MFE350	VN0535N2	MTP2P50	VP0350N5	RFL1N20	VN1120N2	SD1107DD	VN0109N9
MFE500	VN0550N2	MTP3N35	VN0335N1	RFL1P08	TP0610N2	SD1107HD	TN0110N2

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Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
SD1107N	VQ1000N6	SN0130NA	AN0130NA	VN1706L	VN1706L	VND011B	VN1210N2
SD1112BD	TN0620N3	SN0130NB	AN0130NB	VN1706M	VN1706L	VNE010B	VN1210N2
SD1112HD	TN0620N2	SN0140NA	AN0140NA	VN1710L	VN1710L	VNE011B	VN1210N2
SD1113BD	TN0520N3	SN0140NB	AN0140NB	VN1710M	VN1710L	VP0104N3	VP0104N3
SD1113CHP	TN0520ND	SN7000	2N7000	VN2010L	VN2010L	VP0104ND	VP0104ND
SD1113HD	TN0520N2	SP0610L	VP0106N3	VN2222KM	VN2222LL	VP0106N3	VP0106N3
SD1114BD	VN0109N3	TN0106N3	TN0106N3	VN2222L	VN2222LL	VP0106ND	VP0106ND
SD1114DD	VN0109N9	TN0106ND	TN0106ND	VN2222LL	VN2222LL	VP0109N3	VP0109N3
SD1114HD	VN0109N2	TN0110N3	TN0110N3	VN2222LM	VN2222LL	VP0109ND	VP0109ND
SD1115BD	VN0109N3	TN0110ND	TN0110ND	VN2222LM	VN1306N3	VP0300B	VP0300B
SD1115DD	VN0109N9	TZ400BD	VN0104N3	VN2406B	VN2406B	VP0300L	VP0300L
SD1115HD	VN0109N2	TZ402BD	VN1304N3	VN2406D	VN2406D	VP0300M	VP030OL
SD1117BD	TN0606N3	TZ403BD	VN1304N3	VN2406L	VN2406L	VP0535N3	VP0535N3
SD1117DD	VN0106N9	TZ404BD	VN1304N3	VN2406M	VN2406L	VP0535ND	VP0109ND
SD1117HD	TN0606N2	TZ404CY	TN0104N8	VN2410L	VN2410L	VP0535ND	VP0535ND
SD1117N	VQ1001J	UFNF433	VN0345N2	VN2410M	VN2410L	VP0540L	VP0640N5
SD1122BD	TN0520N3	VN01000D	VN1210N5	VN30ABA	VN0104N2	VP0540N3	VP0540N3
SD1122CHP	TN0520ND	VN0104N3	VN0104N3	VN3501A	VN0335N1	VP0540ND	VP0540ND
SD1124BD	VN0106N3	VN0104ND	VN0104ND	VN3501D	VN0335N5	VP0610L	VP0106N3
SD1127BD	VN0106N3	VN0106N3	VN0106N3	VN3515L	VN3515L	VP0614L	VP0106N3
SD1127CHP	VN0106ND	VN0106ND	VN0106ND	VN35AB	TN0606N2	VP0808B	VP0808B
SD1137BD	TN0606N3	VN0109N3	VN0109N3	VN35AK	TN0606N2	VP0808L	VP0808L
SD1137CHP	TN0606ND	VN0109ND	VN0109ND	VN4001A	VN0340N1	VP0808M	VP0808L
SD1200CHP	VN0545ND	VN0300D	VN0300D	VN4001D	VN0340N5	VP1008B	TP0610N2
SD1201BD	VN0540N3	VN0300L	VN0300L	VN4012L	VN4012L	VP1008L	VP1008L
SD1201CHP	VN0540ND	VN0300M	VN0300L	VN40AD	VN0104N5	VP1008M	TP0610N3
SD1202BD	TN0520N3	VN0401D	VN1204N5	VN4502A	VN0345N1	VQ1000J	VQ1000N6
SD1202CHP	TN0520ND	VN0601D	VN1206N5	VN4502D	VN0345N5	VQ1000P	VQ1000N7
SD1500BD	VN0660N3	VN0606M	VN0606LL	VN46AD	VN0104N5	VQ1001J	TN0606N6
SD1500CHP	VN0660ND	VN0610L	VN0610LL	VN5002A	VN0350N1	VQ1001P	VQ1001P
SD1501BD	VN0655N3	VN0610LL	VN0610LL	VN5002D	VN0350N5	VQ1004J	VQ1004J
SD1501CHP	VN0660ND	VN0801D	VN1210N5	VN6035L	VN6035L	VQ1004P	VQ1004P
SD204CHP	VN2106ND	VN0808M	VN0808L	VN66AD	VN0106N5	VQ2000J	TP0606N6
SD204HD	VN0104N3	VN10KE	VN0106N9	VN66AK	VN0106N2	VQ2000P	VQ2006P
SD2107BD	VP0109N3	VN10KM	VN10KN3	VN67AA	VN0106N5	VQ2001J	TP0604N6
SD2107CHP	TP0610ND	VN10KMA	VN10KN3	VN67AB	VN0106N2	VQ2001P	VQ2001P
SD2107DD	VP0109N9	VN10KN3	VN10KN3	VN67ABA	VN0106N2	VQ2004J	TP0606N6
SD2107HD	TP0610N2	VN10LE	VN0106N9	VN67AD	VN0106N5	VQ2004P	VQ2006P
SD2204BD	VP0540N3	VN10LM	VN10KN3	VN67AK	VN0106N2	VQ2006J	TP0606N6
SD2204CHP	VP0540ND	VN10LM	VN10KN3	VN88AD	VN0109N5	VQ2006P	VQ2006P
SD3300BD	VN2210N3	VN10LP	VN1306N3	VN89ABA	VN0109N2	VQ3001J	VQ3001N6
SD3300CHP	VN2210ND	VN1206B	VN1206B	VN89AD	VN0109N5	VQ3001P	VQ3001N7
SD3300HD	TN0610N2	VN1206D	VN1206D	VN90AB	VN0109N2	VQ7254J	VQ7254N6
SD3301BD	TN0604N3	VN1206L	VN1206L	VN90ABA	VN0109N2	VQ7254P	VQ7254N7
SD3301CHP	VN2206ND	VN1206M	VN1206L	VN98AK	VN0109N2	ZVN0104A	VN0104N3
SD3301HD	TN0604N2	VN1210L	VN1210L	VN99AB	VN0109N2	ZVN0104B	VN0104N2
SD5101N	VN1304N6	VN1210M	VN1210L	VN99AK	VN0109N2	ZVN0104L	VN0104N5
SGSP531	VN0340N1	VN1216B	VN2216N2	VNC010B	VN1206N2	ZVN0106A	VN0106N3
SN0120NA	AN0120NA	VN1706B	VN1706B	VNC011B	VN1206N2	ZVN0106B	VN0106N2
SN0120NB	AN0120NB	VN1706D	VN1706D	VND010B	VN1210N2	ZVN0106L	VN0106N5

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Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
ZVN0108A	VN0109N3	ZVN0335B	VN0335N2	ZVN1135M	VN0335N1	ZVN1410A	VN1310N3
ZVN0108B	VN0109N2	ZVN0335L	VN0335N5	ZVN1140B	VN0340N2	ZVN1410B	VN1310N2
ZVN0108L	VN0109N5	ZVN0335M	VN0335N1	ZVN1140L	VN0340N5	ZVN1414A	VN0116N3
ZVN0109A	VN0109N3	ZVN0340B	VN0340N2	ZVN1140M	VN0340N1	ZVN1414B	VN0116N2
ZVN0109A	VN0109N3	ZVN0340L	VN0340N5	ZVN1145B	VN0345N2	ZVN1416A	VN0116N3
ZVN0109B	VN0109N2	ZVN0340M	VN0340N1	ZVN1145L	VN0345N5	ZVN1416B	VN1316N2
ZVN0109L	VN0109N5	ZVN0345B	VN0345N2	ZVN1145M	VN0345N1	ZVN1420A	VN0120N3
ZVN0110A	VN1310N3	ZVN0345L	VN0345N5	ZVN11A2B	VN1204N2	ZVN1420B	VN0120N2
ZVN0110B	VN1310N2	ZVN0345M	VN0345N1	ZVN11A2L	VN1204N5	ZVN2106A	TN0606N3
ZVN0110L	TN0610N5	ZVN0350L	VN0350N5	ZVN11A3B	VN1204N2	ZVN2106B	TN0606N2
ZVN0114A	TN0620N3	ZVN0350M	VN0350N1	ZVN11A3L	VN1204N5	ZVN2106L	TN0606N5
ZVN0114B	TN0620N2	ZVN0355B	VN0355N2	ZVN1204B	VN1204N2	ZVN2110A	TN0610N3
ZVN0114L	TN0620N5	ZVN0355L	VN0355N5	ZVN1204L	VN1204N5	ZVN2110B	TN0610N2
ZVN0116A	VN0116N3	ZVN0355M	VN0355N1	ZVN1206B	VN1206N2	ZVN2110L	TN0610N5
ZVN0116B	VN0116N2	ZVN0360B	VN0360N2	ZVN1206L	VN1206N5	ZVN2120A	VN0120N3
ZVN0116L	VN0116N5	ZVN0360L	VN0360N5	ZVN1208B	VN1210N2	ZVN2120B	VN0120N2
ZVN0117TA	VN0120N3	ZVN0360M	VN0360N1	ZVN1208L	VN1210N5	ZVN2120CSM	TN2524N8
ZVN0120A	VN0120N3	ZVN0450M	VN0350N1	ZVN1209B	VN1210N2	ZVN2120L	VN0120N5
ZVN0120B	VN0120N2	ZVN0530A	VN0535N3	ZVN1209L	VN1210N5	ZVN2206B	VN1206N2
ZVN0120L	VN0120N5	ZVN0530B	VN0535N2	ZVN1210B	VN1110N2	ZVN2206L	VN1206N5
ZVN0124A	TN0524N3	ZVN0535A	VN0535N3	ZVN1210L	VN1110N5	ZVN2210B	VN1110N2
ZVN0124B	TN0524N2	ZVN0535B	VN0635N2	ZVN1214B	VN2220N2	ZVN2210L	VN1110N5
ZVN0124L	TN0624N5	ZVN0535L	VN0635N5	ZVN1220B	VN2220N2	ZVN2220B	VN1120N2
ZVN01A2A	TN0102N3	ZVN0540A	VN0540N3	ZVN12A2B	VN1204N2	ZVN2220L	VN1120N5
ZVN01A2B	TN0602N2	ZVN0540B	VN0540N2	ZVN12A3B	VN1204N2	ZVN2224B	TN0624N2
ZVN01A2L	VN0300D	ZVN0540L	VN0640N5	ZVN12A3L	VN1204N5	ZVN2224L	TN0624N5
ZVN01A3B	TN0604N2	ZVN0545A	VN0545N3	ZVN1304A	VN1304N3	ZVN2535A	VN0535N3
ZVN01A3L	TN0606N5	ZVN0545B	VN0545N2	ZVN1304B	VN1304N2	ZVN2535B	VN0535N2
ZVN0204B	TN0104N2	ZVN0545L	VN0645N5	ZVN1306A	VN1306N3	ZVN2535L	VN0535N5
ZVN0204L	TN0606N5	ZVN1104B	TN0604N2	ZVN1306B	VN1306N2	ZVN3210L	VN1210N5
ZVN0206B	TN0606N2	ZVN1104L	VN1106N5	ZVN1308A	VN1310N3	ZVN3220L	VN2220N5
ZVN0206L	TN0606N5	ZVN1106B	VN1106N2	ZVN1308B	VN1310N2	ZVN3306A	VN0106N3
ZVN0208B	TN0610N2	ZVN1106L	VN1106N5	ZVN1309A	VN1310N3	ZVN3306B	VN0106N2
ZVN0208L	TN0610N5	ZVN1108B	VN1110N2	ZVN1309B	VN1310N2	ZVN3310A	VN1310N3
ZVN0209B	TN0610N2	ZVN1108L	VN1110N5	ZVN1310A	VN1310N3	ZVN3310B	VN1310N2
ZVN0209L	TN0610N5	ZVN1109B	VN1110N2	ZVN1310B	VN1310N2	ZVN3320A	VN0120N3
ZVN0210B	TN0610N2	ZVN1109L	VN1110N5	ZVN1314A	VN0116N3	ZVN3320B	VN0120N3
ZVN0210L	TN0610N5	ZVN1110B	TN0610N2	ZVN1314B	VN0116N2	ZVN4206A	TN0606N3
ZVN0214B	TN0620N2	ZVN1110L	TN0610N5	ZVN1316A	VN1316N3	ZVNL120A	VN0120N3
ZVN0216B	TN0620N2	ZVN1114B	VN2220N2	ZVN1316B	VN1316N2	ZVNL535A	VN0535N3
ZVN0216L	TN0620N5	ZVN1114L	VN2220N5	ZVN1320A	VN1320N3	ZVP0104A	VP0104N3
ZVN0220B	TN0620N2	ZVN1116B	VN1116N2	ZVN1320B	VN1320N2	ZVP0104B	VP0104N2
ZVN0220L	TN0620N5	ZVN1116L	TN0620N5	ZVN1404A	VN1304N3	ZVP0104L	VP0104N5
ZVN02A2B	TN0602N2	ZVN1120B	VN1120N2	ZVN1404B	VN1304N2	ZVP0106A	VP0106N3
ZVN02A2L	VN0300D	ZVN1120L	VN1120N5	ZVN1406A	VN1306N3	ZVP0106B	VP0106N2
ZVN02A3B	TN0604N2	ZVN1130B	VN0335N2	ZVN1406B	VN1306N2	ZVP0106L	VP0106N5
ZVN02A3L	VN0300D	ZVN1130L	VN0335N5	ZVN1408A	VN1310N3	ZVP0108A	VP0109N3
ZVN0330B	VN0335N2	ZVN1130M	VN0335N1	ZVN1408B	VN1310N2	ZVP0108B	VP0109N2
ZVN0330L	VN0335N5	ZVN1135B	VN0335N2	ZVN1409A	VN1310N3	ZVP0108L	VP0109N5
ZVN0330M	VN0335N1	ZVN1135L	VN0335N5	ZVN1409B	VN1310N2	ZVP0109A	VP0109N3

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Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number	Industry Part Number	Supertex Part Number
ZVP0109B	VP0109N2	ZVP0208B	TP0610N2	ZVP1320B	VP1320N2	ZVP2206B	VP1206N2
ZVP0109L	VP0109N5	ZVP0535A	VP0535N3	ZVP2106A	TP0606N3	ZVP2206L	VP1206N5
ZVP0110A	VP0109N3	ZVP0535B	VP0535N2	ZVP2106B	TP0606N2	ZVP2210B	VP1110N2
ZVP0110B	VP0109N2	ZVP0535L	VP0635N5	ZVP2106L	TP0606N5	ZVP2210L	VP1110N5
ZVP0110L	VP0109N5	ZVP0540A	VP0540N3	ZVP2110A	VP0109N3	ZVP2220B	TP0620N2
ZVP0120A	VP0120N3	ZVP0540B	VP0540N2	ZVP2110B	VP0109N2	ZVP2220L	TP0620N5
ZVP0120B	VP0120N2	ZVP0545A	VP0545N3	ZVP2110L	TP0610N5	ZVP3306A	VP0106N3
ZVP0120L	VP0120N5	ZVP0545B	VP0545N2	ZVP2120A	VP0120N3	ZVP3306B	VP0106N2
ZVP0204A	TP0606N3	ZVP0545L	VP0645N5	ZVP2120B	VP0120N2	ZVP3310A	VP1310N3
ZVP0204B	TP0606N2	ZVP1320A	VP1320N3	ZVP2120L	VP0120N5	ZVP3310B	VP1310N2
ZVP0206A	TP0606N3						
ZVP0206B	TP0606N2						
ZVP0208A	TP0610N3						

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Chapter 7 – N- and P-Channel Low Threshold MOSFETs

Supertex inc.

P-Channel Enhancement-Mode Lateral MOSFET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE
-16.5V	1.5Ω	-1.25A	-1.0V	LP0701N3	LP0701ND

Features

- Ultra low threshold
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Freedom from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switch
- General purpose line driver

Absolute Maximum Ratings

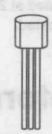
Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 10V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Advanced MOS Technology

These enhancement-mode (normally-off) transistors utilize a lateral MOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown. The low threshold voltage and low on-resistance characteristics are ideally suited for hand held battery operated applications.

Package Options



TO-92

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	-0.9A	-1.25A	1W	125	170	-0.9A	-1.25A

* I_D (continuous) is limited by max rated T_j.

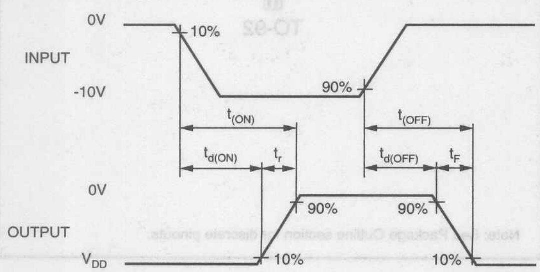
Electrical Characteristics (@ 25°C unless otherwise specified)

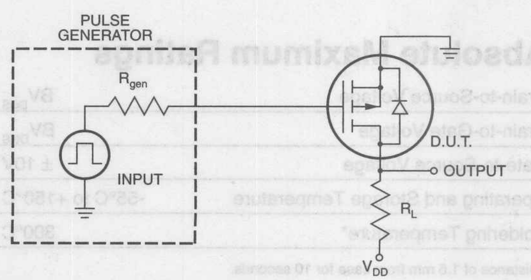
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-16.5			V	$V_{GS} = 0$, $I_D = -1mA$
$V_{GS(th)}$	Gate Threshold Voltage	-0.5	-0.7	-1.0	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 10V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			-100	nA	$V_{DS} = -15V$, $V_{GS} = 0V$
				-1.0	mA	V_{DS} = 0.8 Max Rating, $V_{GS} = 0V$, TA = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4		A	$V_{GS} = V_{DS} = -2V$
		-0.6	-1.0			$V_{GS} = V_{DS} = -3V$
		-1.25	-2.3		A	$V_{GS} = V_{DS} = -5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.0	4.0	Ω	$V_{GS} = -2V$, $I_D = -50mA$
			1.7	2.0		$V_{GS} = -3V$, $I_D = -150mA$
			1.3	1.5		$V_{GS} = -5V$, $I_D = -300mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature			0.75	%/°C	$V_{GS} = -5V$, $I_D = -300mA$
G_{FS}	Forward Transconductance	500	700		m℧	$V_{DS} = -15V$, $I_D = -1A$
C_{ISS}	Input Capacitance		120	250	pF	$V_{GS} = 0V$, $V_{DS} = -15V$, f = 1MHz
C_{OSS}	Common Source Output Capacitance		100	125		
C_{RSS}	Reverse Transfer Capacitance		40	60		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = -15V$, $I_D = -1.25A$, $R_{GEN} = 25\Omega$
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop		-1.2	-1.5	V	$V_{GS} = 0V$, $I_{SD} = -500mA$

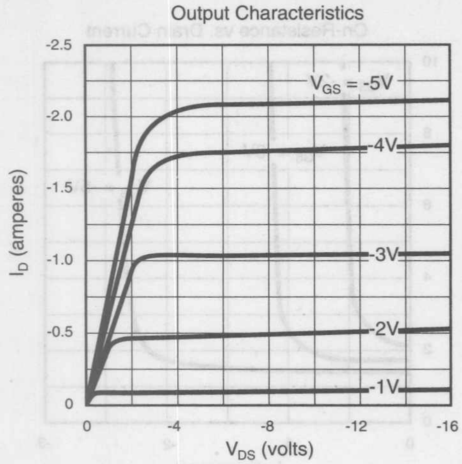
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

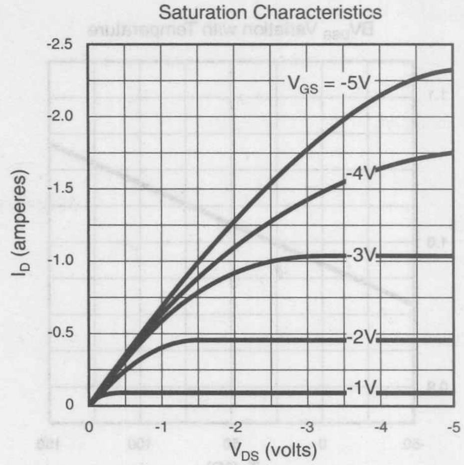
Switching Waveforms and Test Circuit

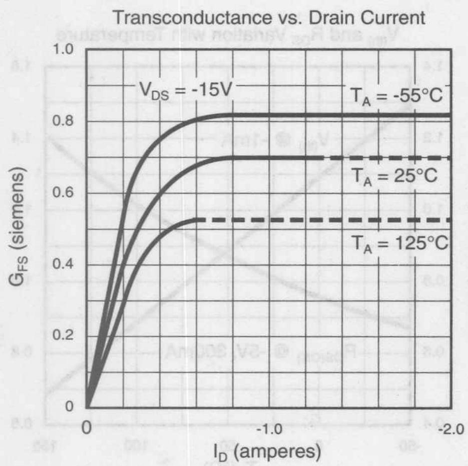


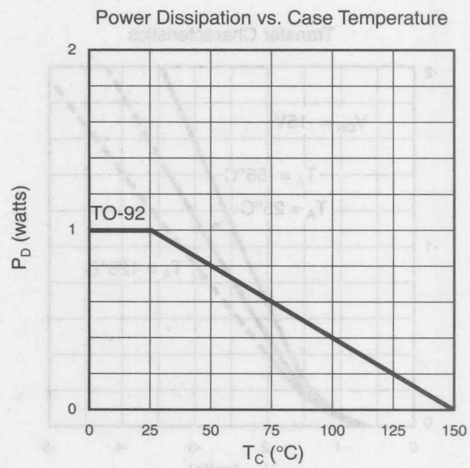


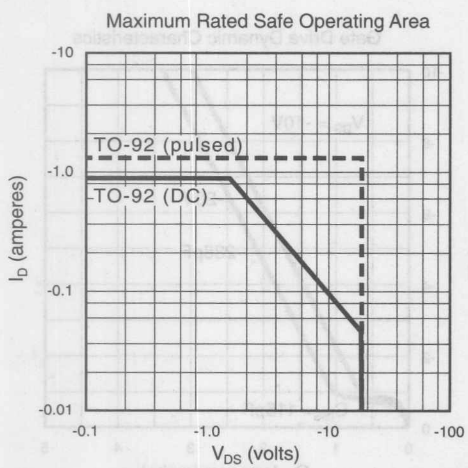
Typical Performance Curves

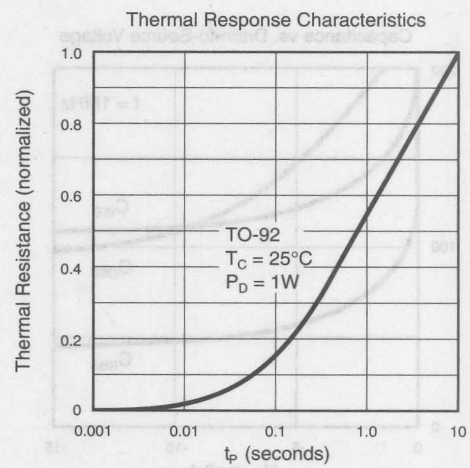






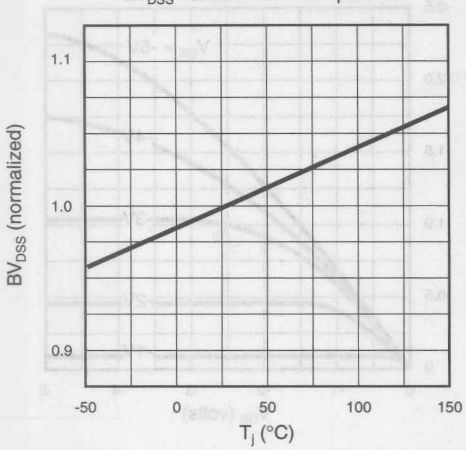




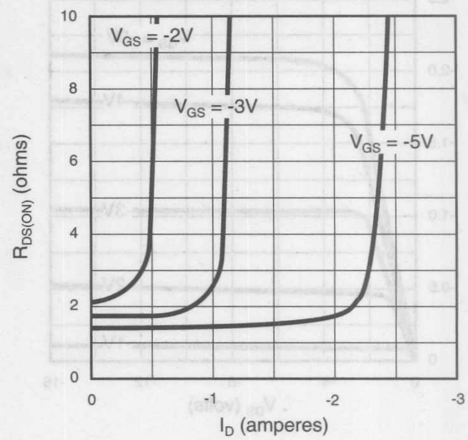


Typical Performance Curves

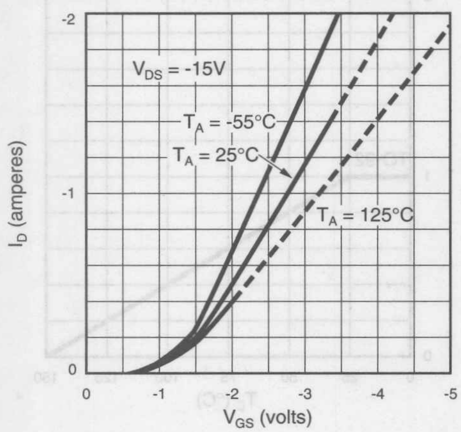
BV_{DSS} Variation with Temperature



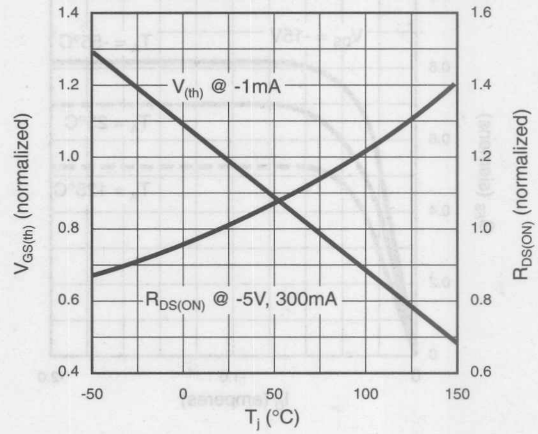
On-Resistance vs. Drain Current



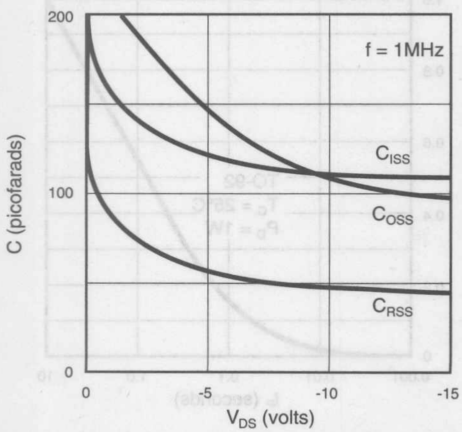
Transfer Characteristics



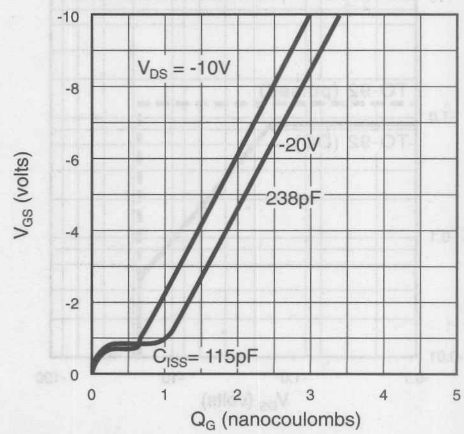
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

Low Threshold

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package		
				TO-39	TO-92	DICE†
60V	3Ω	2A	1.6V	TN0106N2	TN0106N3	TN0106ND
100V	3Ω	2A	1.6V	TN0110N2	TN0110N3	TN0110ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold — 1.6V max.
- High input impedance
- Low input capacitance — 50 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

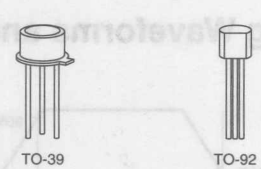
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-39	0.8A	2.5A	3.5W	125	35	0.8A	2.5A

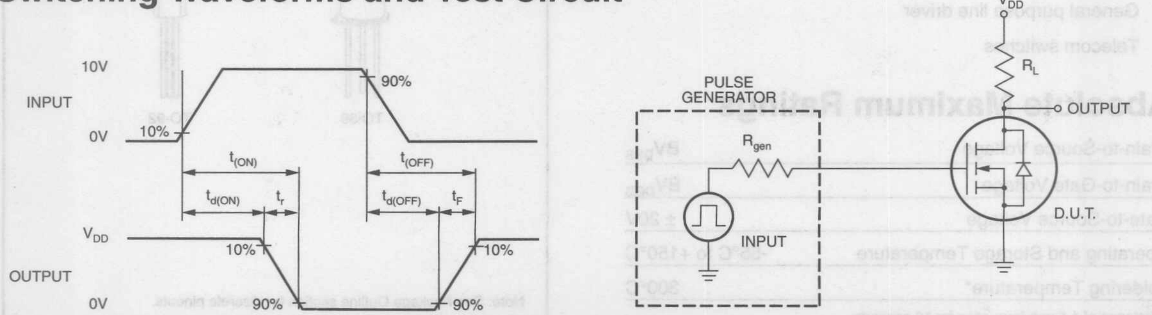
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

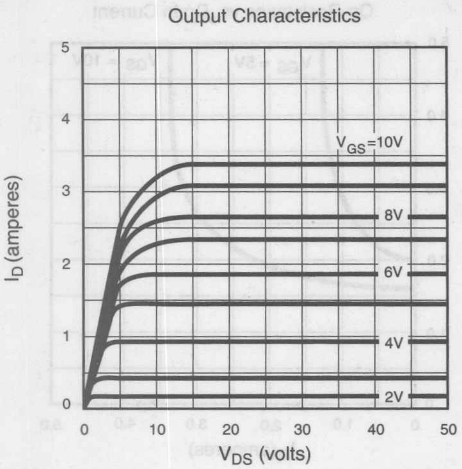
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0110	100			V	$I_D = 1mA, V_{GS} = 0$
		TN0106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}, I_D = 0.5mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.2	-5.0	mV/°C	$V_{GS} = V_{DS}, I_D = 1.0mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0, V_{DS}$ = Max Rating
					500		$V_{GS} = 0, V_{DS}$ = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.75	1.4		A	$V_{GS} = 5V, V_{DS} = 25V$
			2.0	3.4			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	4.5	Ω	$V_{GS} = 5V, I_D = 250mA$
				1.6	3.0		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.1	%/°C	$I_D = 0.5A, V_{GS} = 10V$
G_{FS}	Forward Transconductance		225	400		m℧	$V_{DS} = 25V, I_D = 500mA$
C_{ISS}	Input Capacitance			50	60	pF	$V_{GS} = 0, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25	35		
C_{RSS}	Reverse Transfer Capacitance			4.0	8.0		
$t_{d(ON)}$	Turn-ON Delay Time			2.0	5.0	ns	$V_{DD} = 25V$ $I_D = 1.0A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			3.0	5.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			6.0	7.0		
t_f	Fall Time			3.0	6.0		
V_{SD}	Diode Forward Voltage Drop			1.0	1.5	V	$I_{SD} = 0.5A, V_{GS} = 0$
t_{rr}	Reverse Recovery Time			400		ns	$I_{SD} = 0.5A, V_{GS} = 0$

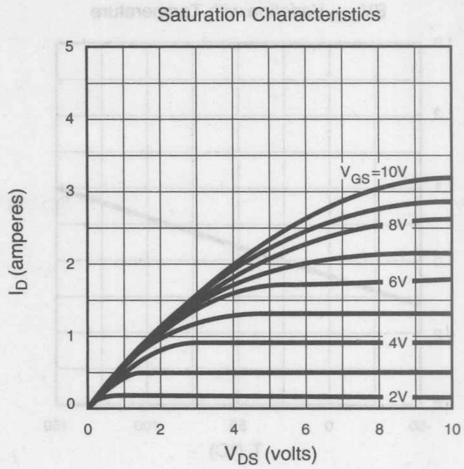
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

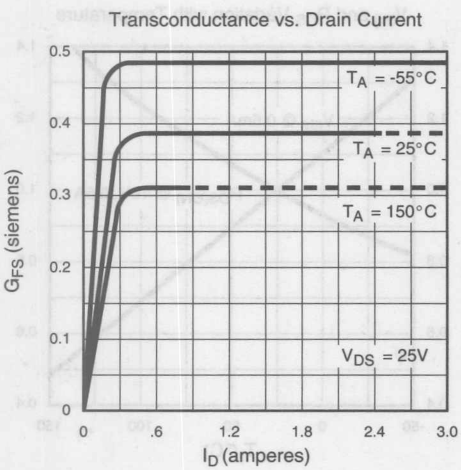
Switching Waveforms and Test Circuit

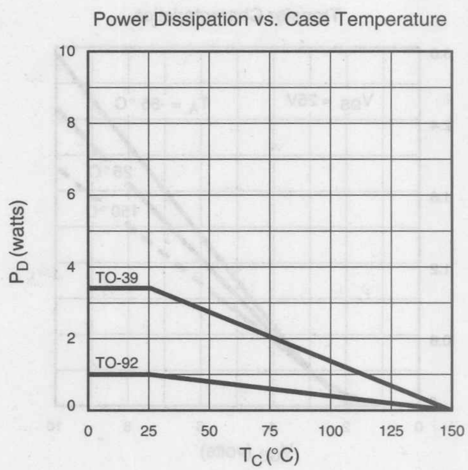


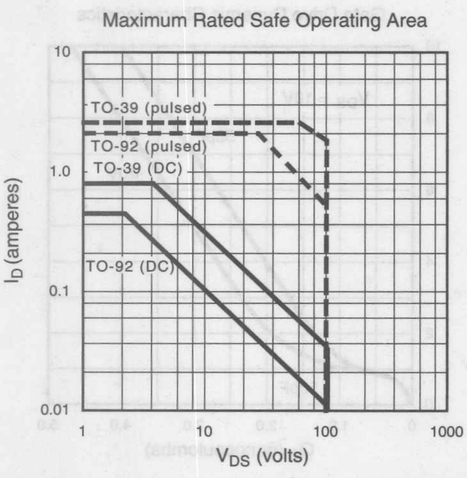
Typical Performance Curves

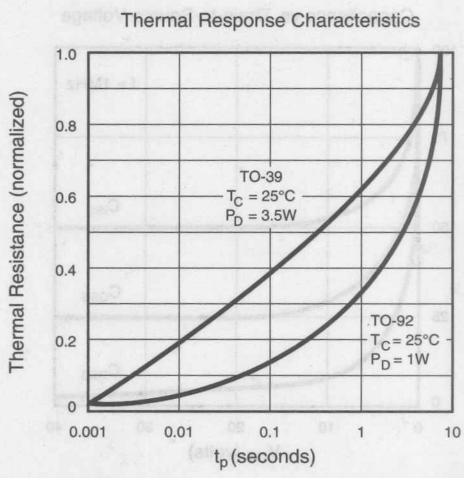












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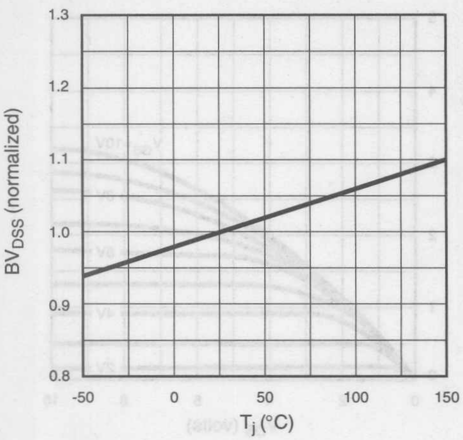
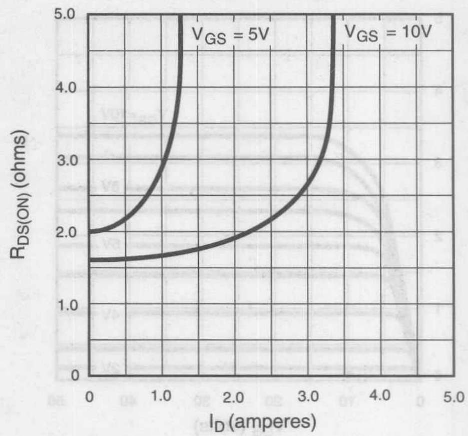
Typical Performance Curves

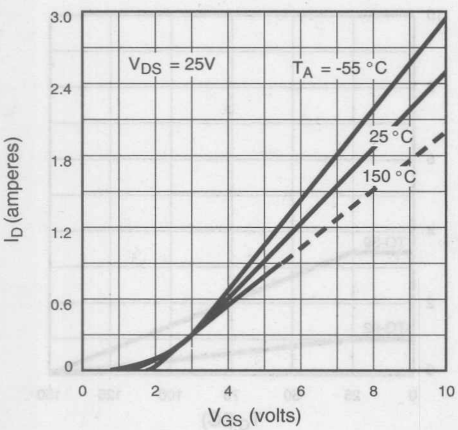
BV_{DSS} Variation with Temperature



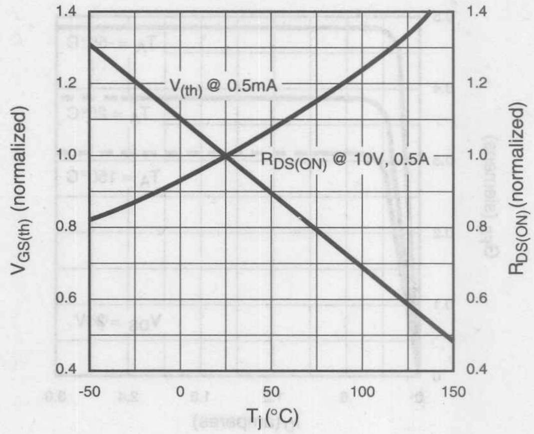
On-Resistance vs. Drain Current



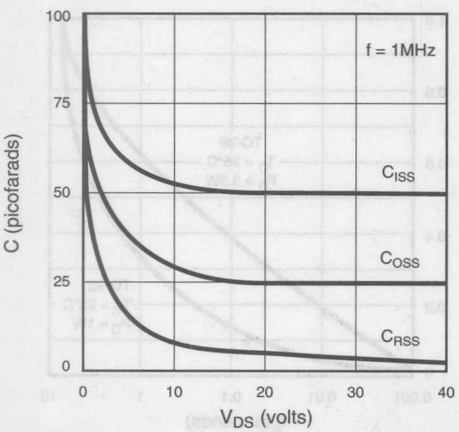
Transfer Characteristics



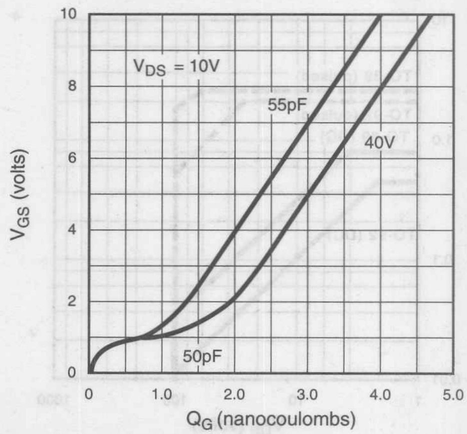
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

Low Threshold

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
				TO-39	TO-92	TO-243AA*	DICE†
20V	1.8Ω	1.6V	2.0A	TN0102N2	TN0102N3	—	TN0102ND
40V	1.8Ω	1.6V	2.0A	TN0104N2	TN0104N3	—	TN0104ND
40V	2.0Ω	1.6V	2.0A	—	—	TN0104N8	—

* Same as SOT-89.
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Low threshold —1.6V max.
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

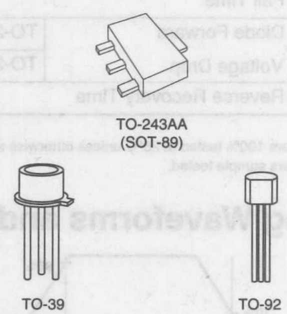
* For TO-39 and TO-92, distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	1.25A	2.90A	3.5W	35	125	1.25A	2.90A
TO-92	0.80A	2.40A	1.0W	125	170	0.80A	2.40A
TO-243AA	1.40A	2.90A	—	15	78†	1.40A	2.90A

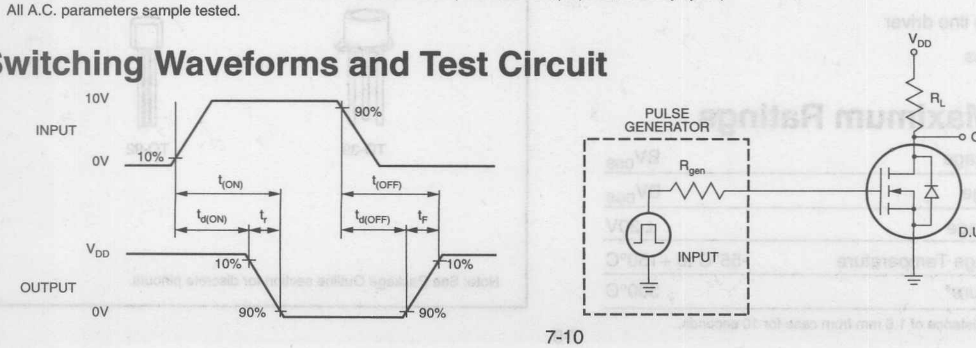
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Signficant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0104	40			V	$V_{GS} = 0$, $I_D = 1.0mA$
		TN0102	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 500\mu A$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					100	µA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			0.35		A	$V_{GS} = 3V$, $V_{DS} = 20V$
			0.5	1.1			$V_{GS} = 5V$, $V_{DS} = 20V$
			2.0	2.6			$V_{GS} = 10V$, $V_{DS} = 20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	All Packages		5.0		Ω	$V_{GS} = 3V$, $I_D = 50mA$
				2.3	2.5		$V_{GS} = 5V$, $I_D = 250mA$
		TO-39, TO-92		1.5	1.8		$V_{GS} = 10V$, $I_D = 1A$
		TO-243AA			2.0		$V_{GS} = 10V$, $I_D = 1A$
$\Delta R_{DS(ON)}$	Change in RDS(ON) with Temperature			0.7	1.0	%/°C	$V_{GS} = 10V$, $I_D = 1A$,
G_{FS}	Forward Transconductance		0.34	0.45		℧	$V_{DS} = 20V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance				70	pF	$V_{GS} = 0$, $V_{DS} = 20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				15		
$t_{d(ON)}$	Turn-ON Delay Time			3.0	5.0	ns	$V_{DD} = 20V$, $I_D = 1A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			7.0	8.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			6.0	9.0		
t_f	Fall Time			5.0	8.0		
V_{SD}	Diode Forward Voltage Drop	TO-39, TO-92		1.2	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
		TO-243AA			2.0		$V_{GS} = 0$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1A$

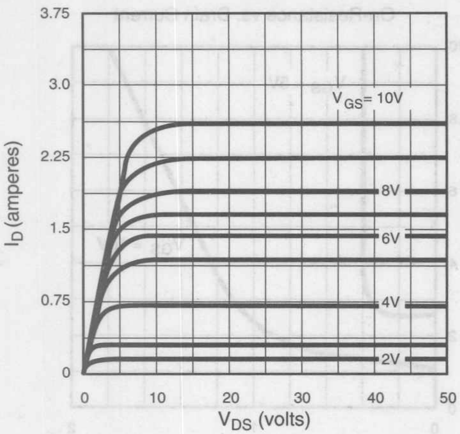
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

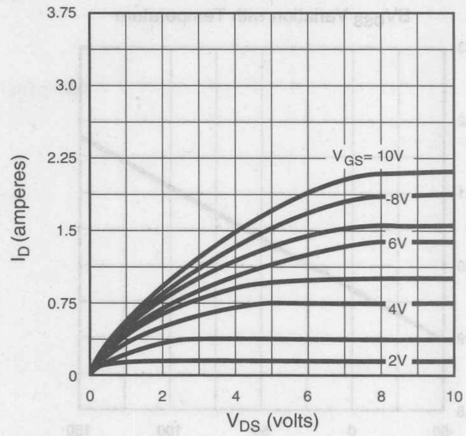


Typical Performance Curves

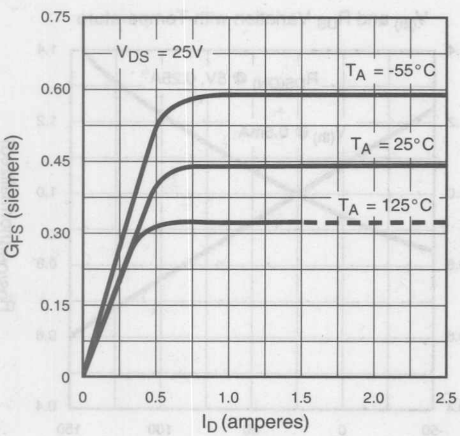
Output Characteristics



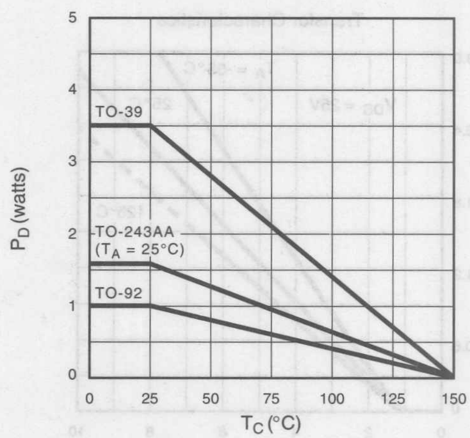
Saturation Characteristics



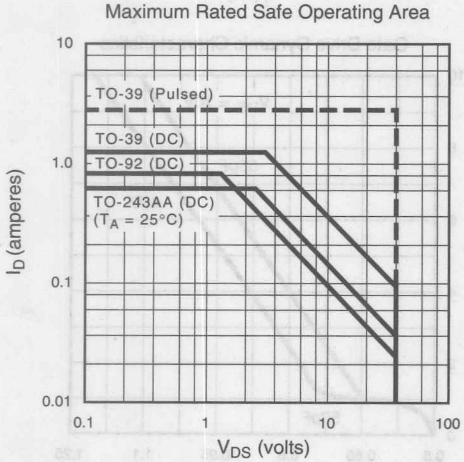
Transconductance vs. Drain Current



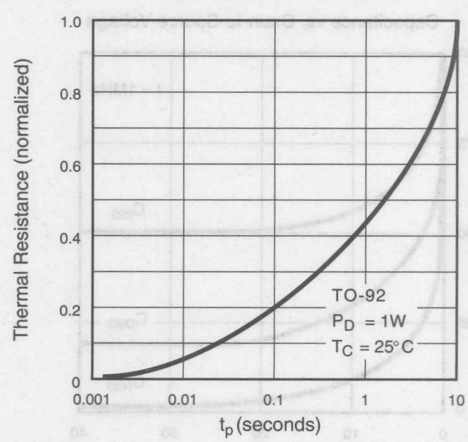
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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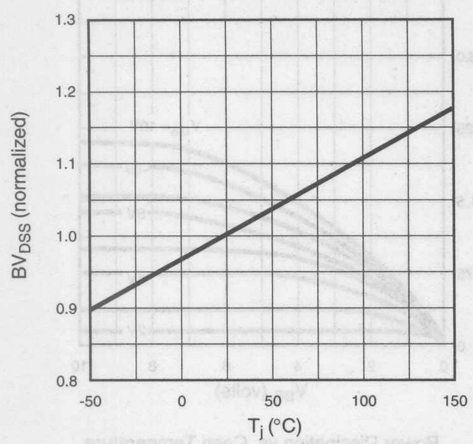
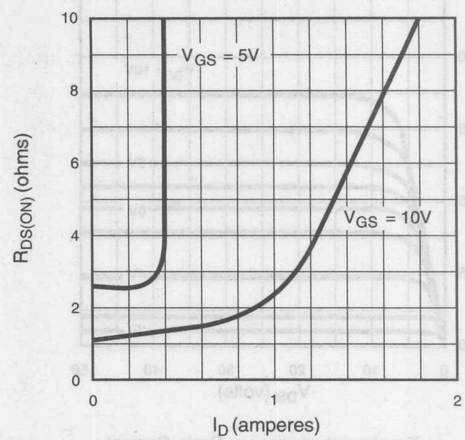
Typical Performance Curves

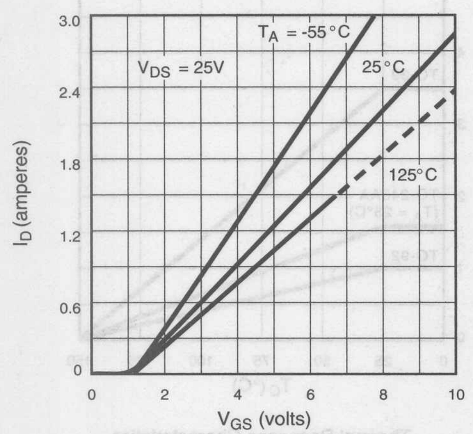
BVDSS Variation with Temperature



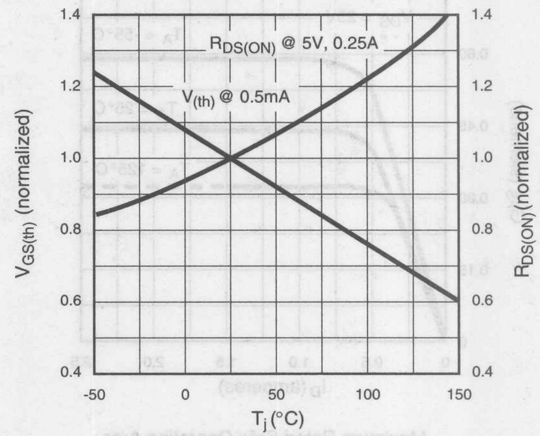
On-Resistance vs. Drain Current



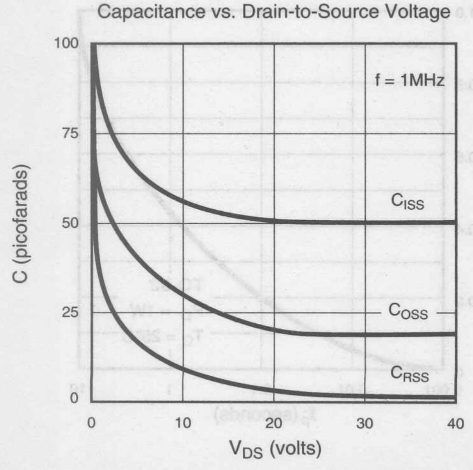
Transfer Characteristics



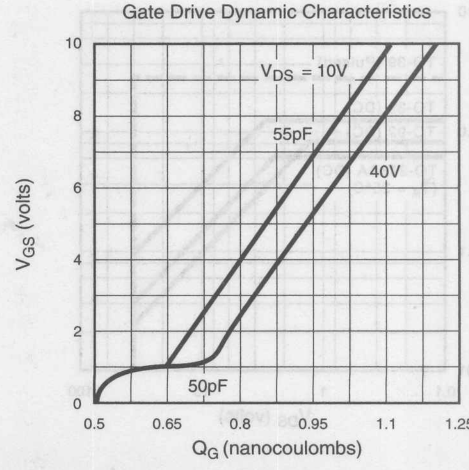
V(th) and RDS Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

TN05C

Low Threshold

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package		
				TO-39	TO-92	DICE†
200V	10Ω	300mA	1.5V	TN0520N2	TN0520N3	TN0520ND
240V	10Ω	300mA	1.5V	TN0524N2	TN0524N3	TN0524ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold —1.5V max.
- High input impedance
- Low input capacitance — 45 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

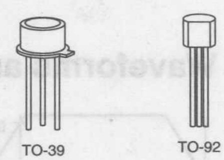
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	0.7A	1.5A	3.5W	35	125	0.7A	1.5A
TO-92	0.3A	1.0A	1.0W	125	170	0.3A	1.0A

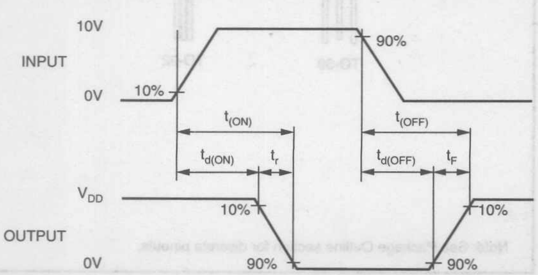
* I_D (continuous) is limited by max rated T_j.

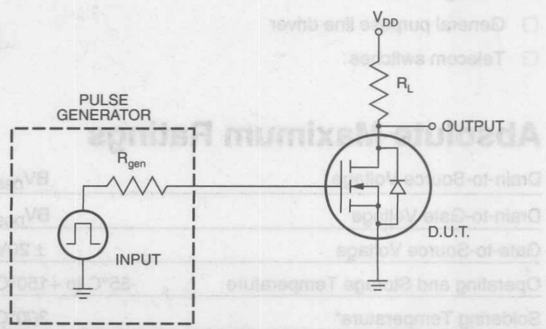
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0524	240			V	$V_{GS} = 0, I_D = 1mA$
		TN0520	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.5	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-4.0	mV/°C	$V_{GS} = V_{DS}, I_D = 1.0mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0, V_{DS}$ = Max Rating
					500		$V_{DS} = 0, V_{GS} = 0.8$ Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		100	360		mA	$V_{GS} = 3V, V_{DS} = 25V$
			300	850			$V_{GS} = 5V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			9.0	15	Ω	$V_{GS} = 3V, I_D = 50mA$
				7.0	10		$V_{GS} = 5V, I_D = 100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.9	1.5	%/°C	$V_{GS} = 5V, I_D = 0.2A$
G_{FS}	Forward Transconductance		0.15	0.35		℧	$V_{DS} = 25V, I_D = 0.2A$
C_{ISS}	Input Capacitance			45	60	pF	$V_{GS} = 0, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			15	35		
C_{RSS}	Reverse Transfer Capacitance			3.0	8.0		
$t_{d(ON)}$	Turn-ON Delay Time			3.0	5.0	ns	$V_{DD} = 25V$ $I_D = 0.3A$ $R_{GEN} = 25Ω$
t_r	Rise Time			3.0	5.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			5.0	10		
t_f	Fall Time			3.0	9.0		
V_{SD}	Diode Forward Voltage Drop			1.1	2.5	V	$V_{GS} = 0, I_{SD} = 100mA$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0, I_{SD} = 100mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

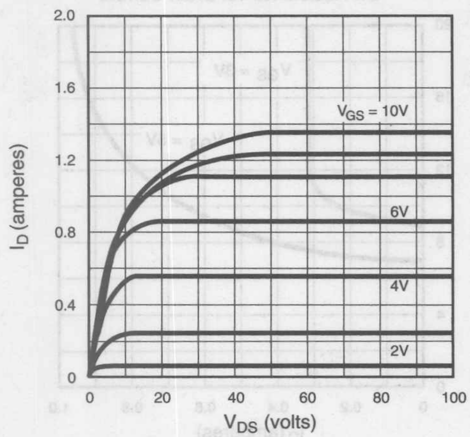
Switching Waveforms and Test Circuit



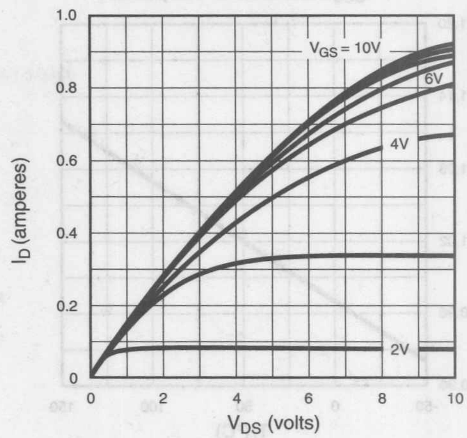


Typical Performance Curves

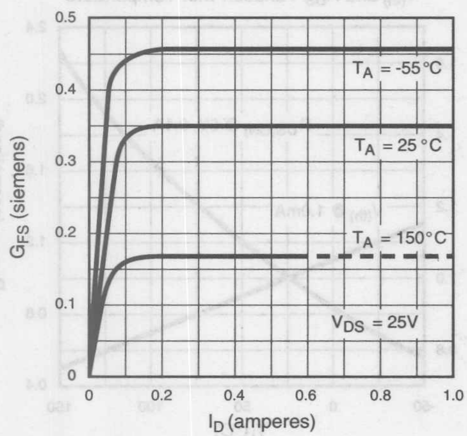
Output Characteristics



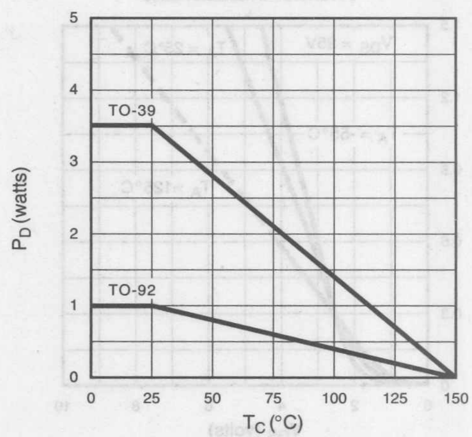
Saturation Characteristics



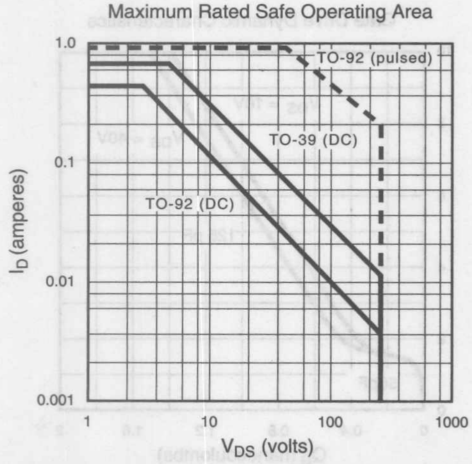
Transconductance vs. Drain Current



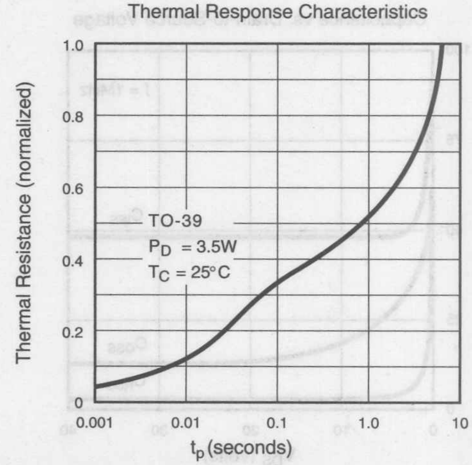
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

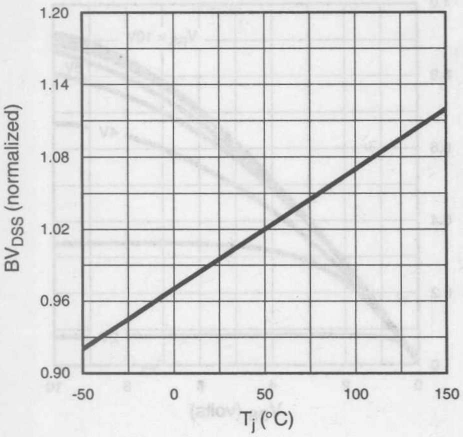


Thermal Response Characteristics

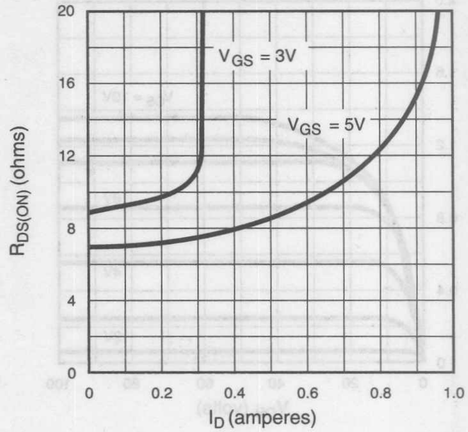


Typical Performance Curves

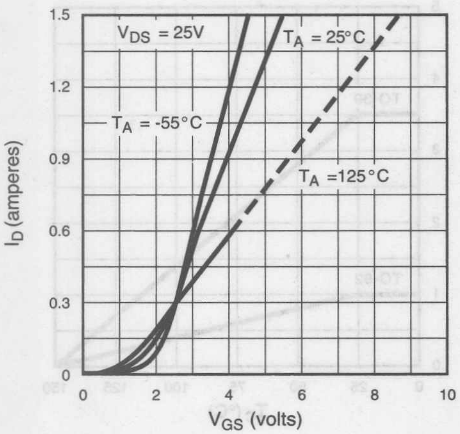
BV$_{DSS}$ Variation with Temperature



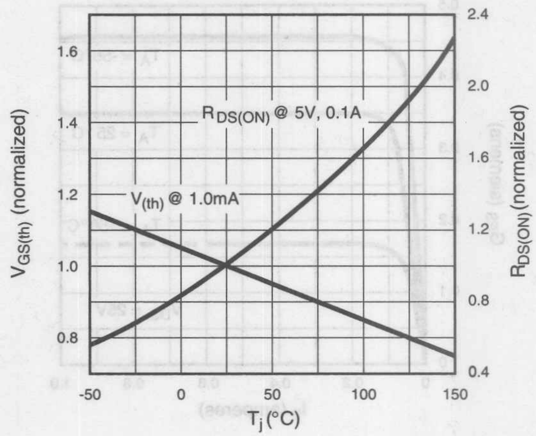
On-Resistance vs. Drain Current



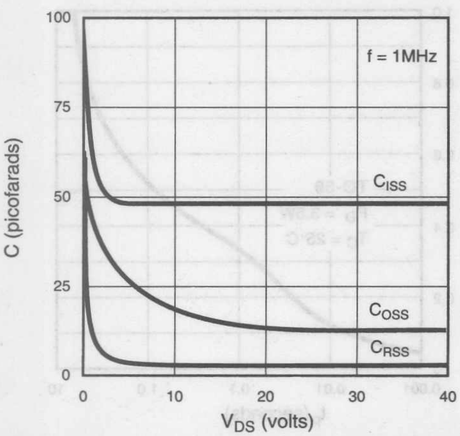
Transfer Characteristics



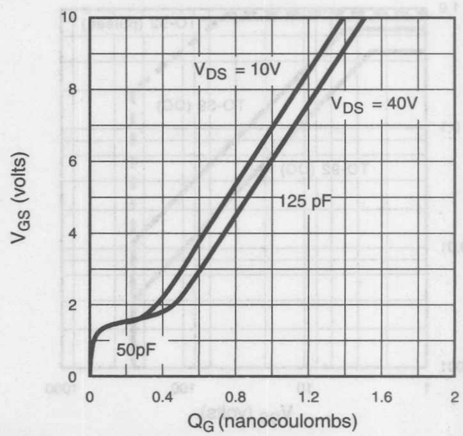
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package TO-92	DICE†
350V	22Ω	250mA	2.0V	TN0535N3	TN0535ND
400V	22Ω	250mA	2.0V	TN0540N3	TN0540ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold —2.0V max.
- High input impedance
- Low input capacitance — 48 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

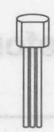
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	140mA	750mA	1.0W	170	125	140mA	750mA

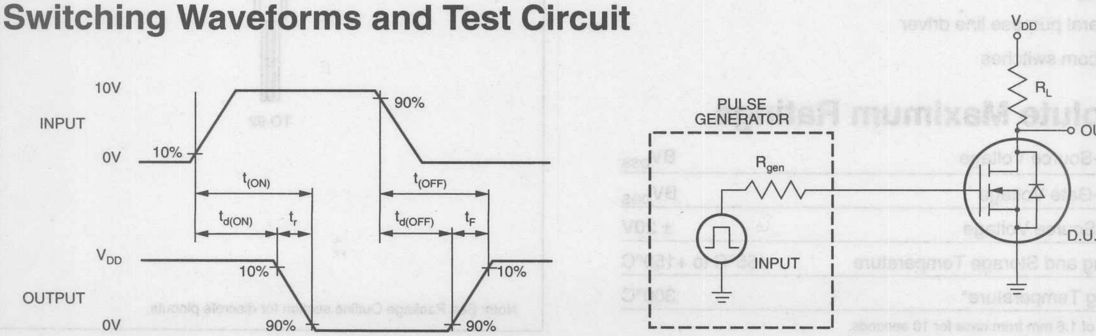
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0540	400			V	$V_{GS} = 0$, $I_D = 1mA$
		TN0535	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					500	µA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			550		mA	$V_{GS} = 5V$, $V_{DS} = 25V$
			250	750			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	22	Ω	$V_{GS} = 4.5V$, $I_D = 100mA$
				19	22		$V_{GS} = 10V$, $I_D = 150mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.9	1.5	%/°C	$V_{GS} = 10V$, $I_D = 0.1A$
G_{FS}	Forward Transconductance		125	200		m℧	$V_{DS} = 25V$, $I_D = 0.1A$
C_{ISS}	Input Capacitance			48	60	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			11	15		
C_{RSS}	Reverse Transfer Capacitance			3.0	8.0		
$t_{d(ON)}$	Turn-ON Delay Time			5.0	8.0	ns	$V_{DD} = 25V$, $I_D = 250mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time			5.0	8.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			5.0	9.0		
t_f	Fall Time			5.0	8.0		
V_{SD}	Diode Forward Voltage Drop			0.8	1.2	V	$V_{GS} = 0$, $I_{SD} = 150mA$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0$, $I_{SD} = 150mA$

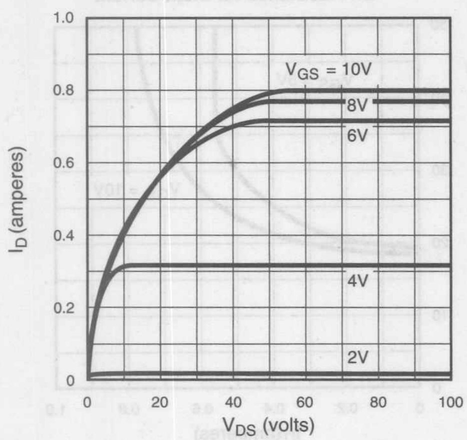
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

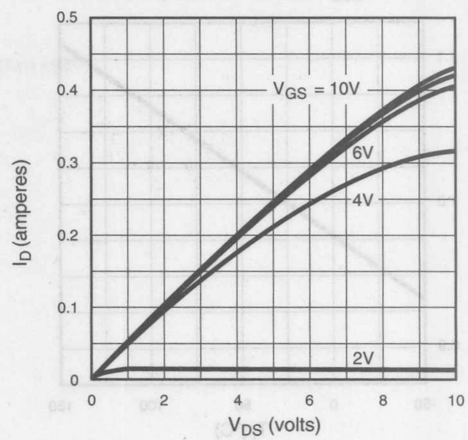


Typical Performance Curves

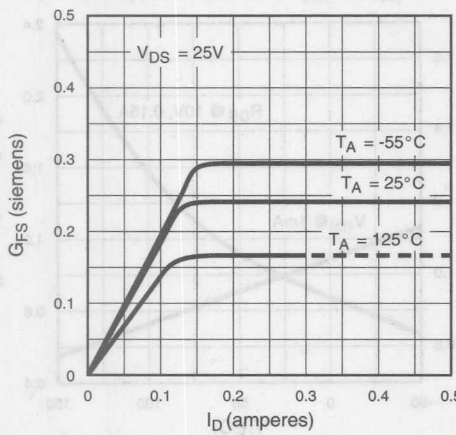
Output Characteristics



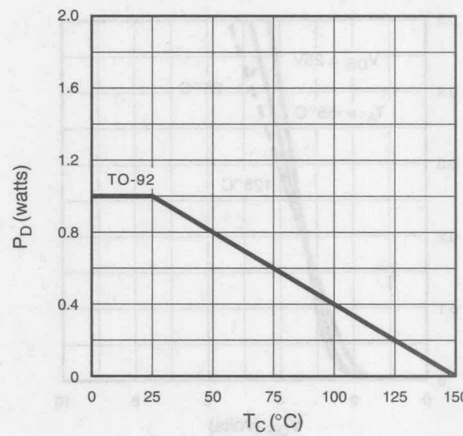
Saturation Characteristics



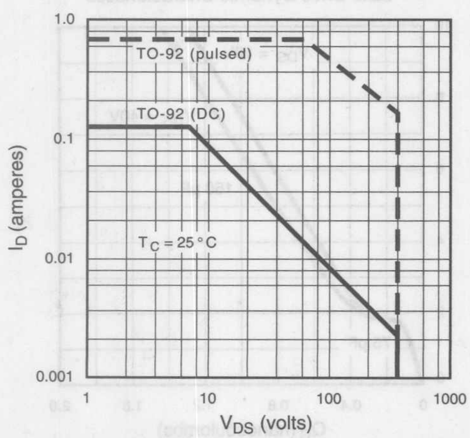
Transconductance vs. Drain Current



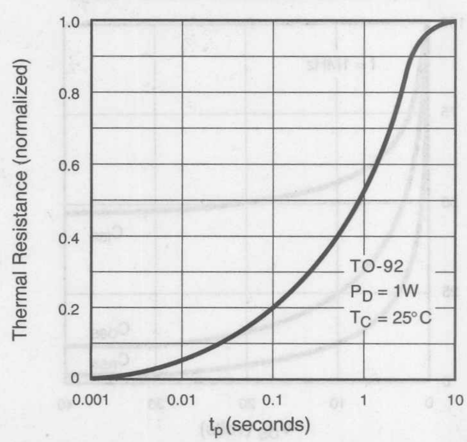
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

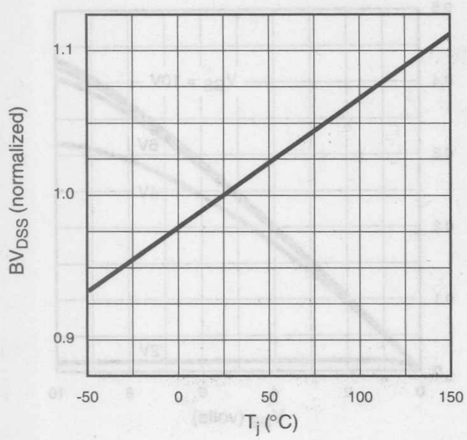


Thermal Response Characteristics

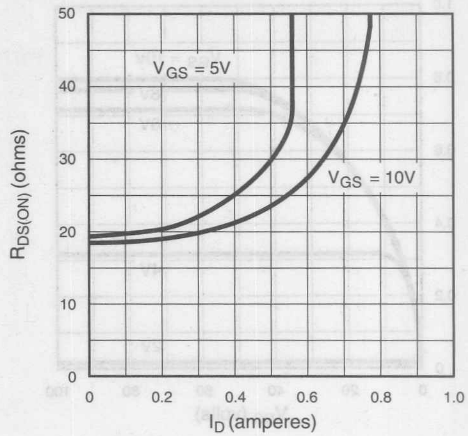


Typical Performance Curves

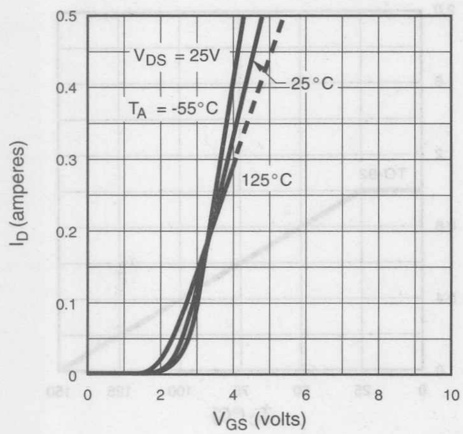
BV_{DSS} Variation with Temperature



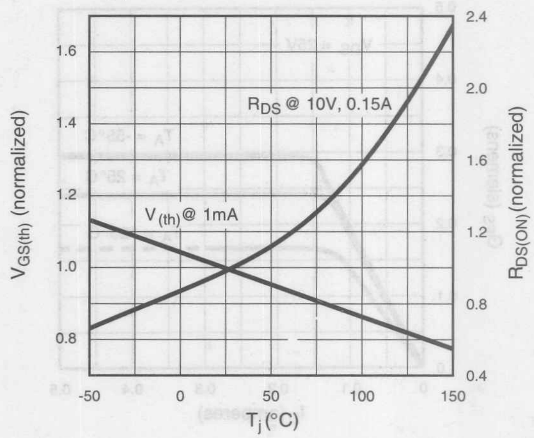
On-Resistance vs. Drain Current



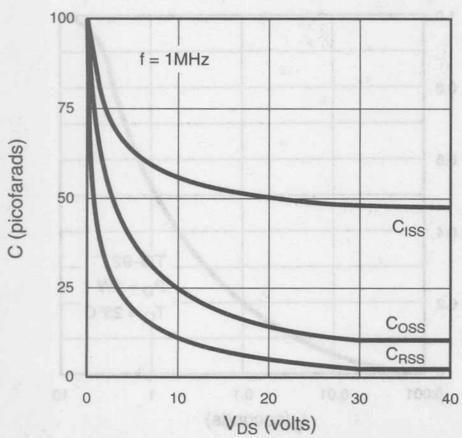
Transfer Characteristics



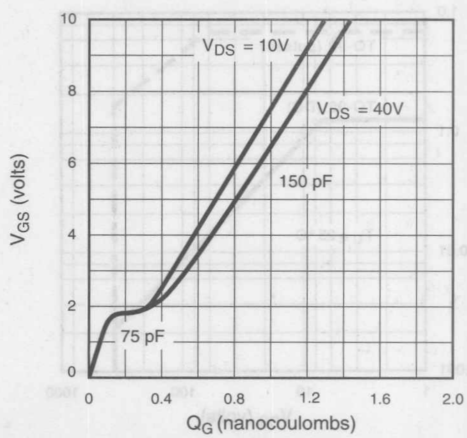
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package					
				TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
60V	1.5Ω	3.0A	1.6V	TN0606N2	TN0606N3	TN0606N5	TN0606N6	TN0606N7	TN0606ND
100V	1.5Ω	3.0A	1.6V	TN0610N2	TN0610N3	TN0610N5	—	—	TN0610ND

* 14 pin side brazed ceramic DIP
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold — 1.6V max.
- High input impedance
- Low input capacitance — 100 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

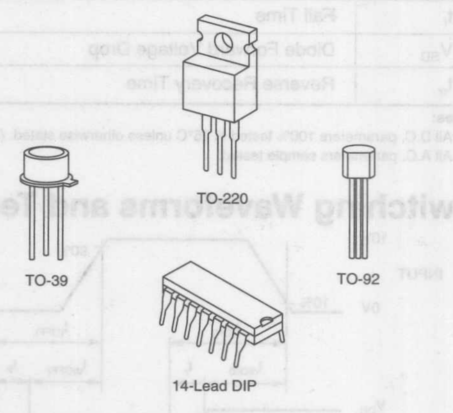
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	0.8A	3.2A	1W	125	170	0.8A	3.2A
TO-39	1.5A	4.0A	6W	20	125	1.5A	4.0A
TO-220	3.0A	4.1A	45W	2.7	70	3.0A	4.1A
Plastic DIP	Refer to Arrays & Special Functions Section.						
Ceramic DIP							

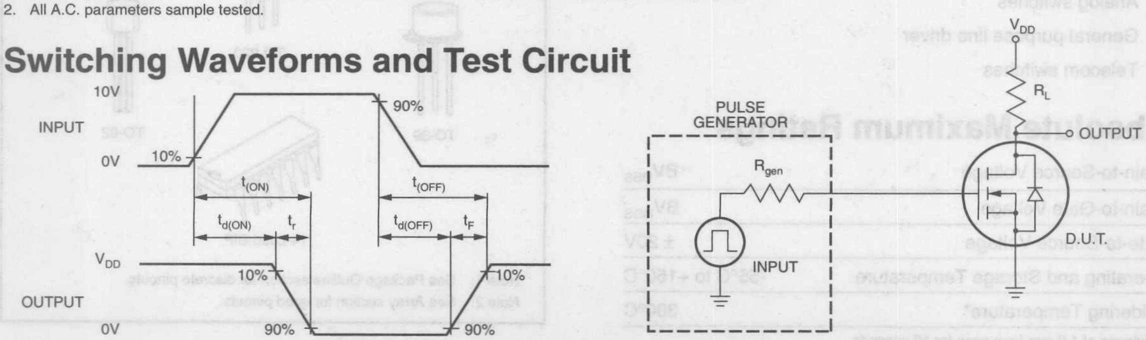
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage — TN0610	100			V	$V_{GS} = 0$, $I_D = 1mA$
	Drain-to-Source Breakdown Voltage — TN0606	60				
$V_{GS(th)}$	Gate Threshold Voltage	0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
				1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$ (note 2)
$I_{D(ON)}$	ON-State Drain Current	1.2	2.0		A	$V_{GS} = 5V$, $V_{DS} = 25V$
		3.0	6.7			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		1.5	2.0	Ω	$V_{GS} = 5V$, $I_D = 0.75A$
			1.0	1.5		$V_{GS} = 10V$, $I_D = 0.75A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/°C	$V_{GS} = 10V$, $I_D = 0.75A$
G_{FS}	Forward Transconductance	0.4	0.5		℧	$V_{DS} = 25V$, $I_D = 1.0A$
C_{ISS}	Input Capacitance		100	150	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance		50	85		
C_{RSS}	Reverse Transfer Capacitance		10	35		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V$ $I_D = 1.5A$ $R_{GEN} = 25Ω$
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
t_f	Fall Time			12		
V_{SD}	Diode Forward Voltage Drop		0.8	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0$, $I_{SD} = 1.5A$

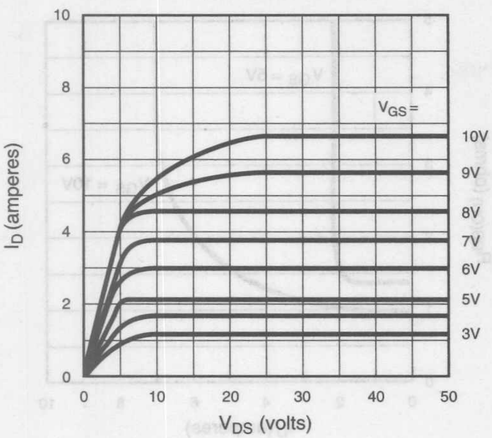
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

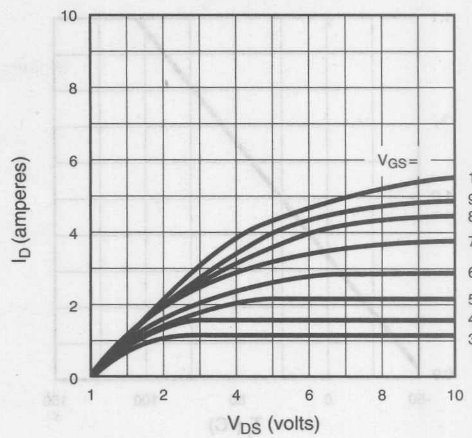


Typical Performance Curves

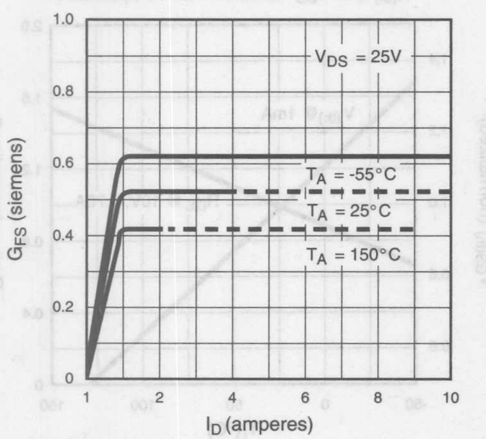
Output Characteristics



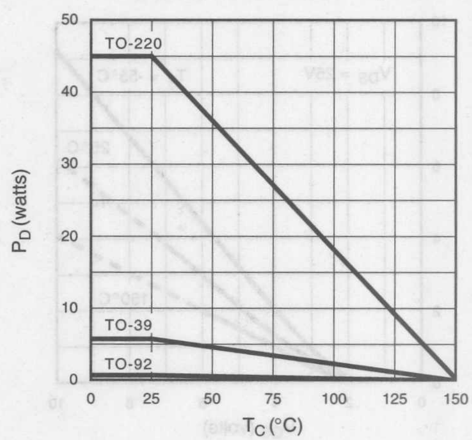
Saturation Characteristics



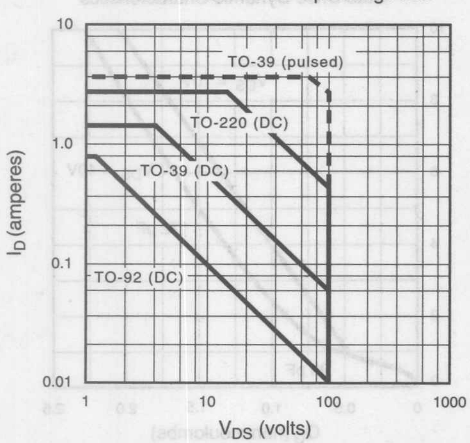
Transconductance vs. Drain Current



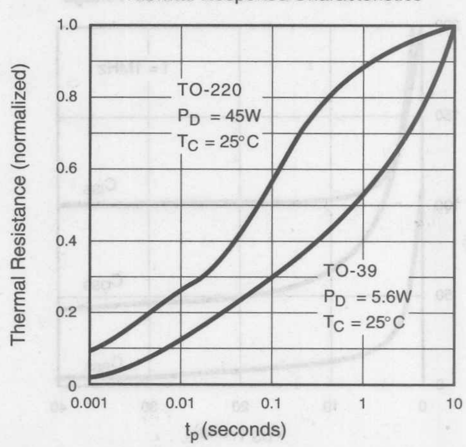
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

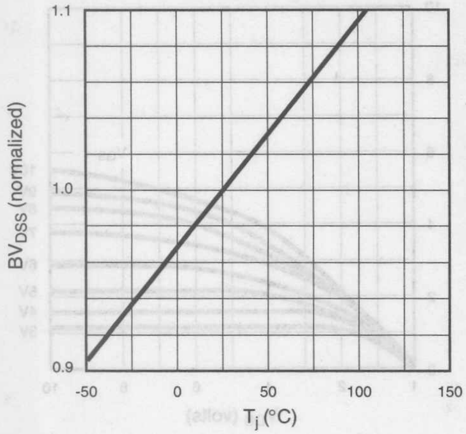


Thermal Response Characteristics

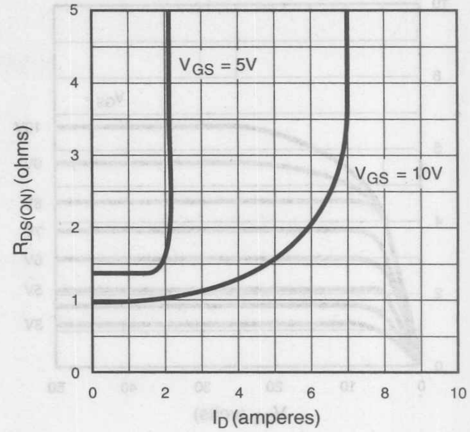


Typical Performance Curves

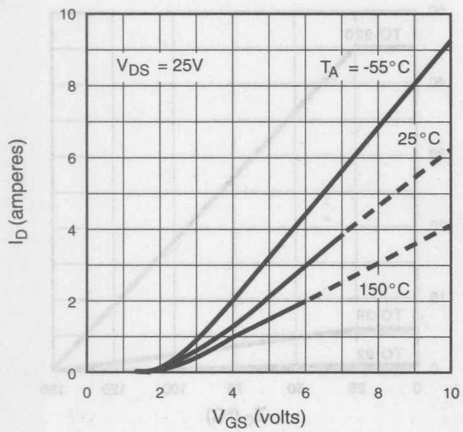
BV$_{DSS}$ Variation with Temperature



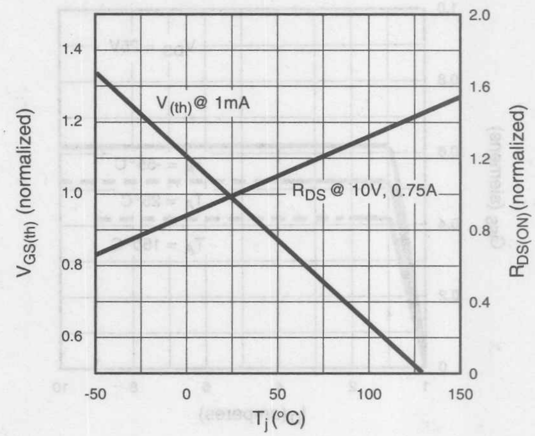
On-Resistance vs. Drain Current



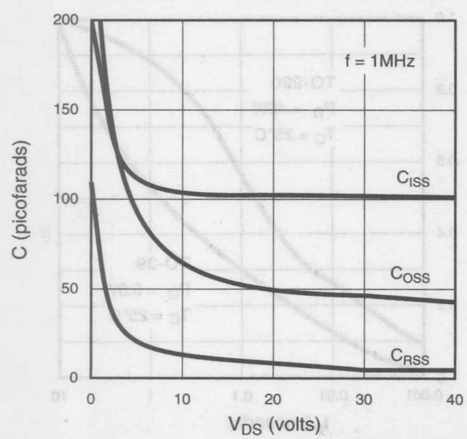
Transfer Characteristics



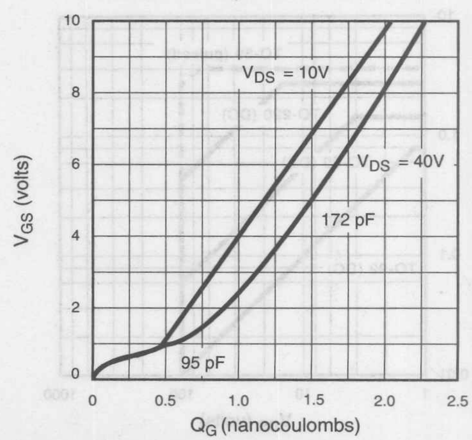
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package TO-39	TO-92	TO-220	DICE†
200V	6Ω	1.0A	1.6V	TN0620N2	TN0620N3	TN0620N5	TN0620ND
240V	6Ω	1.0A	1.6V	TN0624N2	TN0624N3	TN0624N5	TN0624ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Low threshold — 1.6V max.
- ☐ High input impedance
- ☐ Low input capacitance — 110 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

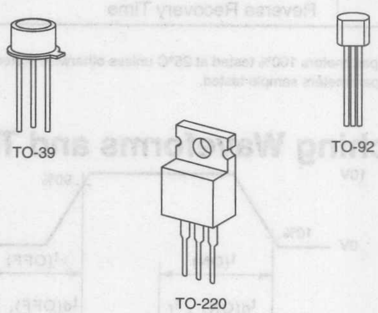
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	0.7A	2.5A	6W	20	125	0.7A	2.5A
TO-92	0.4A	2.0A	1W	125	170	0.4A	2.0A
TO-220	1.5A	2.5A	45W	2.7	70	1.5A	2.5A

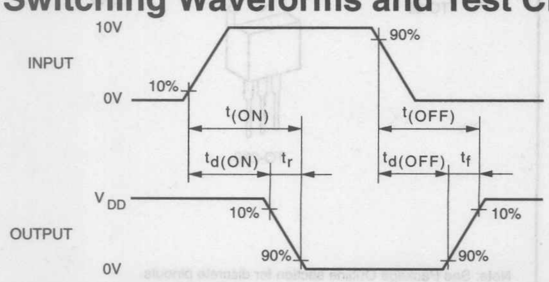
* I_D (continuous) is limited by max rated T_j.

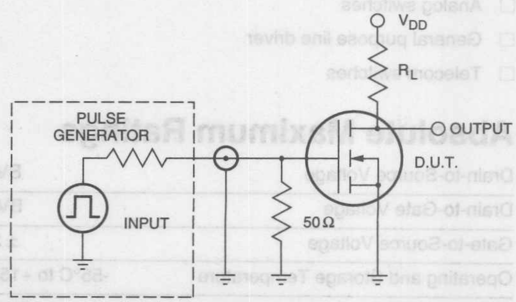
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0624	240			V	$V_{GS} = 0$, $I_D = 2.0mA$
		TN0620	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.5			A	$V_{GS} = 5V$, $V_{DS} = 25V$
			1.0				$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6	8	Ω	$V_{GS} = 5V$, $I_D = 0.25A$
				4	6		$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.4	%/°C	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance		300	400		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			110	150	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			40	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$ $I_D = 1.0A$ $R_{GEN} = 25\Omega$
t_r	Rise Time				8.0		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1.0A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

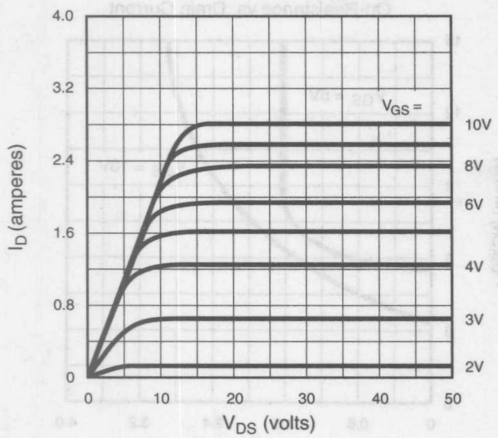
Switching Waveforms and Test Circuit



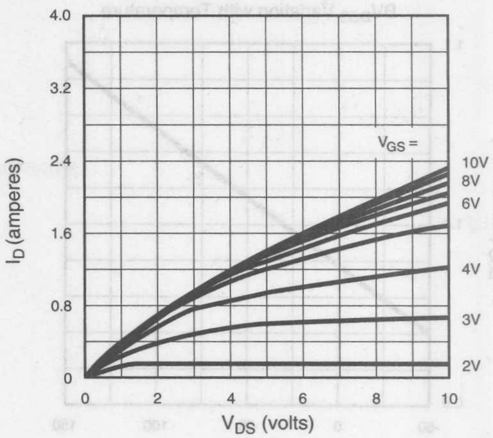


Typical Performance Curves

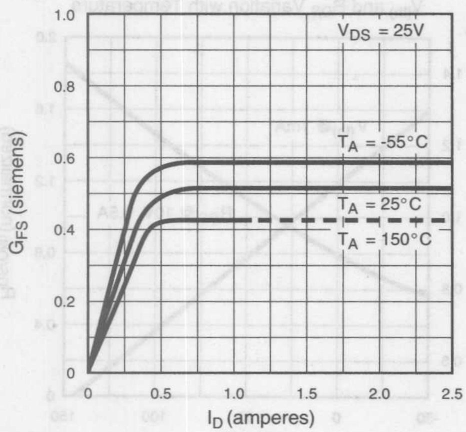
Output Characteristics



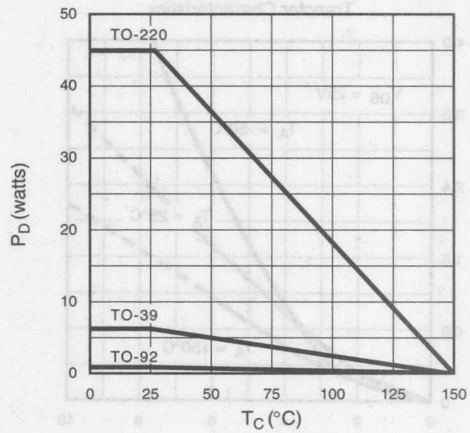
Saturation Characteristics



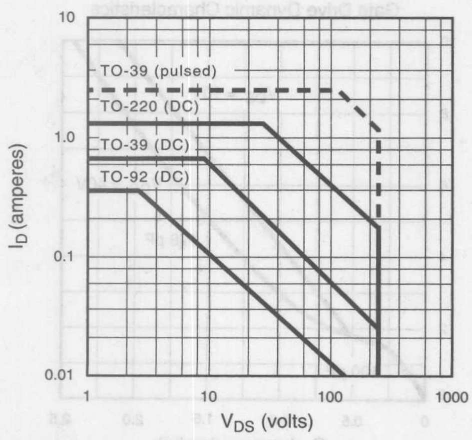
Transconductance vs. Drain Current



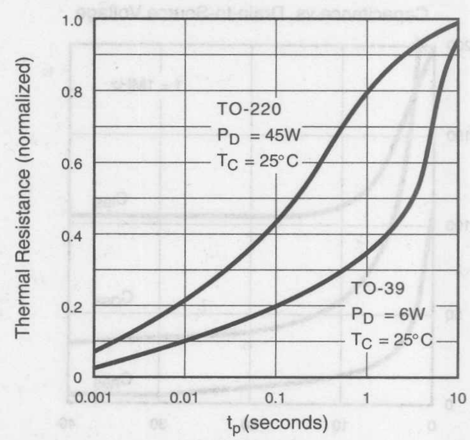
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

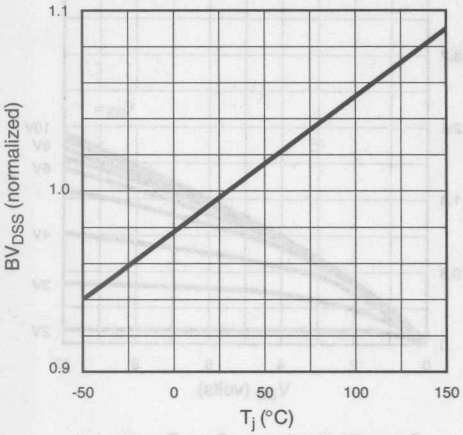


Thermal Response Characteristics

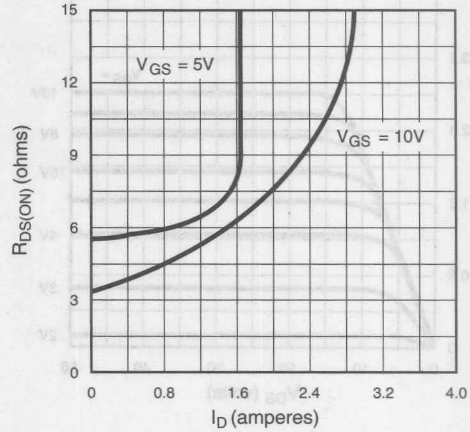


Typical Performance Curves

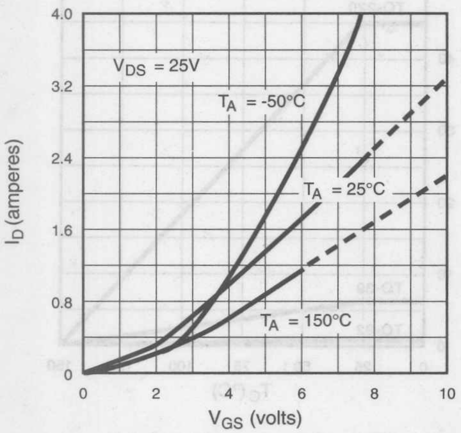
BV_{DSS} Variation with Temperature



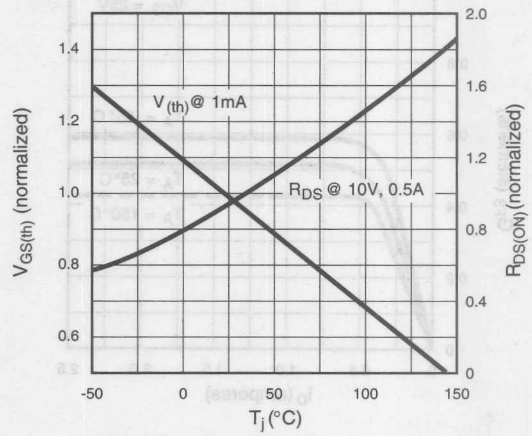
On-Resistance vs. Drain Current



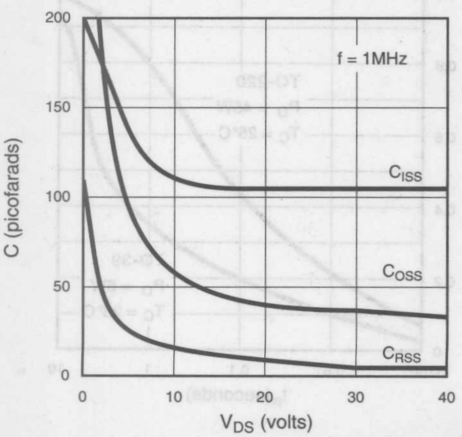
Transfer Characteristics



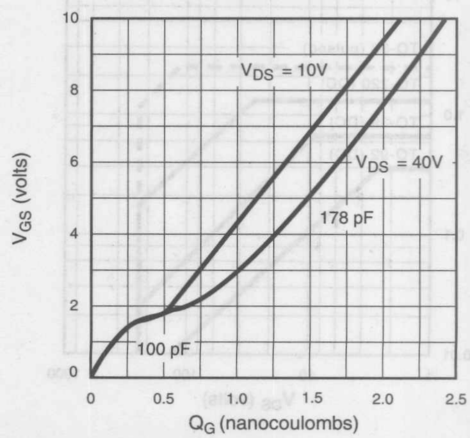
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc. **TN06D**

Low Threshold

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE†
350V	10Ω	1.0A	1.8V	TN0635N3	TN0635ND
400V	10Ω	1.0A	1.8V	TN0640N3	TN0640ND

† MIL visual screening available

Features

- ☐ Low threshold —1.8V max.
- ☐ High input impedance
- ☐ Low input capacitance — 85 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

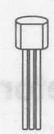
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	200mA	1.5A	1.0W	170	125	200mA	1.5A

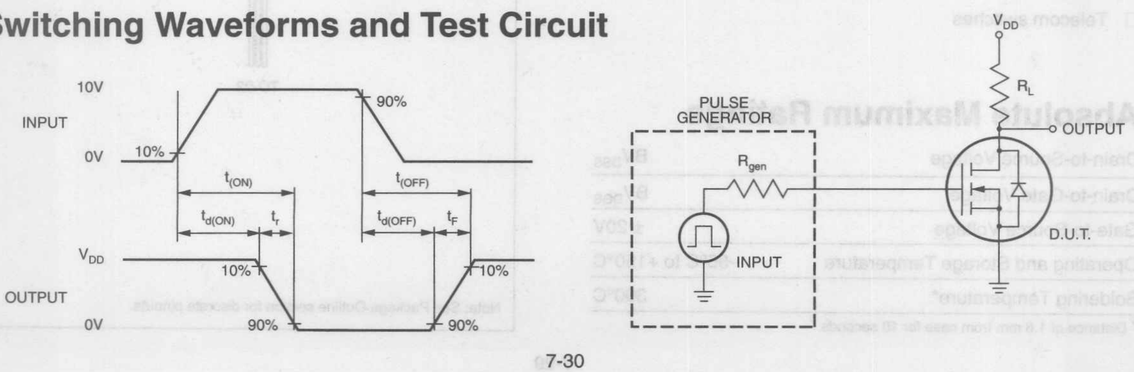
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0640	400			V	$V_{GS} = 0$, $I_D = 100\mu A$
		TN0635	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.8	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-2.5	-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.3	1.5		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			1.0	1.8			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8.0	10	Ω	$V_{GS} = 4.5V$, $I_D = 150mA$
				7.0	10		$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		125	350		m℧	$V_{DS} = 25V$, $I_D = 100mA$
C_{ISS}	Input Capacitance			85	130	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	$V_{DD} = 25V$, $I_D = 1.0A$, $R_{GEN} = 25\Omega$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0$, $I_{SD} = 200mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1.0A$

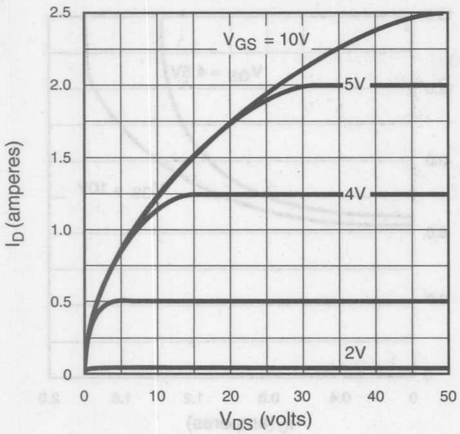
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

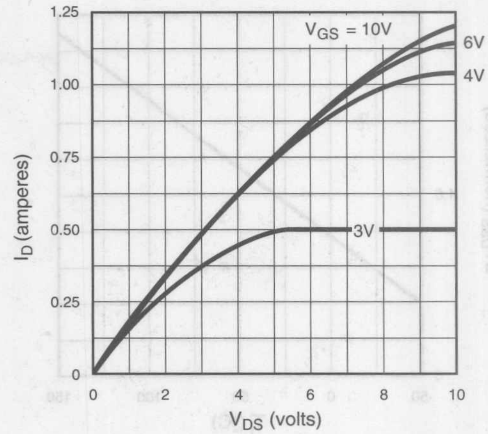


Typical Performance Curves

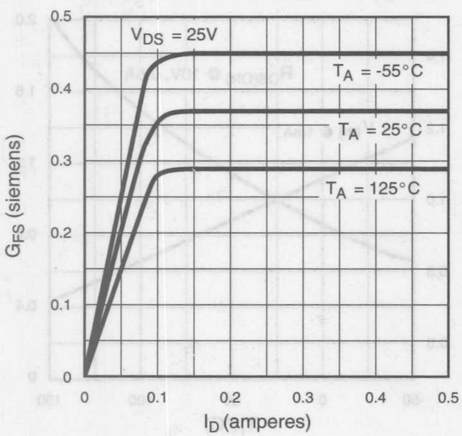
Output Characteristics



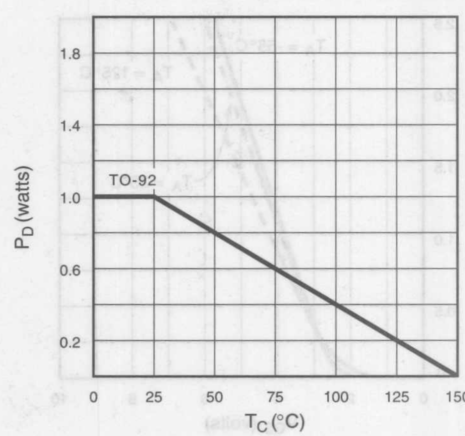
Saturation Characteristics



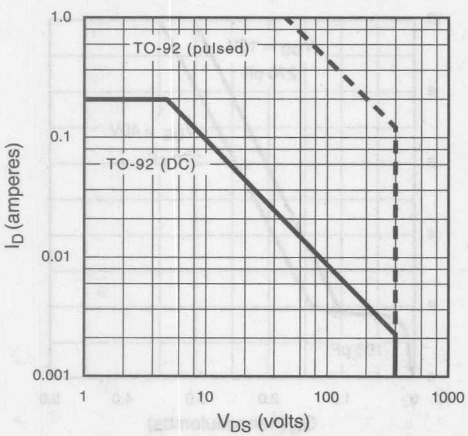
Transconductance vs. Drain Current



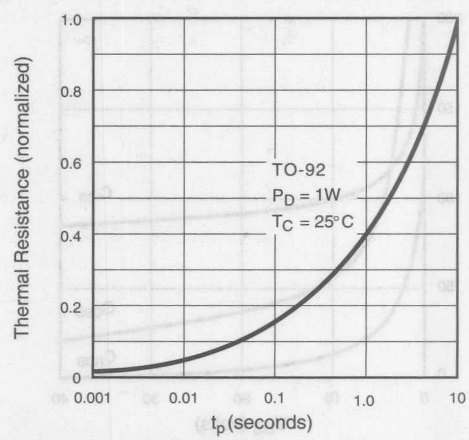
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

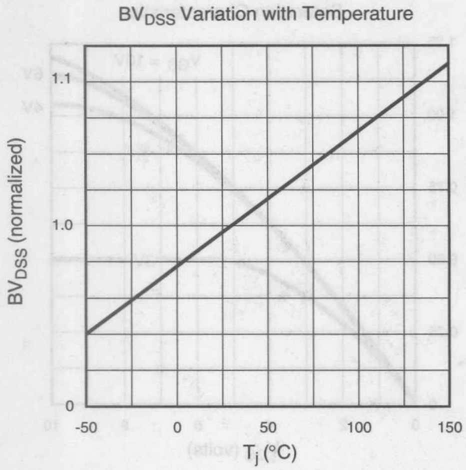


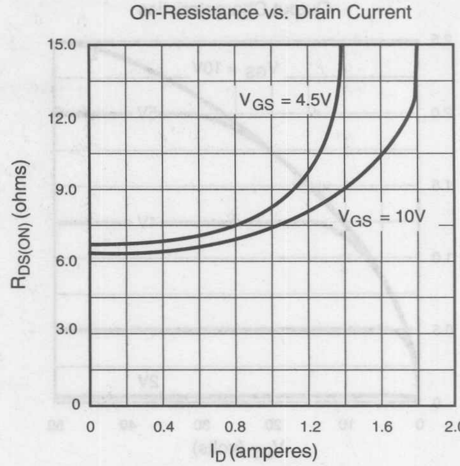
Thermal Response Characteristics

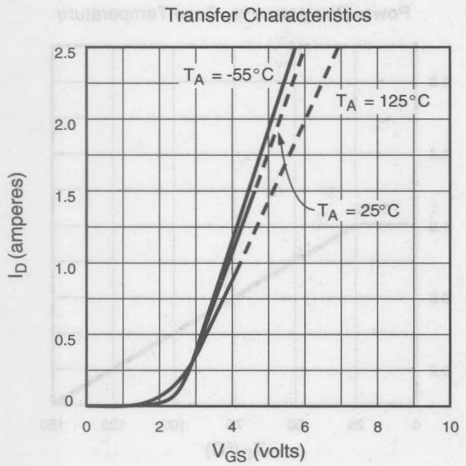


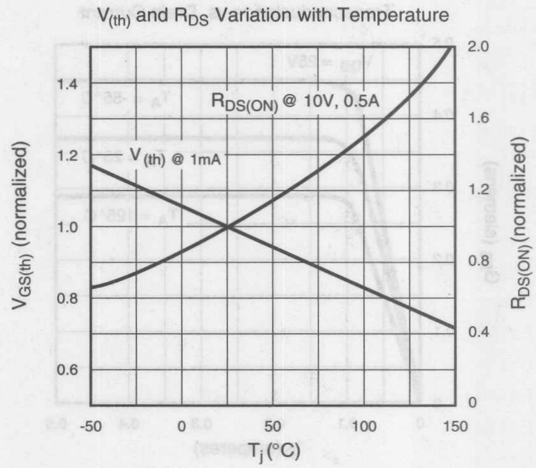
7

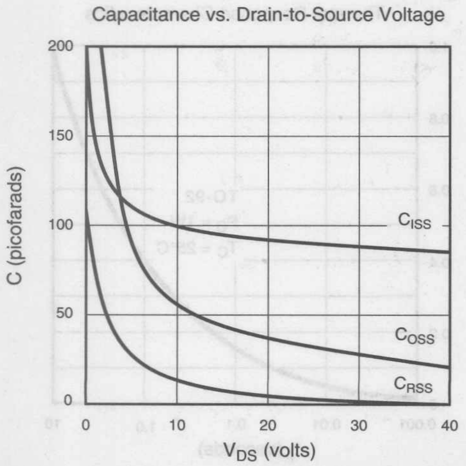
Typical Performance Curves

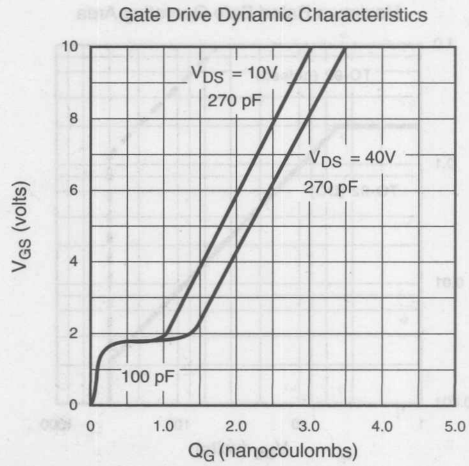












Supertex inc.

Low Threshold

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	SOW-20*	DICE†
20V	0.75Ω	4.0A	1.6V	—	TN0602N3		TN0602ND
20V	0.85Ω	4.0A	1.6V	TN0602N2			—
40V	0.75Ω	4.0A	1.6V	—	TN0604N3		TN0604ND
40V	0.85Ω	4.0A	1.6V	TN0604N2			—
40V	1.0 Ω	4.0A	1.6V	—	—	TN0604WG	—

* Same as SO-20 with 300 mil wide body.
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold — 1.6V max.
- High input impedance
- Low input capacitance — 140pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

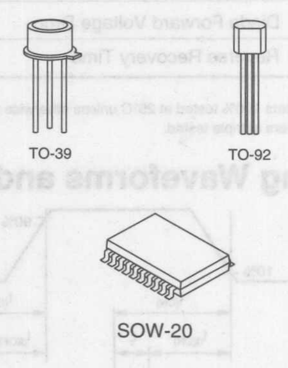
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	2.5A	4.6A	6W	20	125	2.5A	4.6A
TO-92	1.0A	4.6A	1W	125	170	1.0A	4.6A
SOW-20	Refer to Arrays & Special Functions Section.						

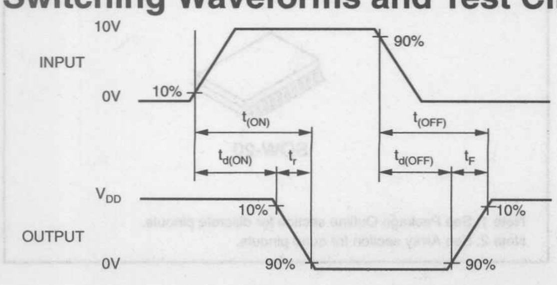
* I_D (continuous) is limited by max rated T_j.

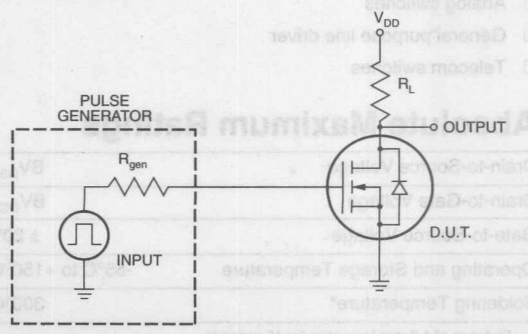
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0604	40			V	$V_{GS} = 0$, $I_D = 2.0mA$
		TN0602	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 2.5mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		1.5	2.1		A	$V_{GS} = 5V$, $V_{DS} = 20V$
			4.0	7.0			$V_{GS} = 10V$, $V_{DS} = 20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	All Packages		0.9	1.5	Ω	$V_{GS} = 5V$, $I_D = 0.75A$
		TO-92		0.6	0.75		$V_{GS} = 10V$, $I_D = 1.5A$
		TO-39			0.85		
		SOW - 20			1.0		
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.5	0.75	%/°C	$V_{GS} = 10V$, $I_D = 2.0A$
G_{FS}	Forward Transconductance		0.5	0.8		℧	$V_{DS} = 20V$, $I_D = 2.0A$
C_{ISS}	Input Capacitance			140	190	pF	$V_{GS} = 0$, $V_{DS} = 20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75	110		
C_{RSS}	Reverse Transfer Capacitance			25	50		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 20V$ $I_D = 0.5A$ $R_{GEN} = 25\Omega$
t_r	Rise Time				6.0		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2: All A.C. parameters sample tested.

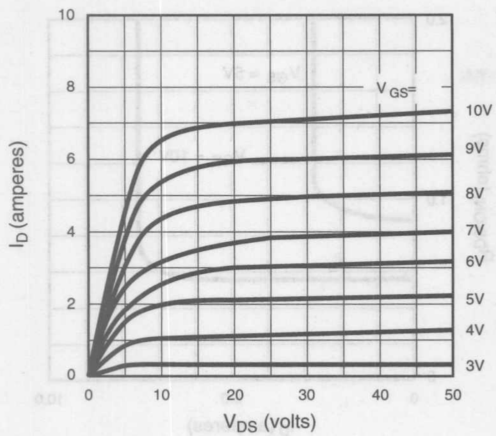
Switching Waveforms and Test Circuit



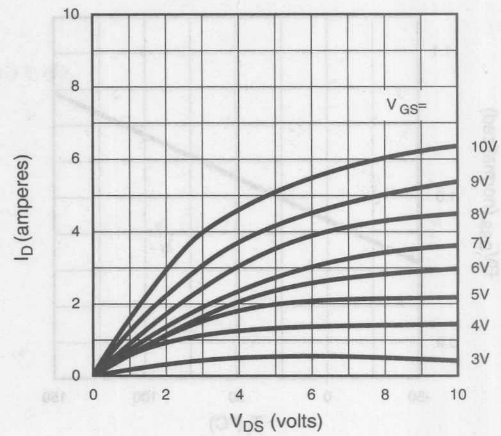


Typical Performance Curves

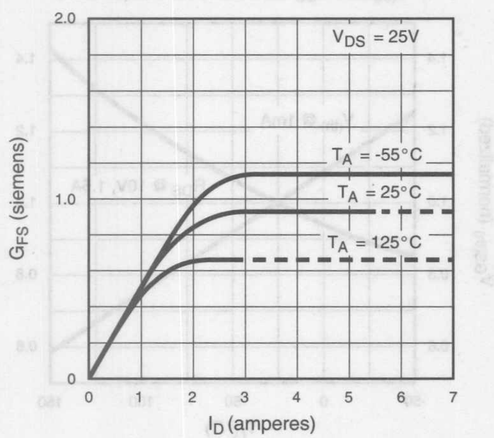
Output Characteristics



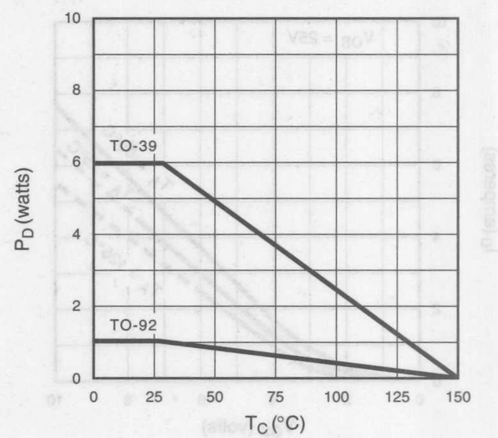
Saturation Characteristics



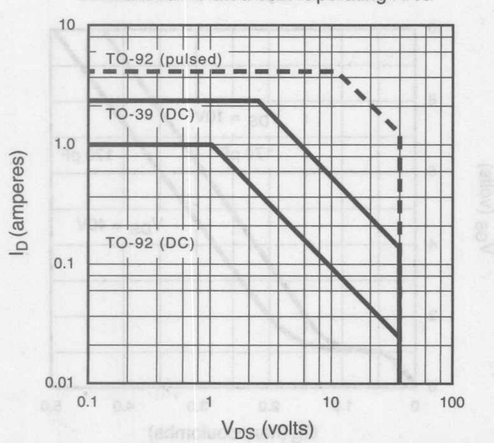
Transconductance vs. Drain Current



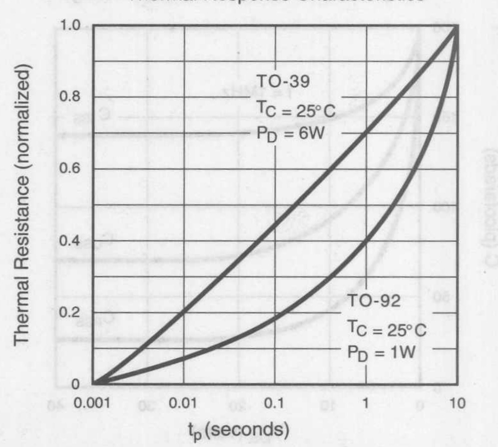
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

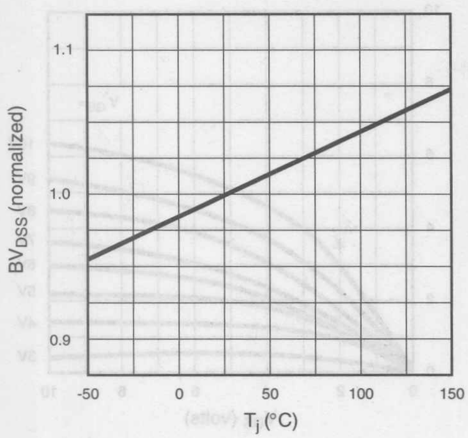


Thermal Response Characteristics

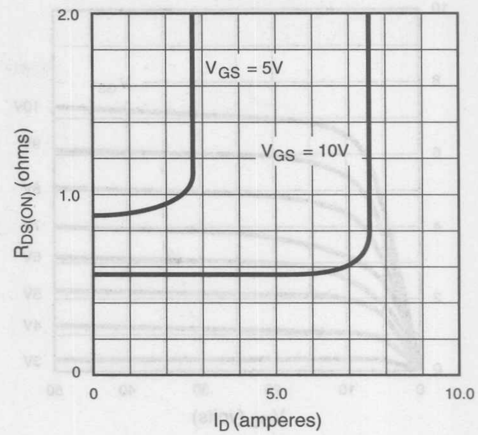


Typical Performance Curves

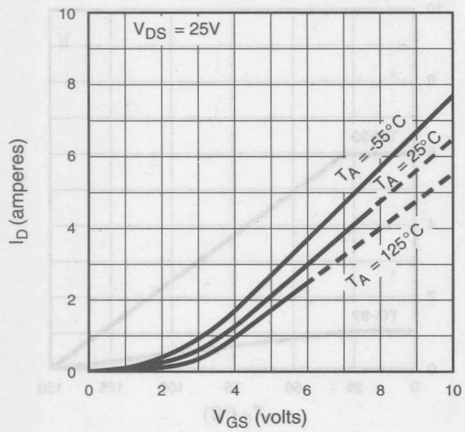
BV_{DSS} Variation with Temperature



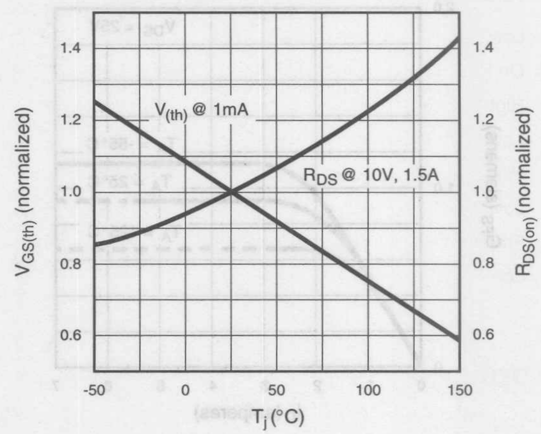
On-Resistance vs. Drain Current



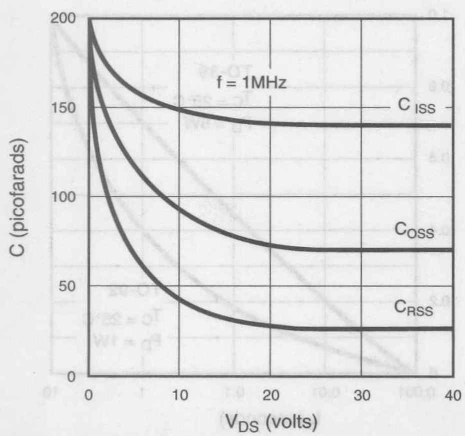
Transfer Characteristics



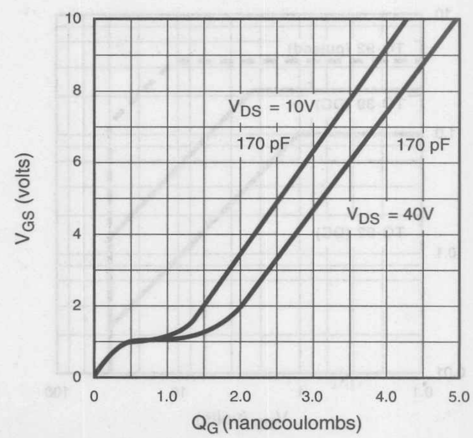
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package TO-92	DICE[†]
20V	1.3Ω	0.5A	1.0V	TN0702N3	TN0702ND

[†] MIL visual screening available

Features

- ☐ Low threshold — 1.0 volt max
- ☐ On resistance guaranteed at V_{GS} = 2, 3, and 5 volts
- ☐ High input impedance
- ☐ Low input capacitance —130 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

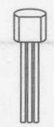
*Distance of 1.6 mm from case for 10 seconds maximum.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	0.6A	1.0A	1W	125	170	0.6A	1.0A

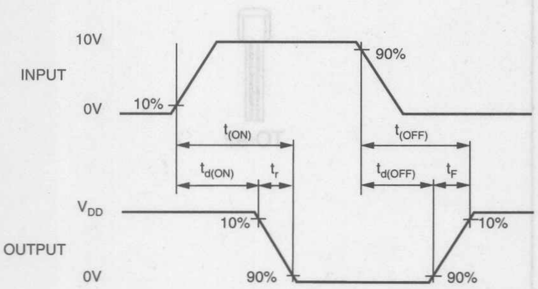
* I_D (continuous) is limited by max rated T_j.

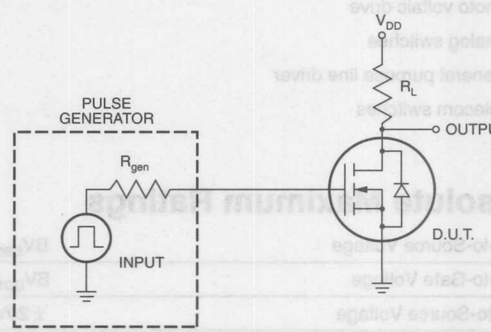
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20			V	$V_{GS} = 0$, $I_D = 1mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.8	1.0	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			100	nA	$V_{DS} = 20V$, $V_{GS} = 0V$
				100	µA	V_{DS} = 0.8 Max Rating, $V_{GS} = 0V$, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	0.5	1.0		A	$V_{GS} = V_{DS} = 5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		4.0	5.0	Ω	$V_{GS} = 2V$, $I_D = 50mA$
			1.9	2.5		$V_{GS} = 3V$, $I_D = 200mA$
			1.0	1.3		$V_{GS} = 5V$, $I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/°C	$V_{GS} = 5V$, $I_D = 500mA$
G_{FS}	Forward Transconductance	100	500		m℧	$V_{DS} = 5V$, $I_D = 500mA$
C_{ISS}	Input Capacitance		130	200	pF	$V_{GS} = 0V$, $V_{DS} = 20V$, f = 1MHz
C_{OSS}	Common Source Output Capacitance		70	125		
C_{RSS}	Reverse Transfer Capacitance		30	60		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = 20V$, $I_D = 0.5A$, $R_{GEN} = 25\Omega$
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			1.0	V	$V_{GS} = 0V$, $I_{SD} = 0.5A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwide stated. (Pulse test: 300 µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

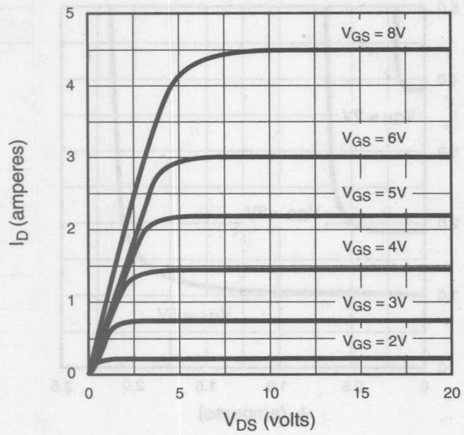
Switching Waveforms and Test Circuit



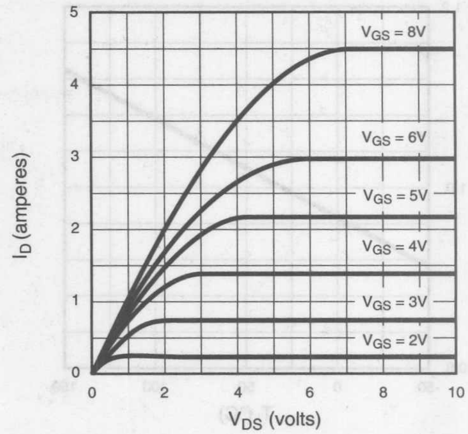


Typical Performance Curves

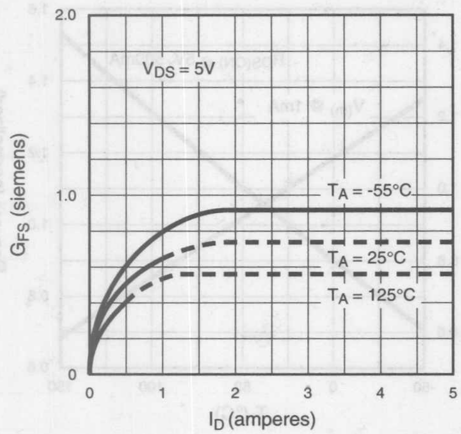
Output Characteristics



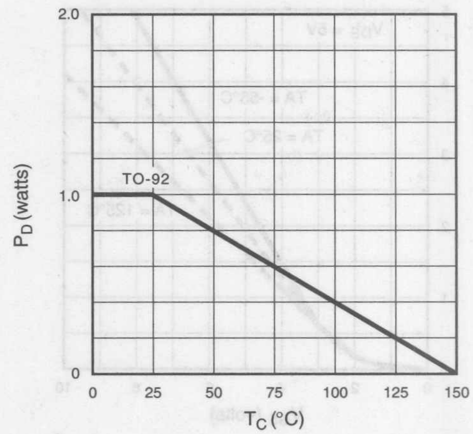
Saturation Characteristics



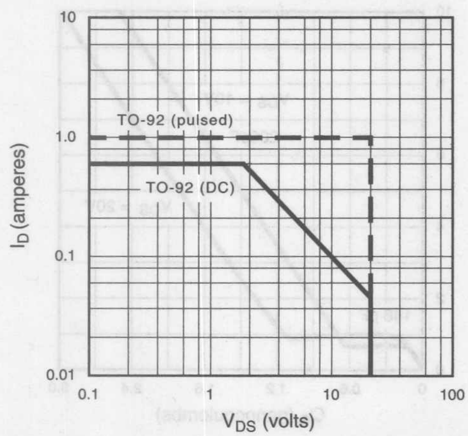
Transconductance vs. Drain Current



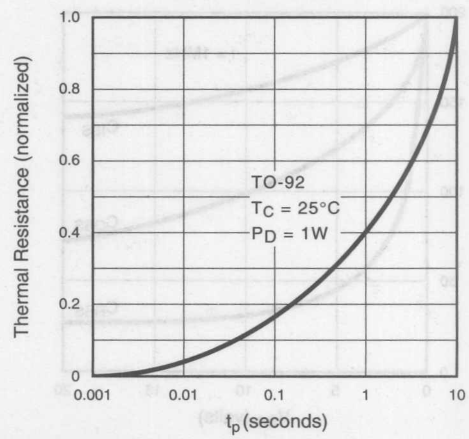
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

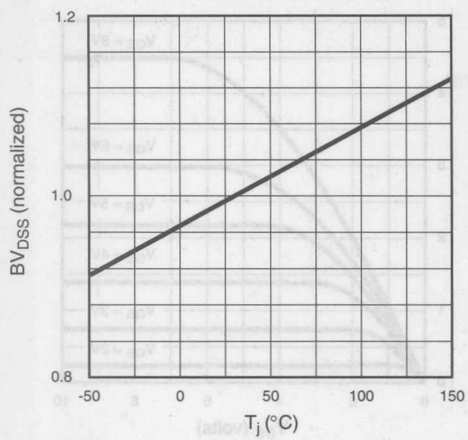


Thermal Response Characteristics

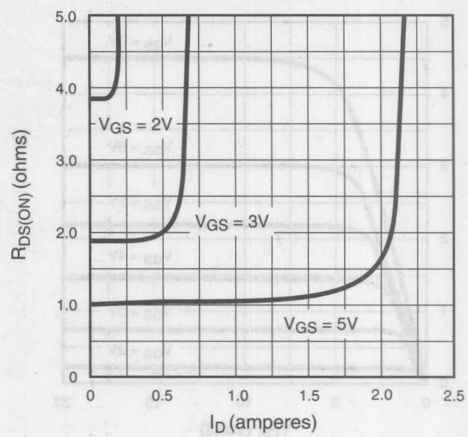


Typical Performance Curves

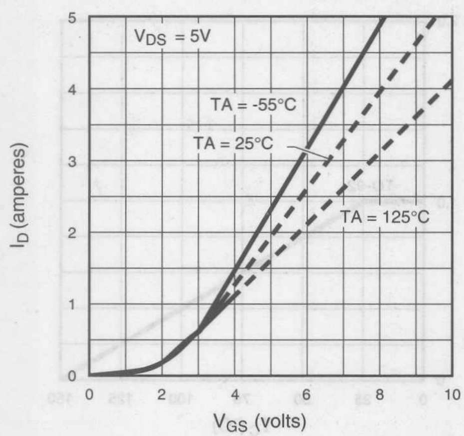
BV_{DSS} Variation with Temperature



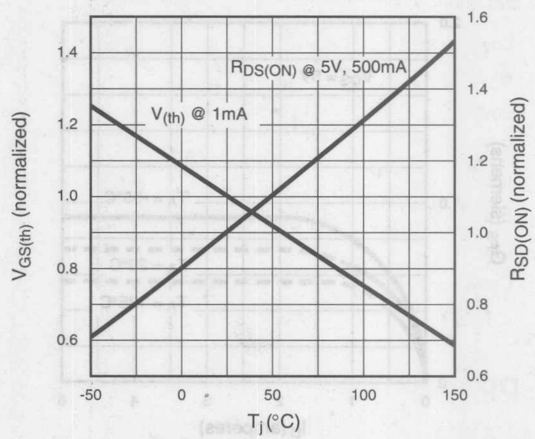
On-Resistance vs. Drain Current



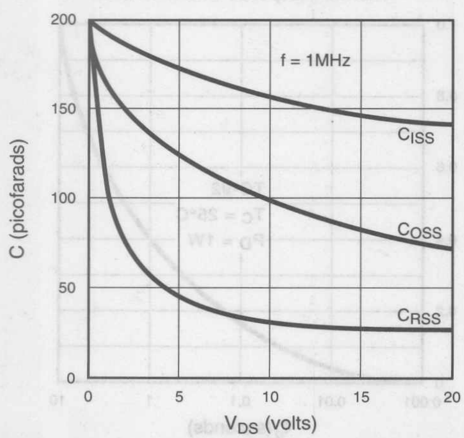
Transfer Characteristics



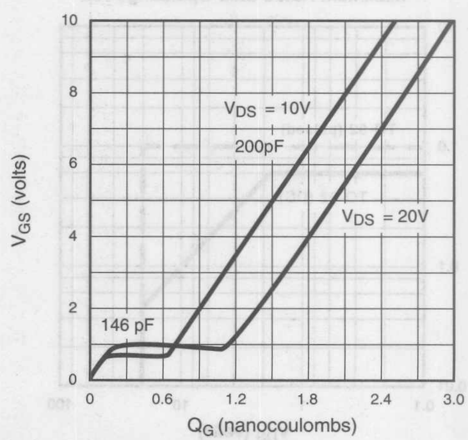
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
60V	1.5Ω	1.6V	3.0A	—	TN2506ND
100V	1.5Ω	1.6V	3.0A	TN2510N8	TN2510ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold —1.6V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

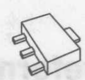
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	1.3A	5.0A	1.6W†	15	78†	1.3A	5.0A

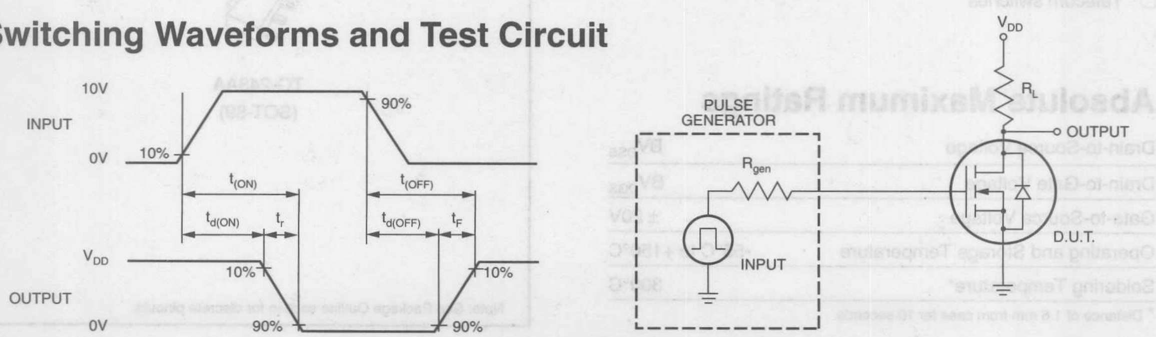
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2510	100			V	$V_{GS} = 0$, $I_D = 2mA$
		TN2506	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		1.2	2.0		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			3.0	6.0			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.5	2.0	Ω	$V_{GS} = 5V$, $I_D = 750mA$
				1.0	1.5		$V_{GS} = 10V$, $I_D = 750mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance		0.4	0.8		℧	$V_{DS} = 25V$, $I_D = 1.0A$
C_{ISS}	Input Capacitance			70	125	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30	70		
C_{RSS}	Reverse Transfer Capacitance			15	25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 1.5A$, $R_{GEN} = 25Ω$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0$, $I_{SD} = 1.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1.5A$

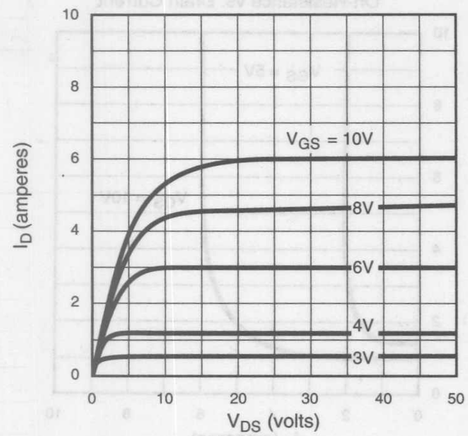
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

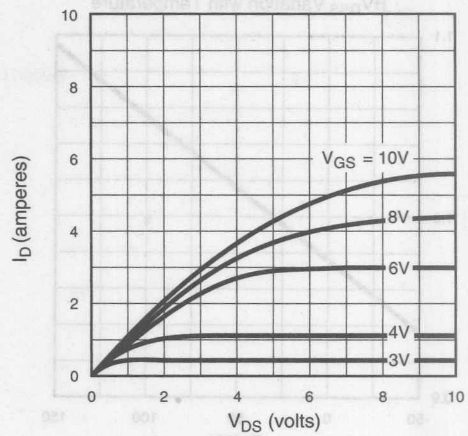


Typical Performance Curves

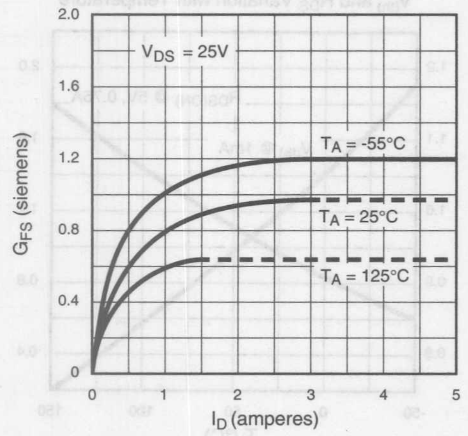
Output Characteristics



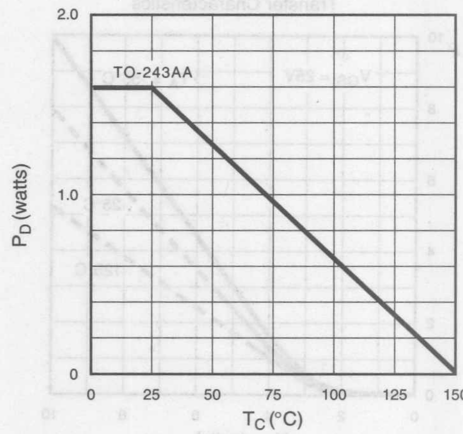
Saturation Characteristics



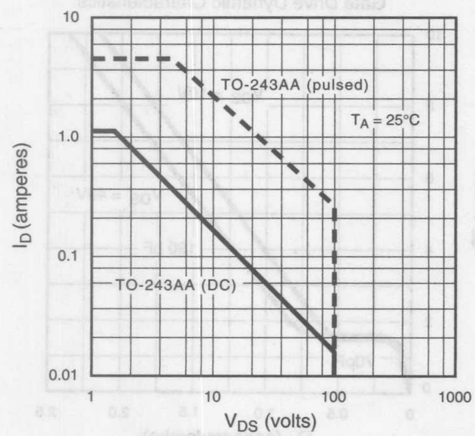
Transconductance vs. Drain Current



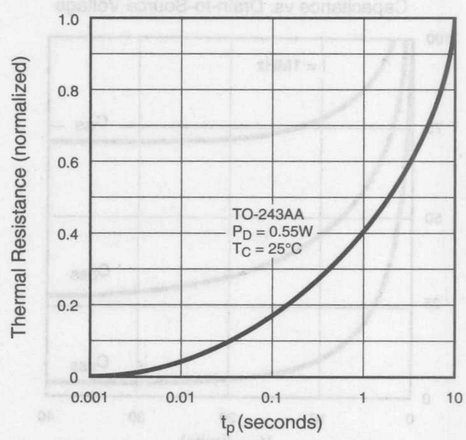
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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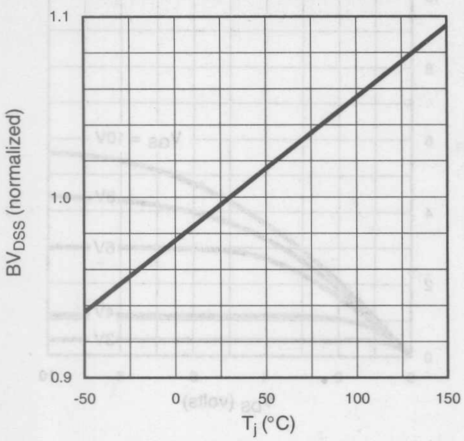
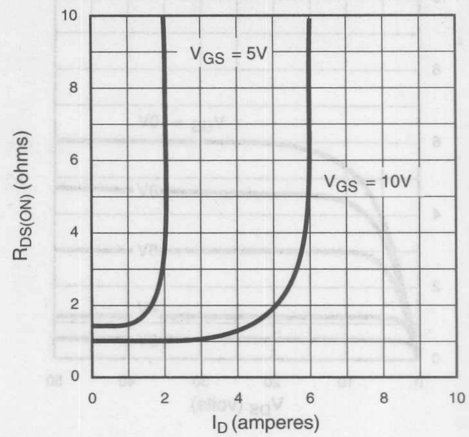
Typical Performance Curves

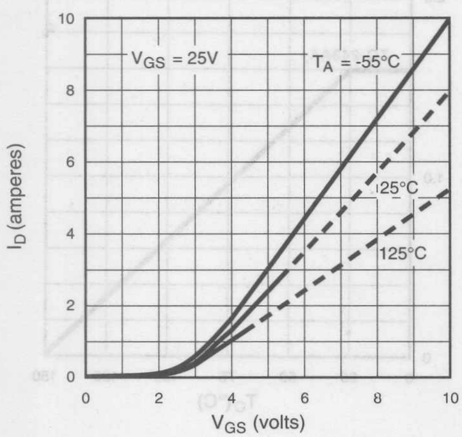
BV_{DSS} Variation with Temperature



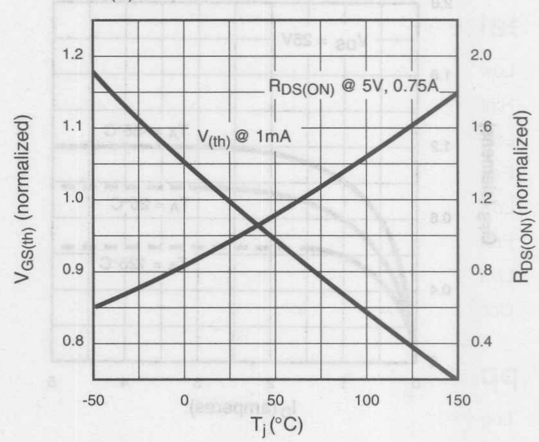
On-Resistance vs. Drain Current



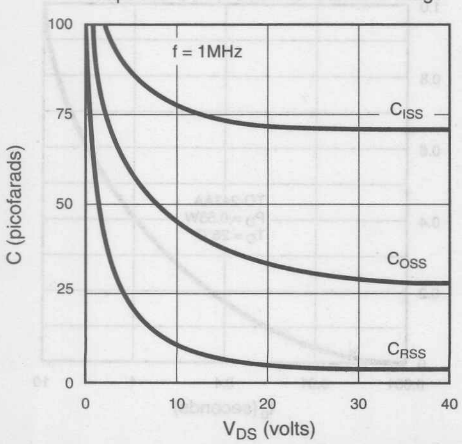
Transfer Characteristics



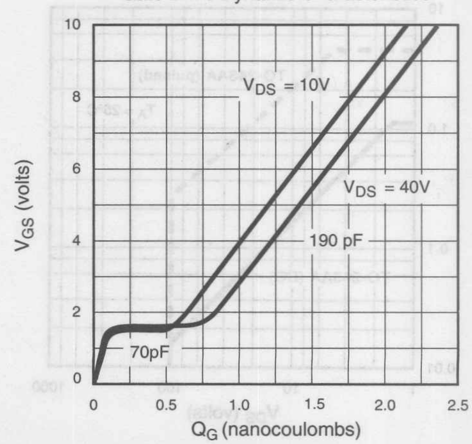
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE
200V	6Ω	2.0V	1.0A	—	TN2520ND
240V	6Ω	2.0V	1.0A	TN2524N8	TN2524ND

* Same as SOT-89.

Features

- ☐ Low threshold — 2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

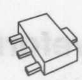
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	0.8A	2.0A	1.6W†	15	78†	0.8A	2.0A

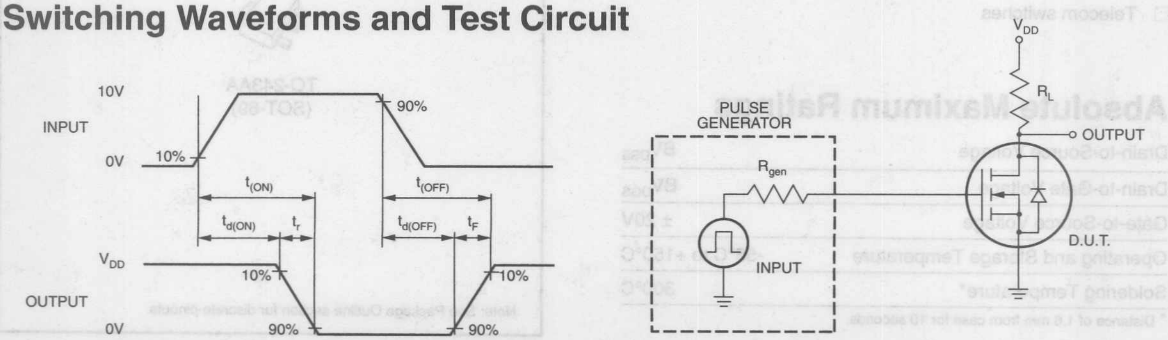
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2524	240			V	$V_{GS} = 0$, $I_D = 2mA$
		TN2520	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.5	1.9		A	$V_{GS} = 4.5V$, $V_{DS} = 25V$
			1.0	2.8			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.0	6.0	Ω	$V_{GS} = 4.5V$, $I_D = 250mA$
				4.0	6.0		$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.4	%/°C	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance		300	600		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			65	125	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			35	70		
C_{RSS}	Reverse Transfer Capacitance			10	25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 1.0A$, $R_{GEN} = 25Ω$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1.0A$

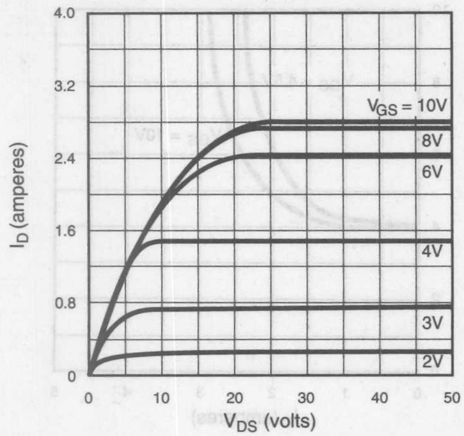
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

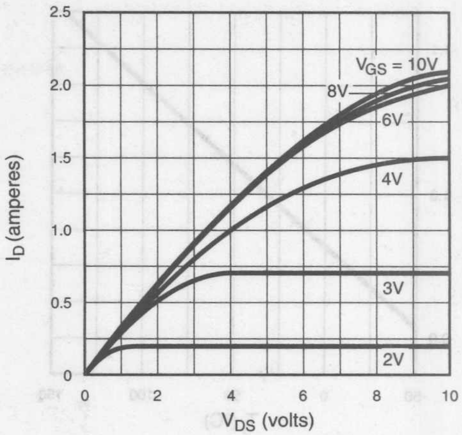


Typical Performance Curves

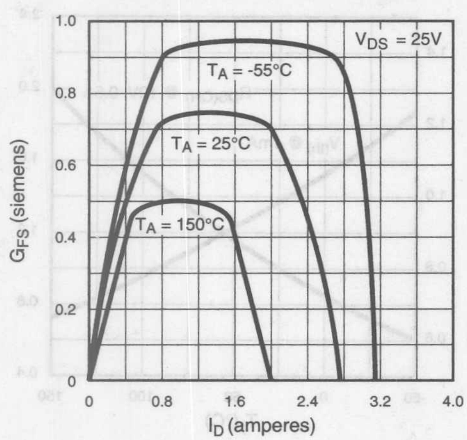
Output Characteristics



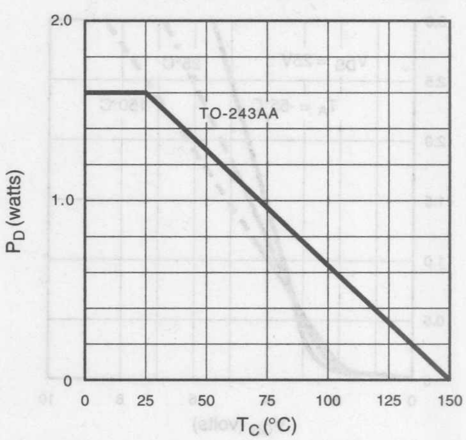
Saturation Characteristics



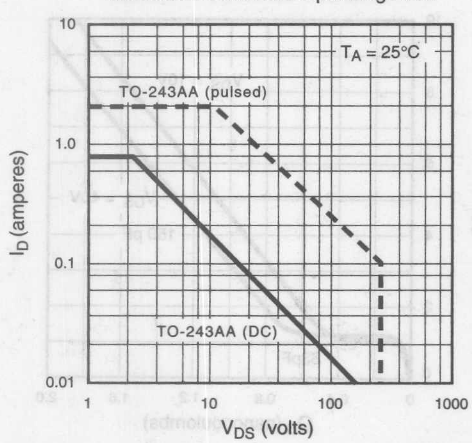
Transconductance vs. Drain Current



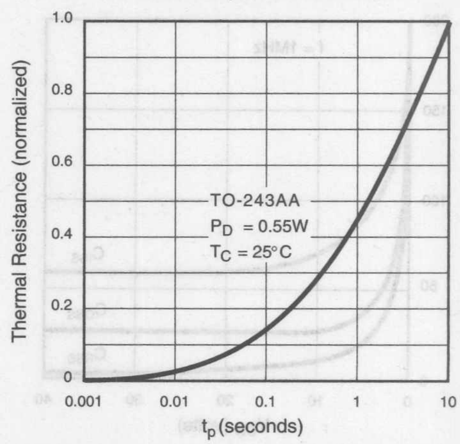
Power Dissipation vs. AmbientTemperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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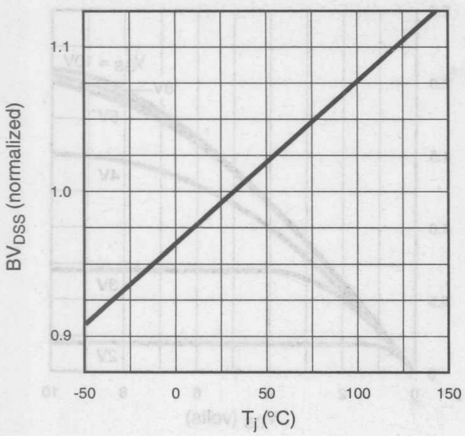
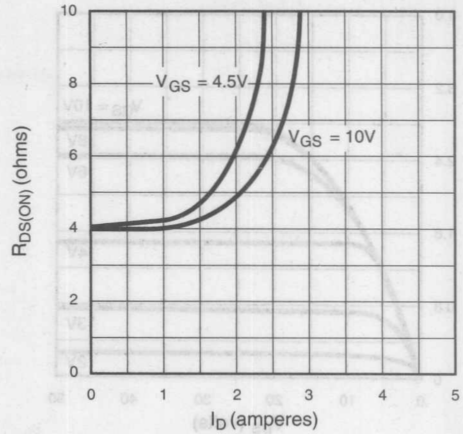
Typical Performance Curves

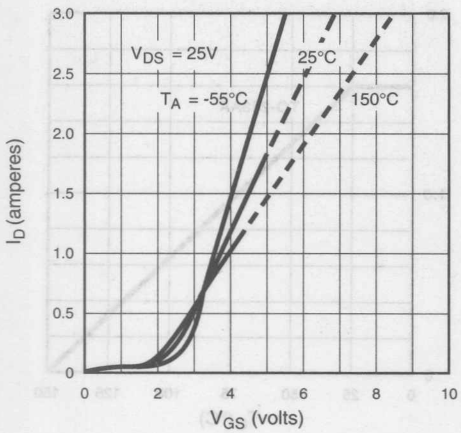
BV_{DSS} Variation with Temperature



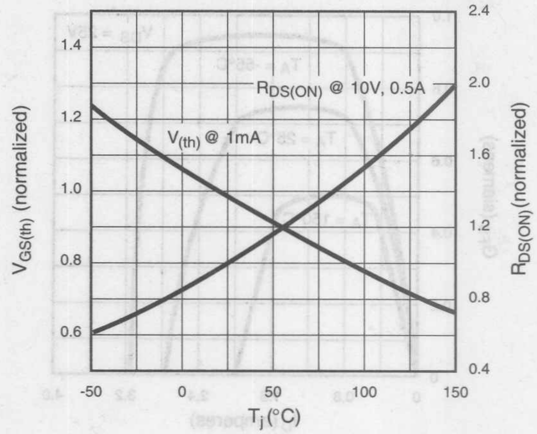
On-Resistance vs. Drain Current



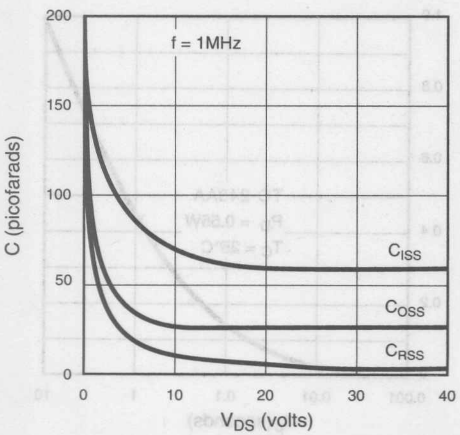
Transfer Characteristics



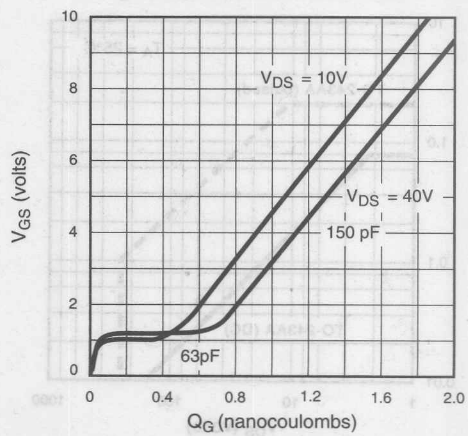
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
350V	12Ω	1.8V	1.0A	—	TN2535ND
400V	12Ω	1.8V	1.0A	TN2540N8	TN2540ND

* Same as SOT-89.
† MIL visual screening available.

Features

- Low threshold — 1.8V max.
- High input impedance
- Low input capacitance — 125 pF max.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

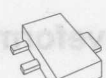
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	570mA	1.8A	1.6W†	15	78†	570mA	1.8A

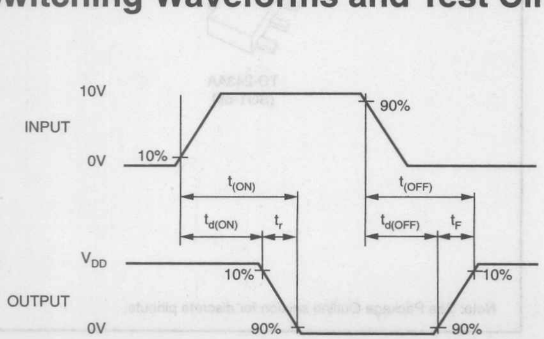
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

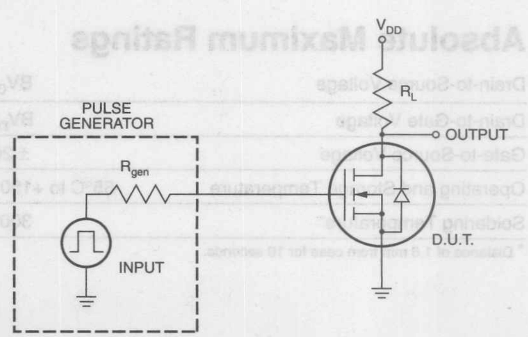
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2540	400			V	$V_{GS} = 0$, $I_D = 100\mu A$
		TN2535	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.8	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-2.5	-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.3	0.5		A	$V_{GS} = 4.5V$, $V_{DS} = 25V$
			1.0	1.4			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8.0	12	Ω	$V_{GS} = 4.5V$, $I_D = 150mA$
				8.0	12		$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		125	200		m℧	$V_{DS} = 25V$, $I_D = 100mA$
C_{ISS}	Input Capacitance			95	125	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	70		
C_{RSS}	Reverse Transfer Capacitance			10	25		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	$V_{DD} = 25V$, $I_D = 1A$, $R_{GEN} = 25\Omega$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0$, $I_{SD} = 200mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

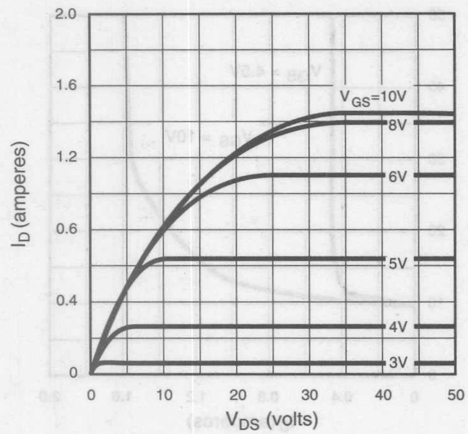
Switching Waveforms and Test Circuit



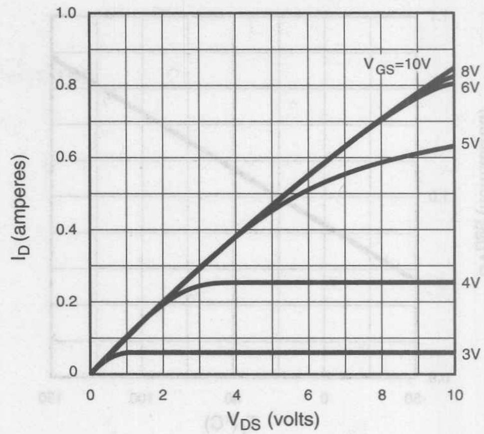


Typical Performance Curves

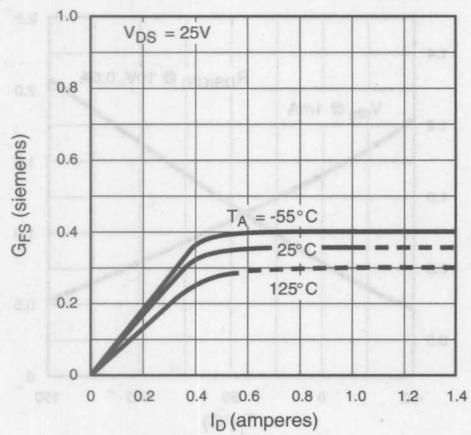
Output Characteristics



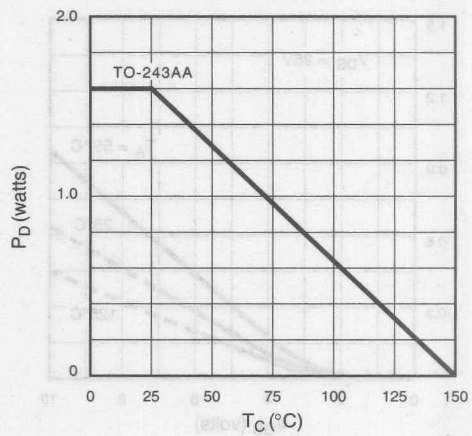
Saturation Characteristics



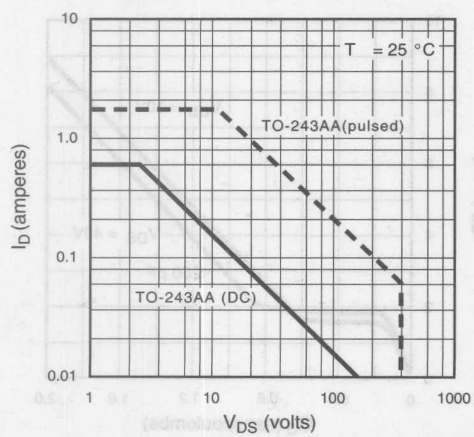
Transconductance vs. Drain Current



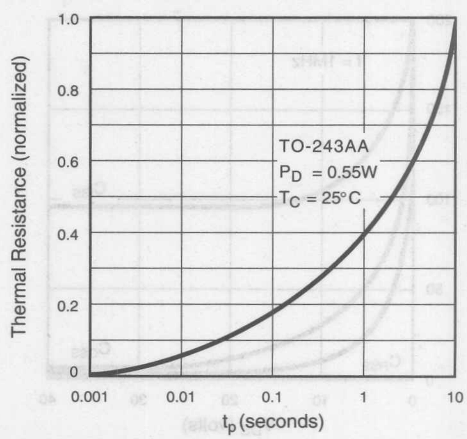
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

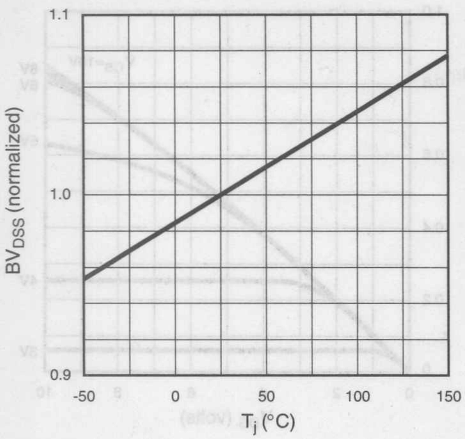


Thermal Response Characteristics

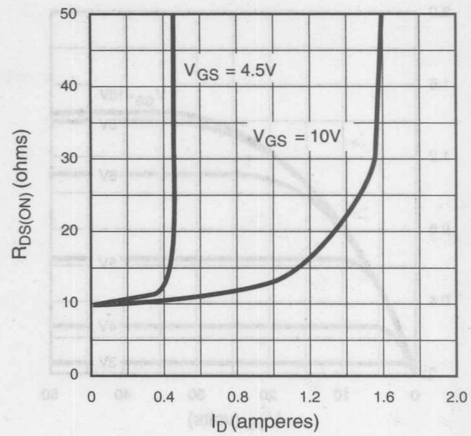


Typical Performance Curves

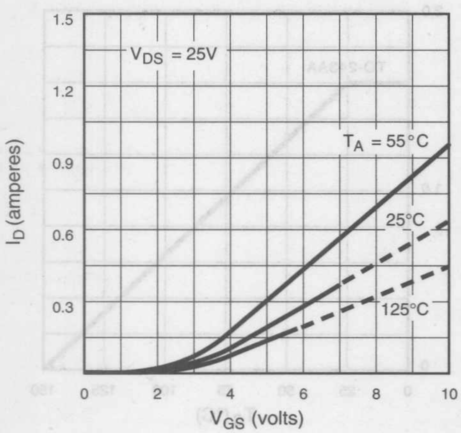
BV_{DSS} Variation with Temperature



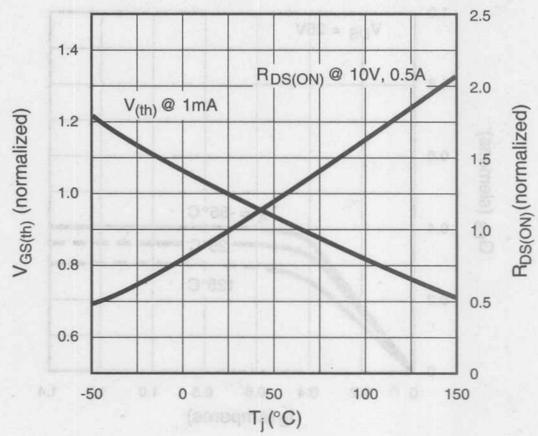
On-Resistance vs. Drain Current



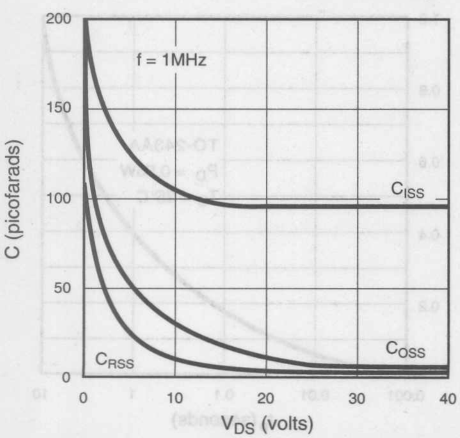
Transfer Characteristics



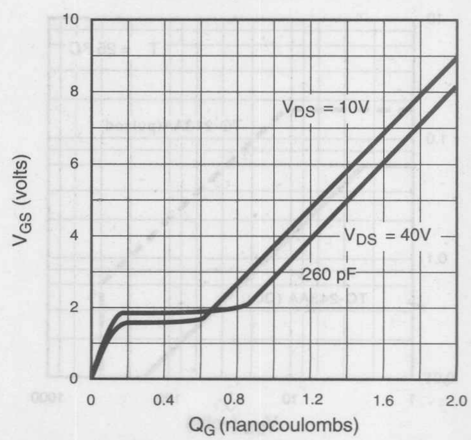
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-243AA*	DICE†
20V	1.0Ω	1.6V	4.0A	—	TN2502ND
40V	1.0Ω	1.6V	4.0A	TN2504N8	TN2504ND

* Same as SOT-89.
† MIL visual screening available.

Features

- Low threshold — 1.6V max.
- High input impedance
- Low input capacitance — 125 pF max.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

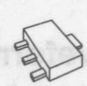
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	2.0A	4.5A	1.6W†	15	78†	2.0A	4.5A

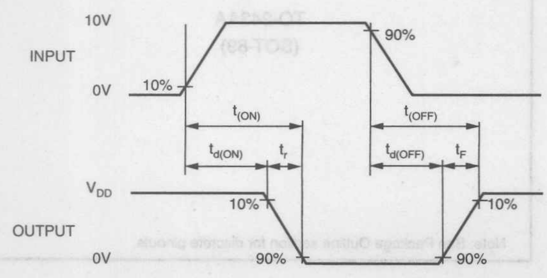
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

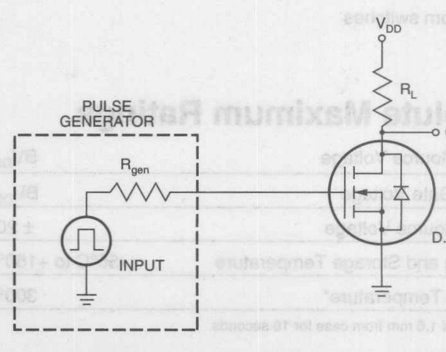
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2504	40			V	$V_{GS} = 0$, $I_D = 2mA$
		TN2502	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		1.0	1.7		A	$V_{GS} = 5V$, $V_{DS} = 15V$
			4.0	4.5			$V_{GS} = 10V$, $V_{DS} = 15V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.25	1.5	Ω	$V_{GS} = 5V$, $I_D = 300mA$
				0.8	1.0		$V_{GS} = 10V$, $I_D = 1.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 1.5A$
G_{FS}	Forward Transconductance		0.5	0.7		℧	$V_{DS} = 15V$, $I_D = 2.0A$
C_{ISS}	Input Capacitance			70	125	pF	$V_{GS} = 0$, $V_{DS} = 20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	70		
C_{RSS}	Reverse Transfer Capacitance			20	25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 20V$, $I_D = 500mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

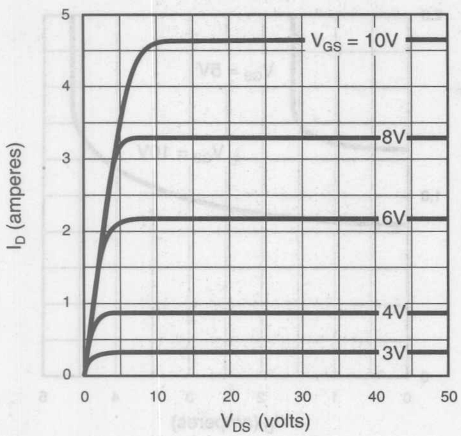
Switching Waveforms and Test Circuit



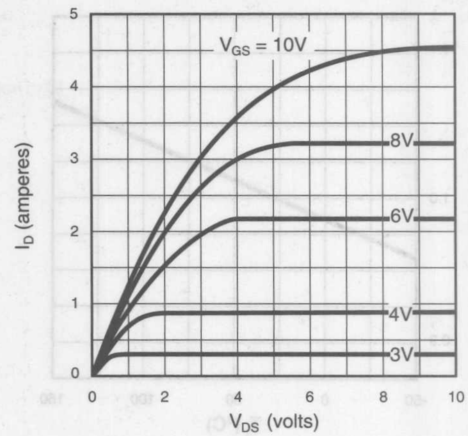


Typical Performance Curves

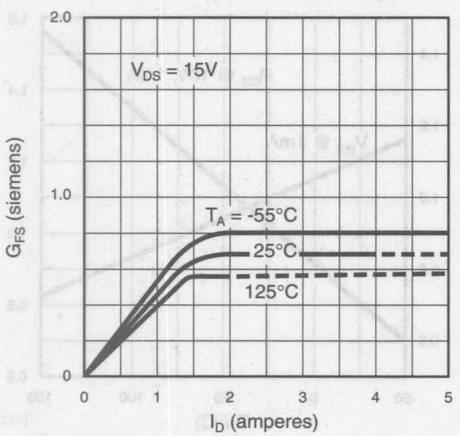
Output Characteristics



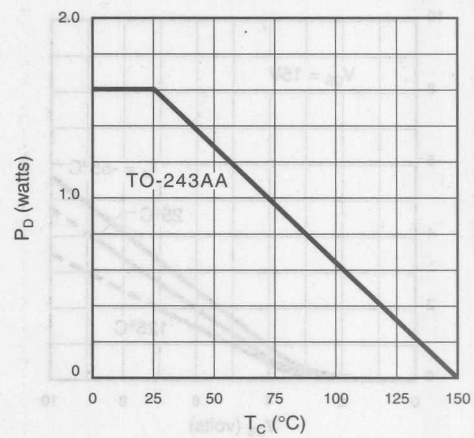
Saturation Characteristics



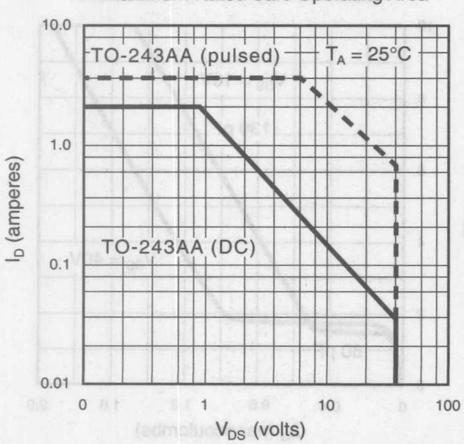
Transconductance vs. Drain Current



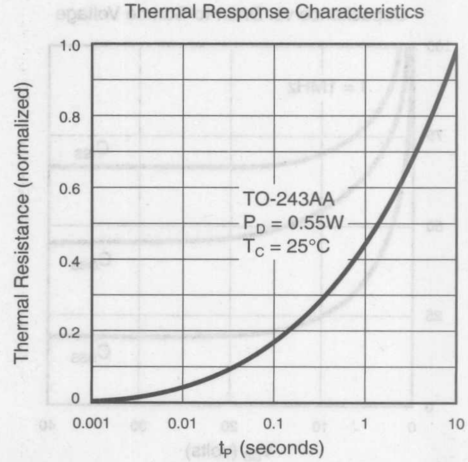
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

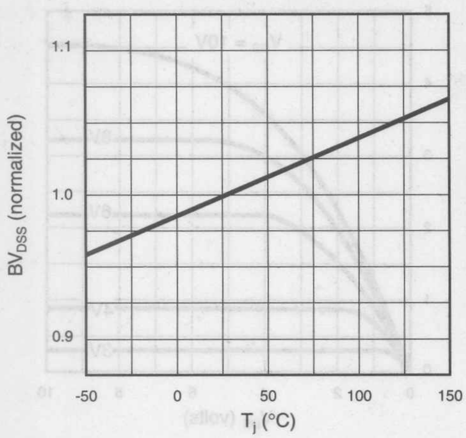


Thermal Response Characteristics

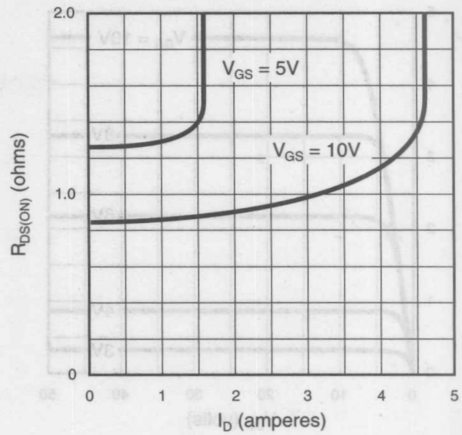


Typical Performance Curves

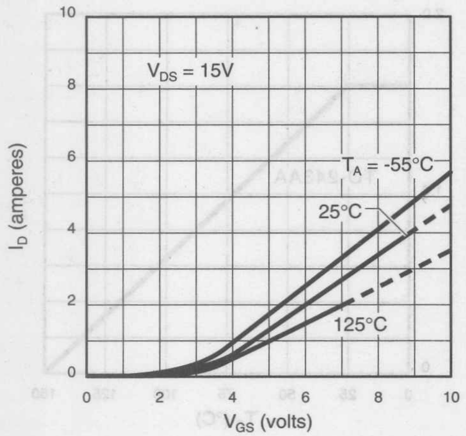
BV$_{DSS}$ Variation with Temperature



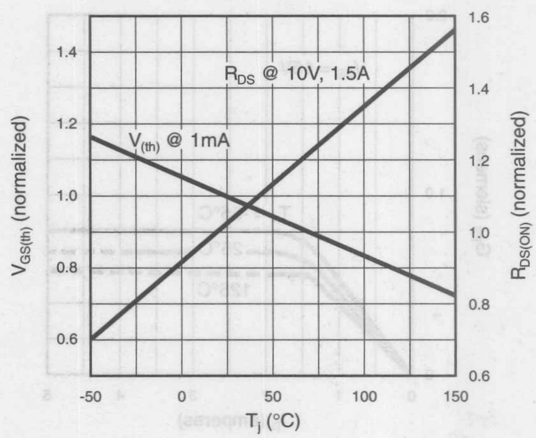
On-Resistance vs. Drain Current



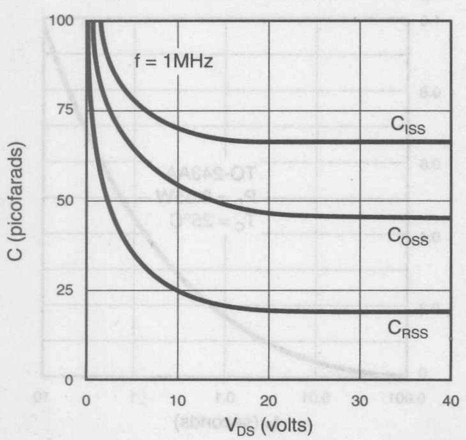
Transfer Characteristics



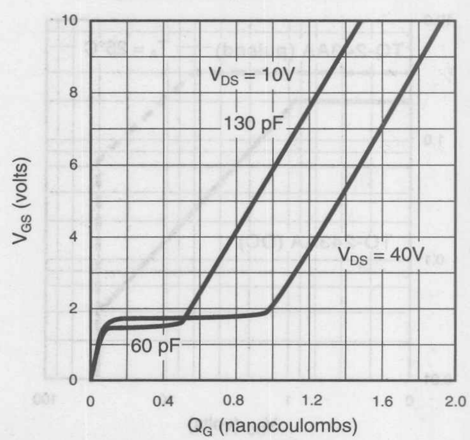
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

TN25U

Low Threshold

Preliminary

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS\,(th)}$ (max)	Order Number /Package	
				TO-243AA*	DICE†
18V	2.5Ω	250mA	0.8V	TN2501N8	TN2501ND

*Same as SOT-89.
†MIL visual screening available.

Features

- ☐ Low threshold — 0.8V max.
- ☐ High input impedance
- ☐ Low input capacitance — 110pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 15V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

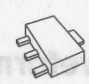
*Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	400mA	750mA	1.6W†	15	78†	400mA	750mA

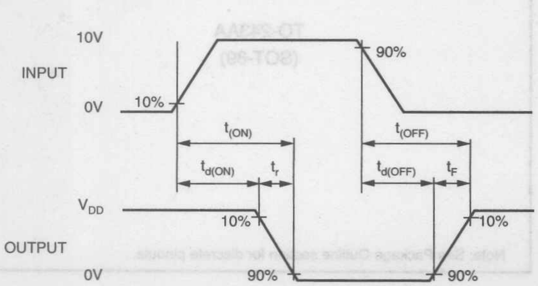
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

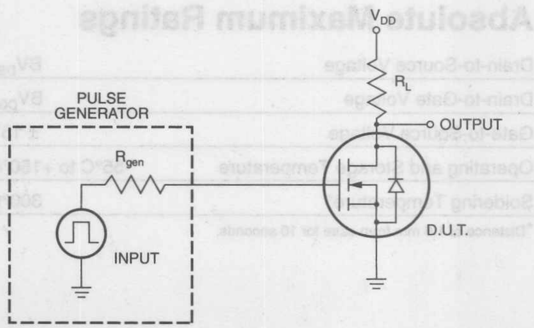
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	18			V	$V_{GS} = 0$, $I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.3		0.8	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
				1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	250	600		mA	$V_{GS} = V_{DS} = 3.0V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			25	Ω	$V_{GS} = 1.0V$, $I_D = 3.0mA$
				3.5	Ω	$V_{GS} = 2.0V$, $I_D = 50mA$
				2.5	Ω	$V_{GS} = 3.0V$, $I_D = 200mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/°C	$V_{GS} = 3.0V$, $I_D = 200mA$
G_{FS}	Forward Transconductance	0.15	0.3		℧	$V_{DS} = 3.0V$, $I_D = 200mA$
C_{ISS}	Input Capacitance			110	pF	$V_{GS} = 0$, $V_{DS} = 15V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			60	pF	
C_{RSS}	Reverse Transfer Capacitance			35	pF	
$t_{d(ON)}$	Turn-ON Delay Time			5.0	ns	$V_{DD} = 15V$, $I_D = 250mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time			15	ns	
$t_{d(OFF)}$	Turn-OFF Delay Time			15	ns	
t_f	Fall Time			8.0	ns	
V_{SD}	Diode Forward Voltage Drop		1.1	1.8	V	$V_{GS} = 0$, $I_{SD} = 200mA$
t_{rr}	Reverse Recovery Time		100		ns	$V_{GS} = 0$, $I_{SD} = 200mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µsec pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

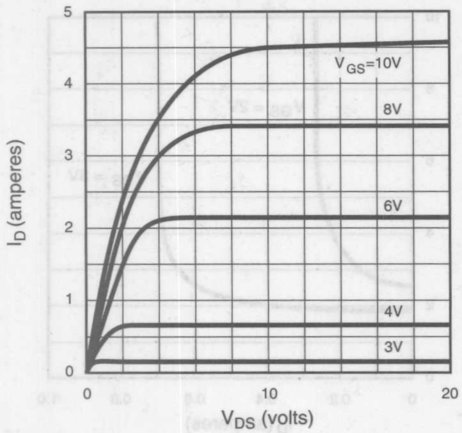
Switching Waveforms and Test Circuit



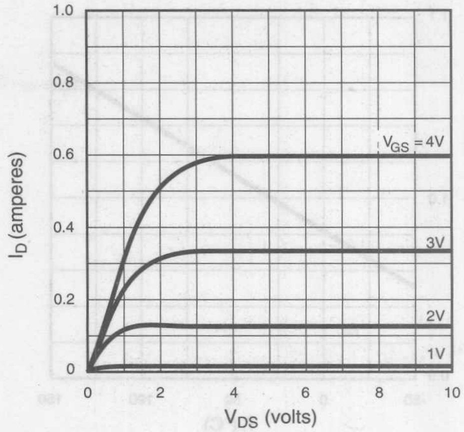


Typical Performance Curves

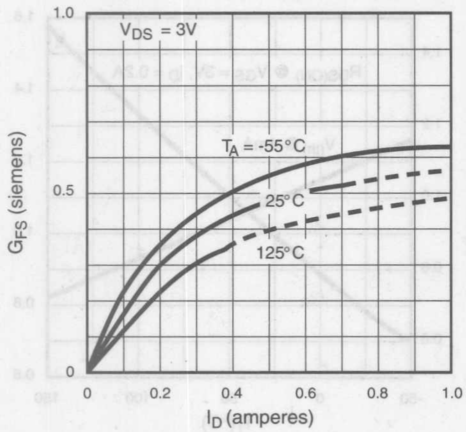
Output Characteristics



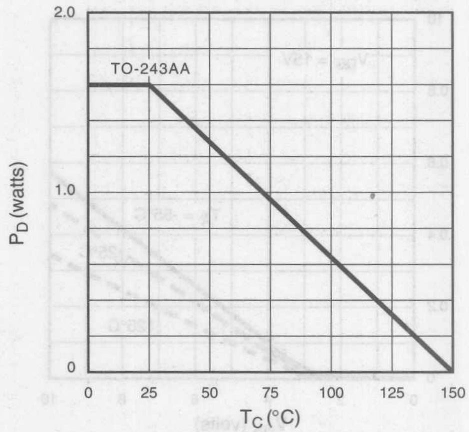
Saturation Characteristics



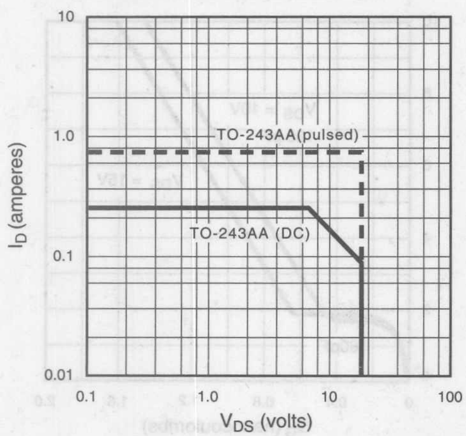
Transconductance vs. Drain Current



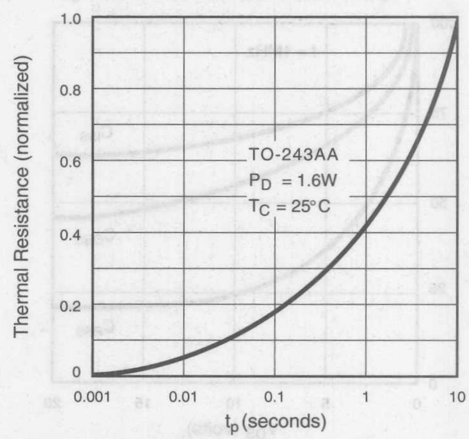
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

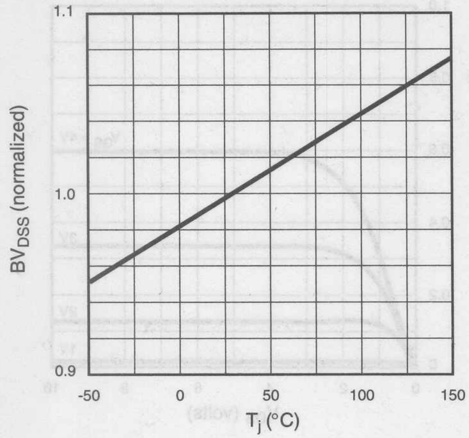


Thermal Response Characteristics

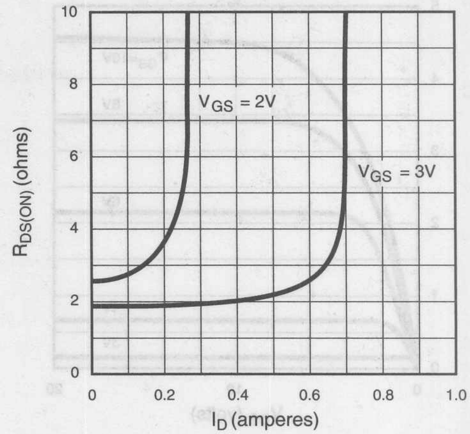


Typical Performance Curves

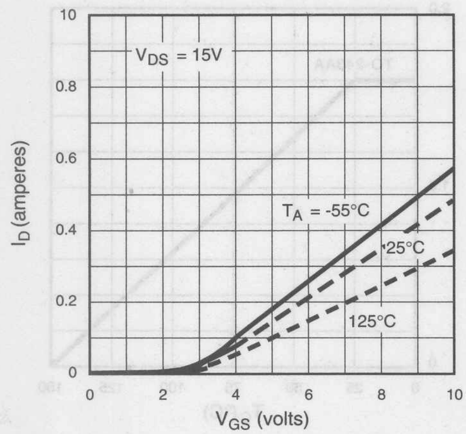
BV$_{DSS}$ Variation with Temperature



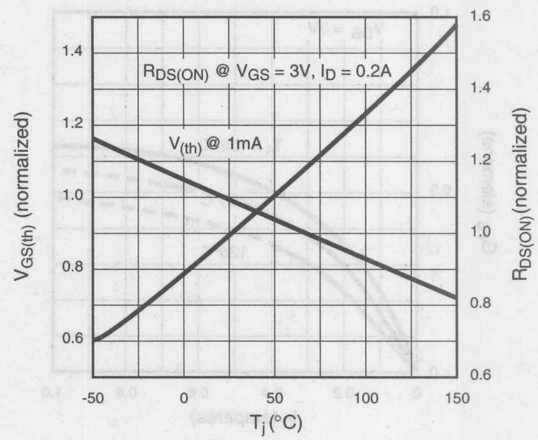
On-Resistance vs. I$_D$



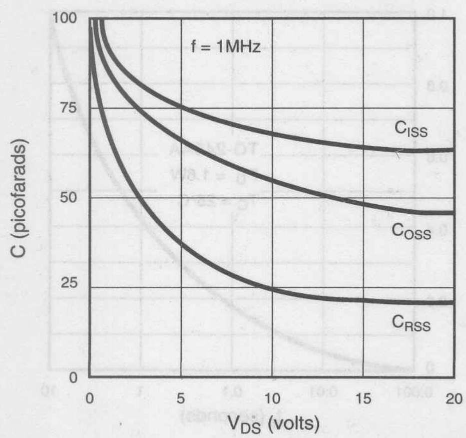
Transfer Characteristics



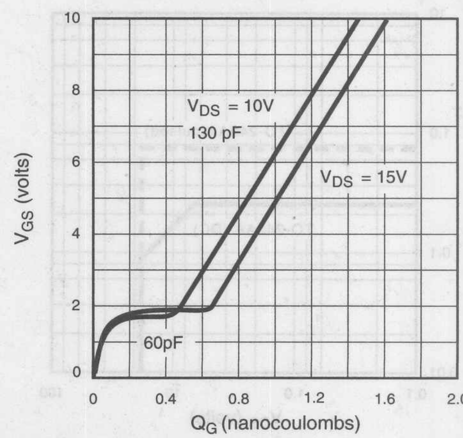
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92	DICE†
350V	5.0Ω	2.0V	2.0A	TN2635N3	TN2635ND
400V	5.0Ω	2.0V	2.0A	TN2640N3	TN2640ND

† MIL visual screening available.

Features

- ☐ Low threshold — 2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

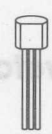
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	0.4A	2.0A	1.0W	170	125	0.4A	2.0A

* I_D (continuous) is limited by max rated T_j.

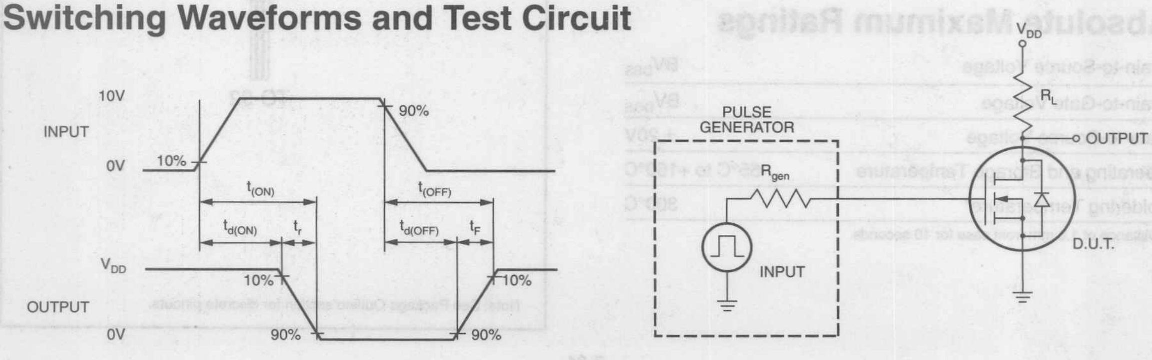
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2640	400			V	$V_{GS} = 0$, $I_D = 1mA$
		TN2635	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-2.5	-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		1.5	3.5		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			2.0	4.0			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.2	5.0	Ω	$V_{GS} = 5V$, $I_D = 150mA$
				3.0	5.0		$V_{GS} = 10V$, $I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		200	330		m℧	$V_{DS} = 25V$, $I_D = 100mA$
C_{ISS}	Input Capacitance			180	225	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			35	70		
C_{RSS}	Reverse Transfer Capacitance			7	25		
$t_{d(ON)}$	Turn-ON Delay Time			4	15	ns	$V_{DD} = 25V$, $I_D = 2A$, $R_{GEN} = 25\Omega$
t_r	Rise Time			15	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			20	25		
t_f	Fall Time			22	27		
V_{SD}	Diode Forward Voltage Drop				0.9	V	$V_{GS} = 0$, $I_{SD} = 200mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Supertex inc.

TP01L

Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92	TO-243AA*	DICE†
-20V	4.0Ω	-2.4V	-0.85A	TP0102N2	TP0102N3		TP0102ND
-40V	4.0Ω	-2.4V	-0.85A	TP0104N2	TP0104N3	TP0104N8	TP0104ND

* Same as SOT-89.
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Low threshold — 2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

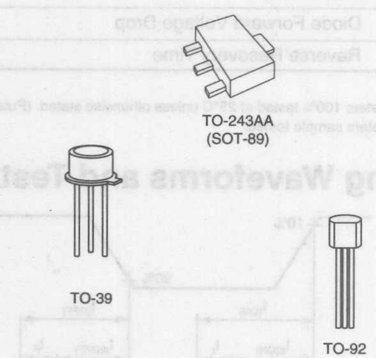
* For TO-39 and TO-92, distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for discrete pinouts.

7

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.9A	-2.0A	3.50W	35	125	-0.90A	-2.0A
TO-92	-0.5A	-2.0A	1.00W	125	170	-0.50A	-2.0A
TO-243AA	-1.0A	-2.0A	—	15	78†	-0.26A	-2.0A

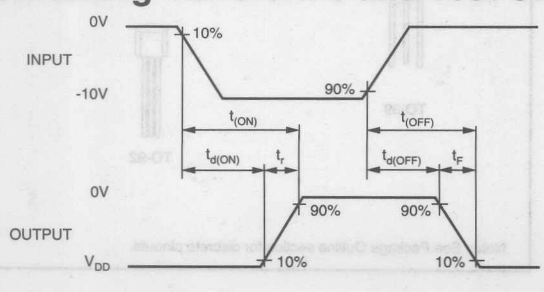
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

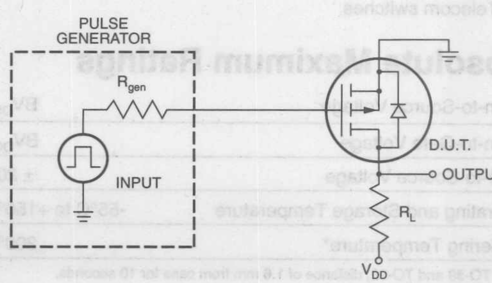
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0104	-40			V	$V_{GS} = 0$, $I_D = -1.0mA$
		TP0102	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.8	-6.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			-0.08		A	$V_{GS} = -3V$, $V_{DS} = -20V$
			-0.25	-0.50			$V_{GS} = -5V$, $V_{DS} = -20V$
			-0.85	-1.70			$V_{GS} = -10V$, $V_{DS} = -20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15		Ω	$V_{GS} = -3V$, $I_D = -25mA$
				4.7	7.5		$V_{GS} = -5V$, $I_D = -0.1A$
				2.5	4.0		$V_{GS} = -10V$, $I_D = -0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	$I_D = -0.5A$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		225	250		m℧	$V_{DS} = -20V$, $I_D = -0.5A$
C_{ISS}	Input Capacitance				60	pF	$V_{GS} = 0$, $V_{DS} = -20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance				50		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time			4.0	6.0	ns	$V_{DD} = -20V$, $I_D = -0.85A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			7.0	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3.0	9.0		
t_f	Fall Time			4.0	13		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	$I_{SD} = -0.25A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time			300		ns	$I_{SD} = -0.25A$, $V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

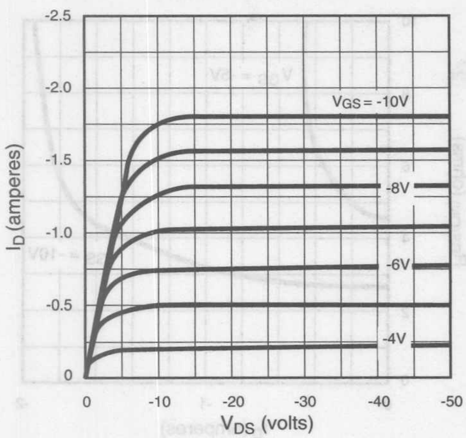
Switching Waveforms and Test Circuit



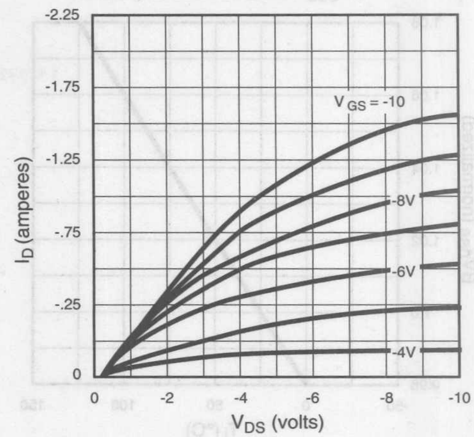


Typical Performance Curves

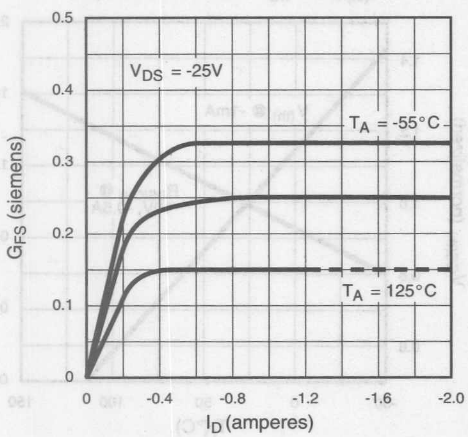
Output Characteristics



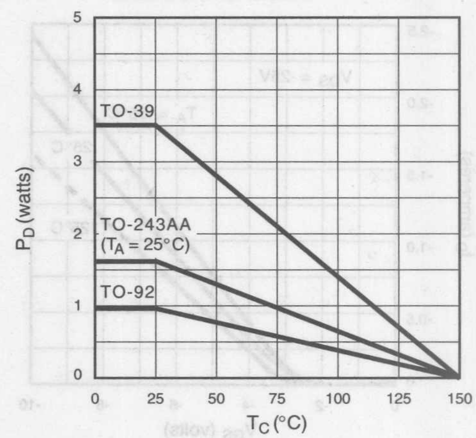
Saturation Characteristics



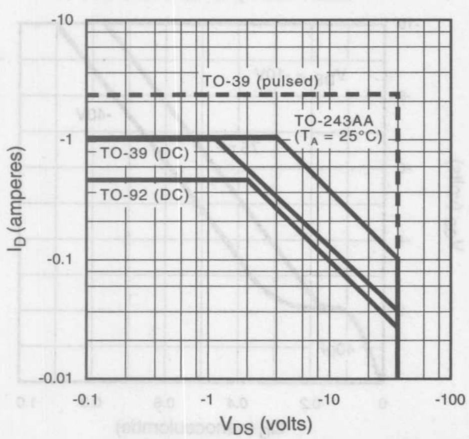
Transconductance vs. Drain Current



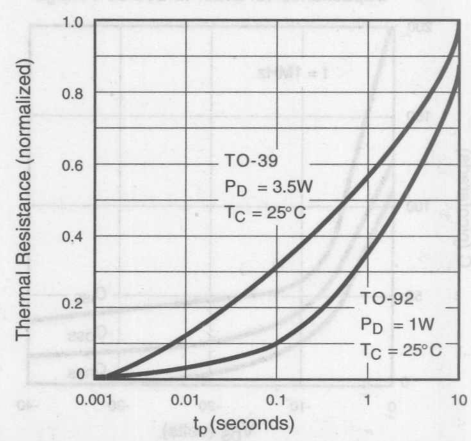
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

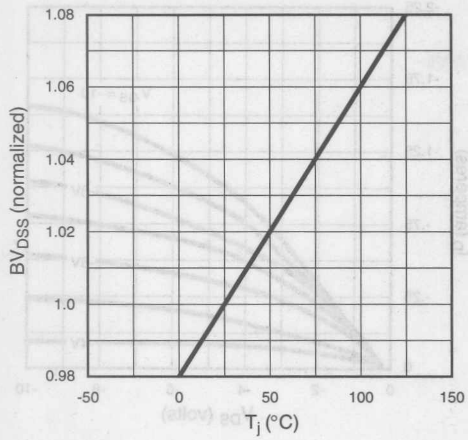


Thermal Response Characteristics

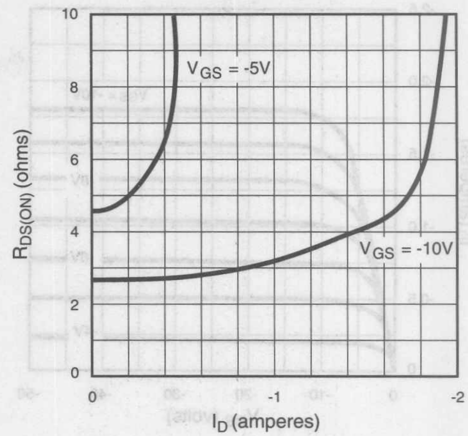


Typical Performance Curves

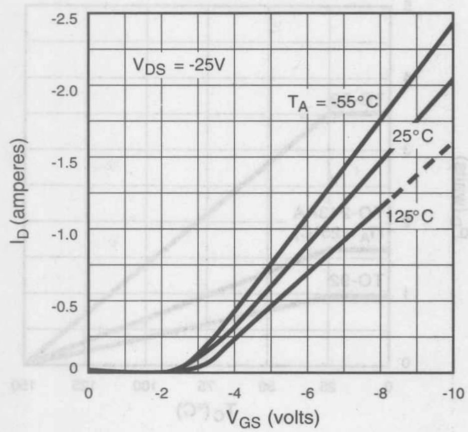
BV$_{DSS}$ Variation with Temperature



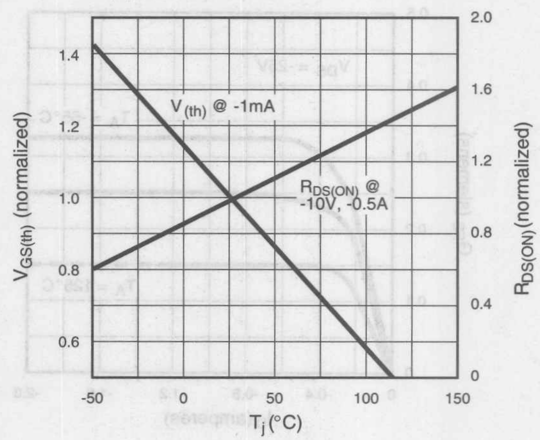
On-Resistance vs. Drain Current



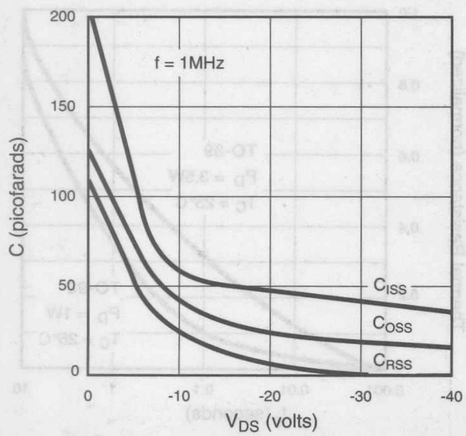
Transfer Characteristics



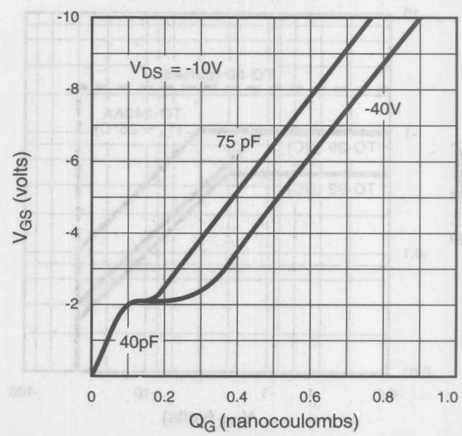
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

TP06A

Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
-60V	3.5Ω	-1.5A	-2.4V	TP0606N2	TP0606N3	TP0606N5	TP0606N6	TP0606N7	TP0606ND
-100V	3.5Ω	-1.5A	-2.4V	TP0610N2	TP0610N3	TP0610N5	—	—	TP0610ND

* 14 pin side brazed ceramic DIP
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold — -2.4V max
- High input impedance
- Low input capacitance — 80 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

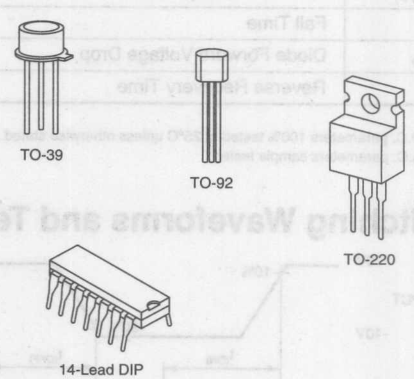
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-1.0A	-4.0A	6W	20	125	-0.8A	-4.0A
TO-92	-0.5A	-3.5A	1W	125	170	-0.4A	-3.5A
TO-220	-2.0A	-4.5A	45W	2.7	70	-2.0A	-4.5A
Plastic Dip	Refer to Arrays & Special Functions Section.						
Ceramic Dip							

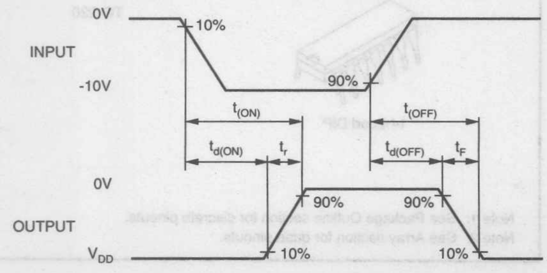
* I_D (continuous) is limited by max rated T_j.

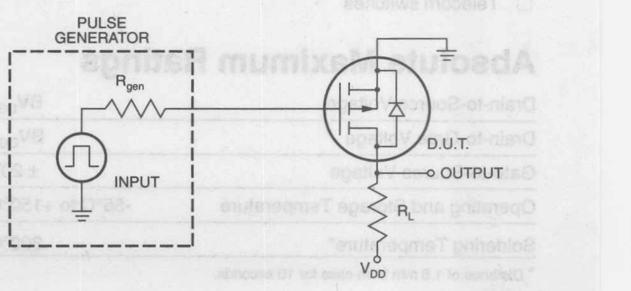
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0610	-100			V	$V_{GS} = 0$, $I_D = -2.0mA$
		TP0606	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.6		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-1.5	-2.5			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.0	7.0	Ω	$V_{GS} = -5V$, $I_D = -250mA$
				3.0	3.5		$V_{GS} = -10V$, $I_D = -0.75A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	$V_{GS} = -10V$, $I_D = -0.75A$
G_{FS}	Forward Transconductance		300	400		m℧	$V_{DS} = -25V$, $I_D = -0.75A$
C_{ISS}	Input Capacitance			80	150	pF	$V_{GS} = 0$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	85		
C_{RSS}	Reverse Transfer Capacitance			15	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$ $I_D = -1.0A$ $R_{GEN} = 25\Omega$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0$, $I_{SD} = -1.0A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = -1.0A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

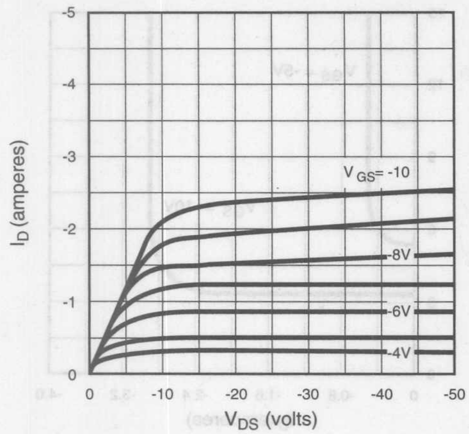
Switching Waveforms and Test Circuit



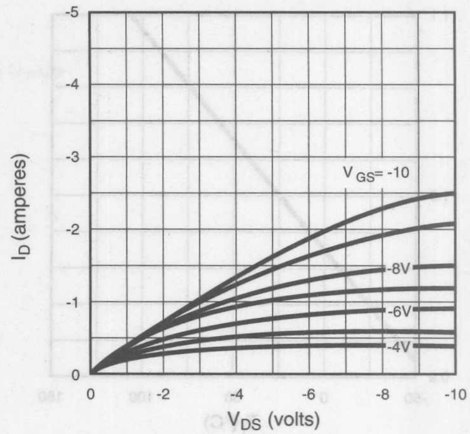


Typical Performance Curves

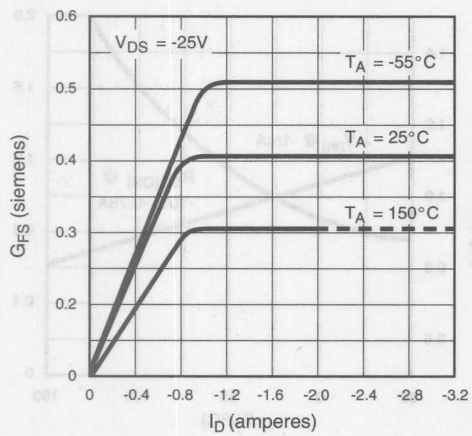
Output Characteristics



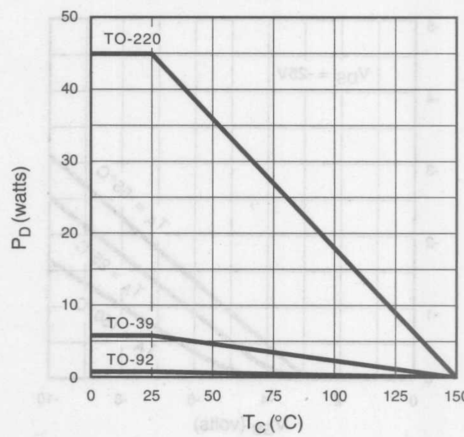
Saturation Characteristics



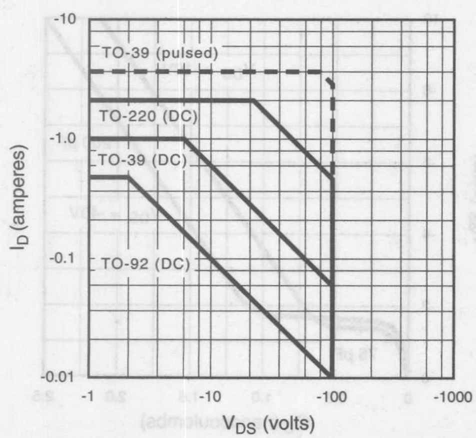
Transconductance vs. Drain Current



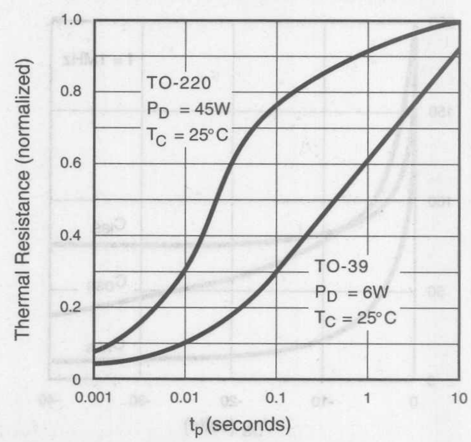
Power Dissipation vs. Case Temperature



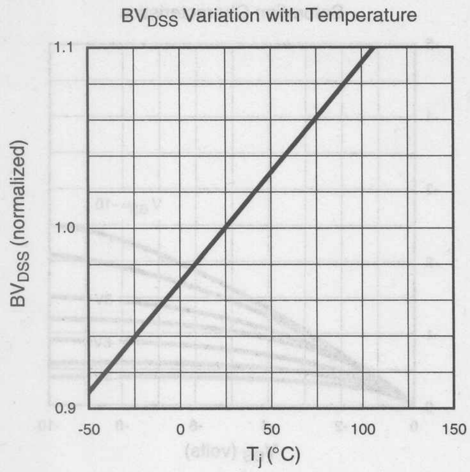
Maximum Rated Safe Operating Area

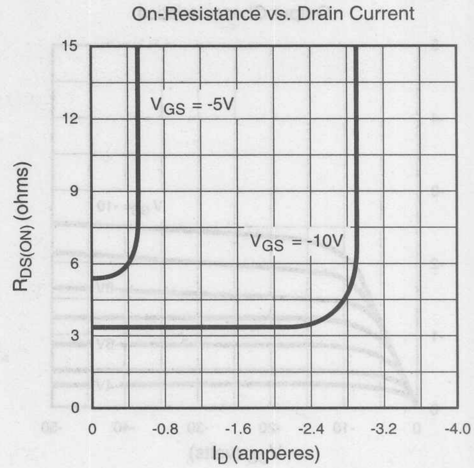


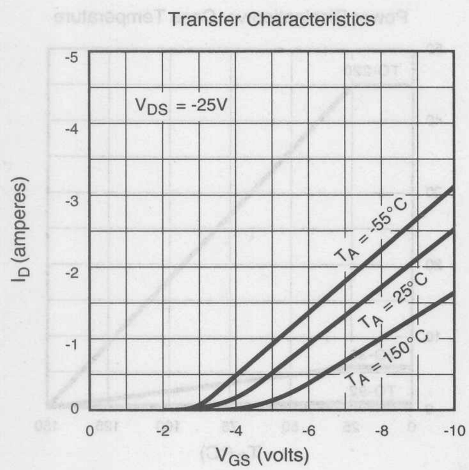
Thermal Response Characteristics

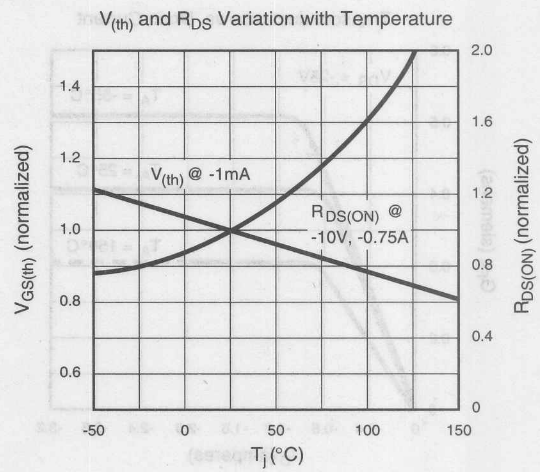


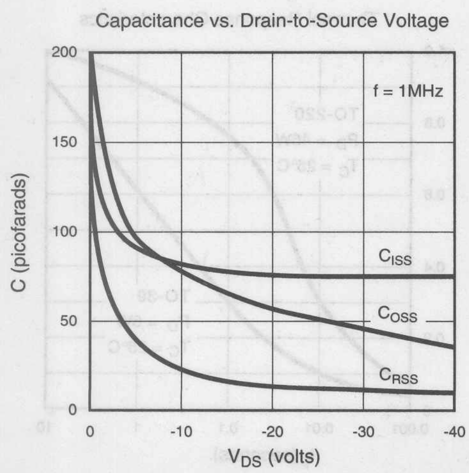
Typical Performance Curves

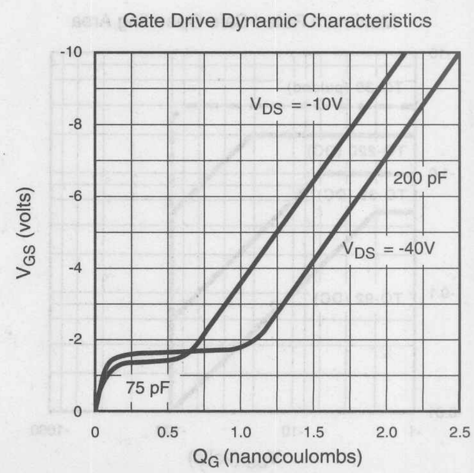












Supertex inc.

TP06C

Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package			
				TO-39	TO-92	TO-220	DICE†
-160V	12Ω	-0.75A	-2.4V	TP0616N2	TP0616N3	TP0616N5	TP0616ND
-200V	12Ω	-0.75A	-2.4V	TP0620N2	TP0620N3	TP0620N5	TP0620ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Low threshold — -2.4 V max
- ☐ High input impedance
- ☐ Low input capacitance — 85 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

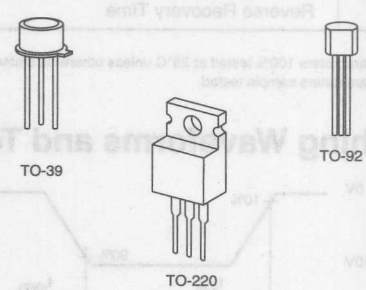
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.6A	-1.5A	6W	20	125	-0.6A	-1.5A
TO-92	-0.4A	-0.8A	1W	125	170	-0.4A	-0.8A
TO-220	-1.4A	-2.5A	45W	2.7	70	-1.4A	-2.5A

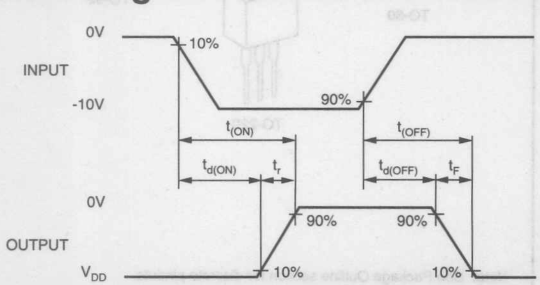
* I_D (continuous) is limited by max rated T_j.

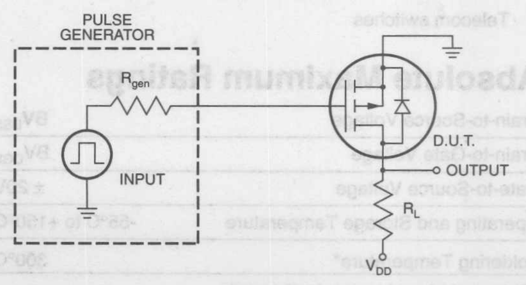
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0620	-200			V	$V_{GS} = 0$, $I_D = -2.0mA$
		TP0616	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.25			A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-0.75				$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			9.0	15	Ω	$V_{GS} = -5V$, $I_D = -0.1A$
				7.0	12		$V_{GS} = -10V$, $I_D = -0.2A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	$V_{GS} = -10V$, $I_D = -0.2A$
G_{FS}	Forward Transconductance		100	150		m℧	$V_{DS} = -25V$, $I_D = -0.4A$
C_{ISS}	Input Capacitance			85	150	pF	$V_{GS} = 0$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$ $I_D = -0.75A$ $R_{GEN} = 25\Omega$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				16		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0$, $I_{SD} = -0.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = -0.5A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

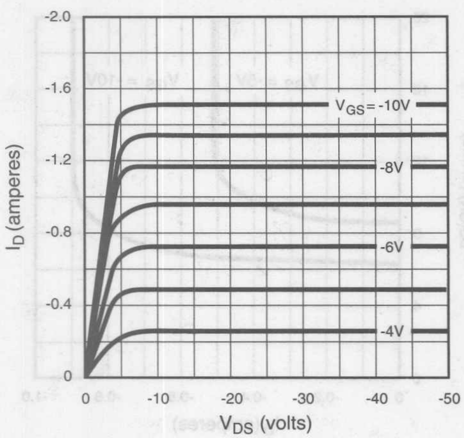
Switching Waveforms and Test Circuit



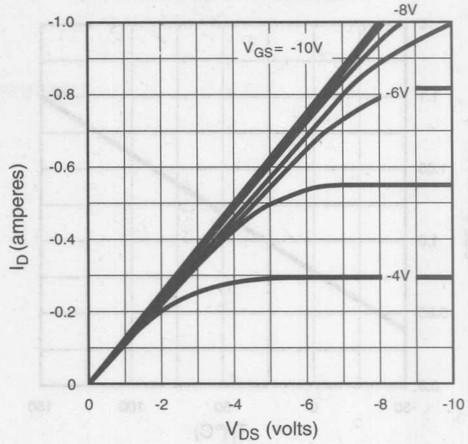


Typical Performance Curves

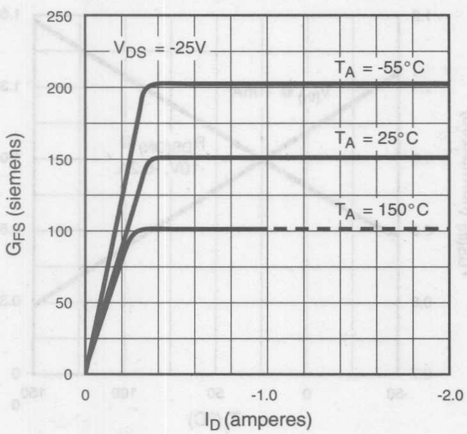
Output Characteristics



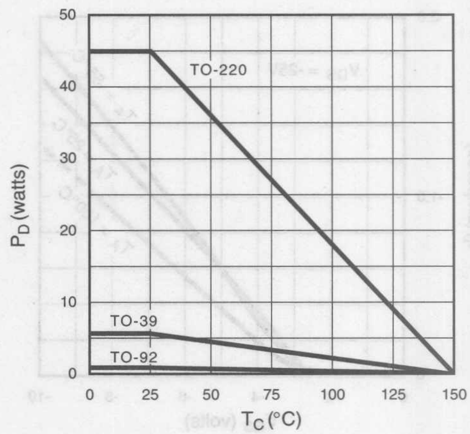
Saturation Characteristics



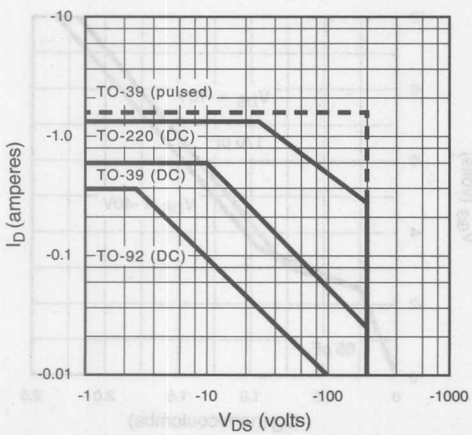
Transconductance vs. Drain Current



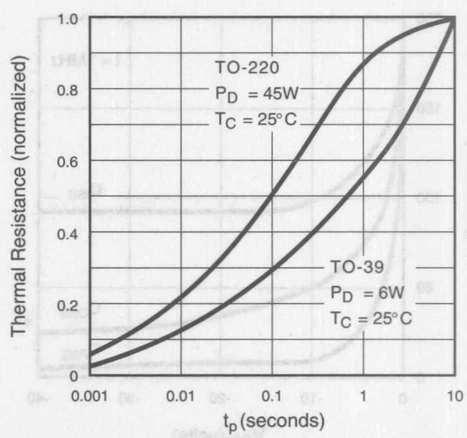
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

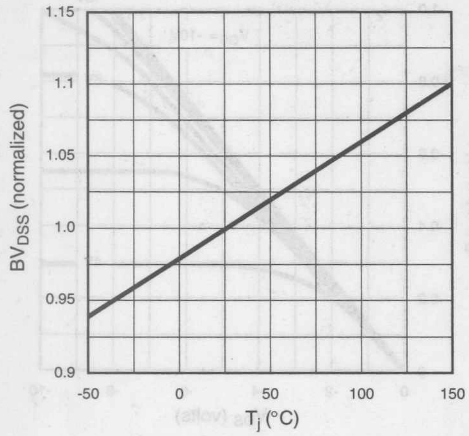


Thermal Response Characteristics

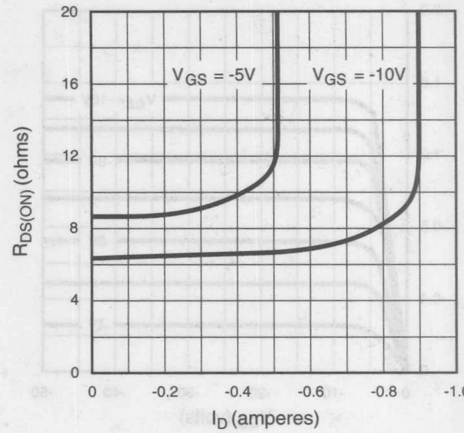


Typical Performance Curves

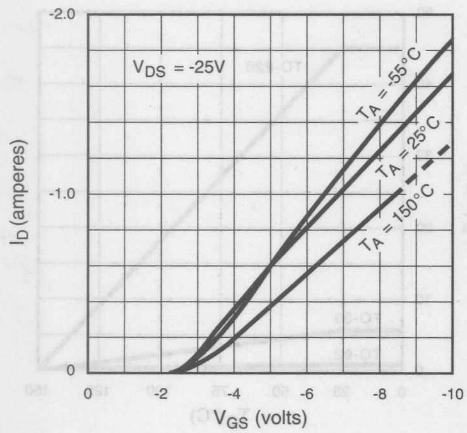
BV_{DSS} Variation with Temperature



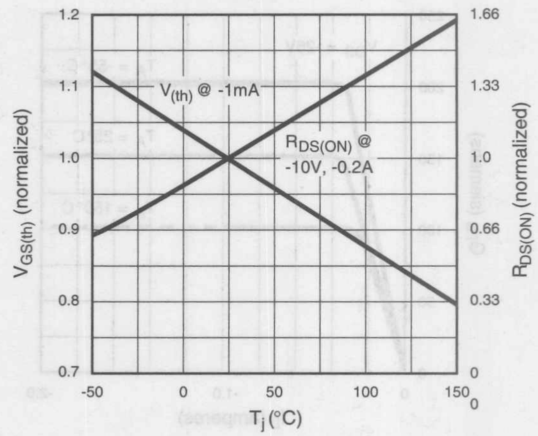
On-Resistance vs. Drain Current



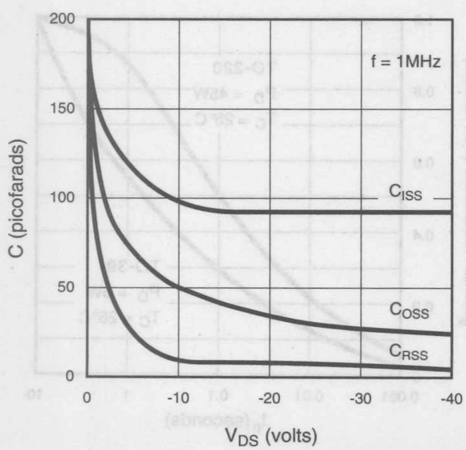
Transfer Characteristics



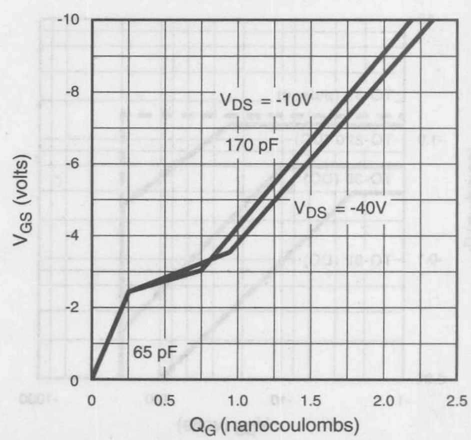
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package TO-39	TO-92	SOW-20*	DICE†
-20V	2.0Ω	-2.0A	-2.4V	TP0602N2	TP0602N3	—	TP0602ND
-40V	2.0Ω	-2.0A	-2.4V	TP0604N2	TP0604N3	TP0604WG	TP0604ND

* Same as SO-20 with 300 mil wide body.
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Low threshold — -2.4V max.
- High input impedance
- Low input capacitance — 95 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

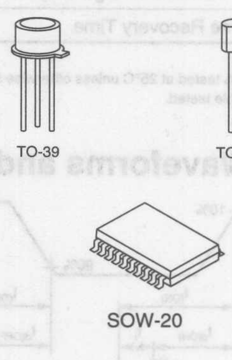
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-2.0A	-4.8A	6W	20	125	-2.0A	-4.8A
TO-92	-0.75A	-4.2A	1W	125	170	-0.75A	-4.2A
SOW-20	Refer to Arrays & Special Functions Section						

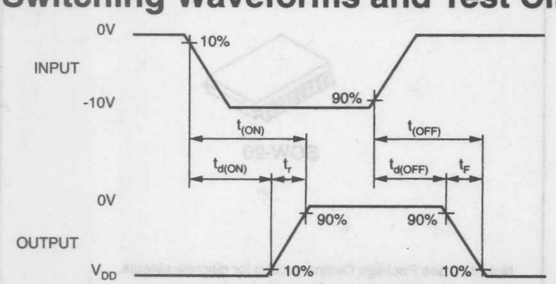
* I_D (continuous) is limited by max rated T_j.

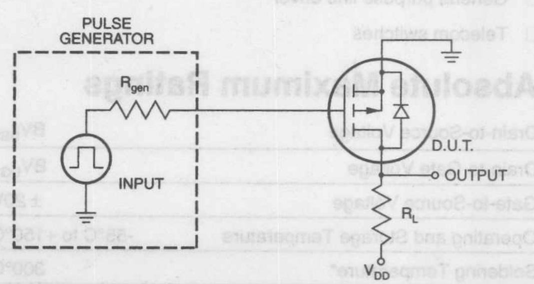
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0604	-40			V	$V_{GS} = 0$, $I_D = -2.0mA$
		TP0602	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.6		A	$V_{GS} = -5V$, $V_{DS} = -20V$
			-2.0	-3.3			$V_{GS} = -10V$, $V_{DS} = -20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	3.5	Ω	$V_{GS} = -5V$, $I_D = -250mA$
				1.5	2.0		$V_{GS} = -10V$, $I_D = -1.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	1.2	%/°C	$V_{GS} = -10V$, $I_D = -1.0A$
G_{FS}	Forward Transconductance		0.4	0.6		℧	$V_{DS} = -20V$, $I_D = -1.0A$
C_{ISS}	Input Capacitance			95	150	pF	$V_{GS} = 0$, $V_{DS} = -20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			85	120		
C_{RSS}	Reverse Transfer Capacitance			35	60		
$t_{d(ON)}$	Turn-ON Delay Time			5.0	8	ns	$V_{DD} = -20V$ $I_D = -1.0A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			7.0	18		
$t_{d(OFF)}$	Turn-OFF Delay Time			10	15		
t_f	Fall Time			6.0	19		
V_{SD}	Diode Forward Voltage Drop			-1.3	-2.0	V	$V_{GS} = 0$, $I_{SD} = -1.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = -1.5A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

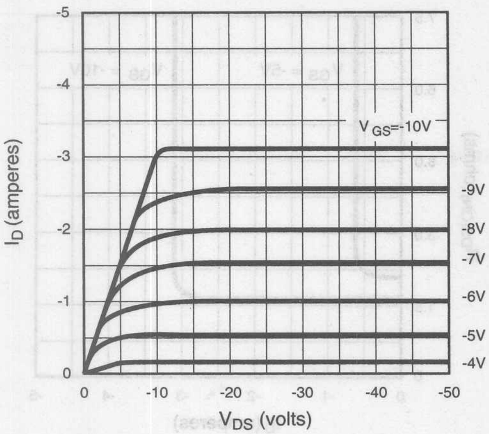
Switching Waveforms and Test Circuit



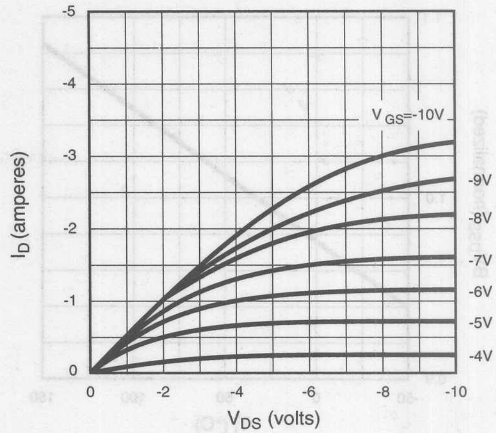


Typical Performance Curves

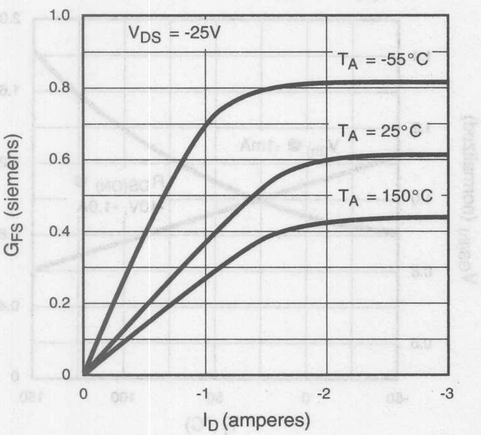
Output Characteristics



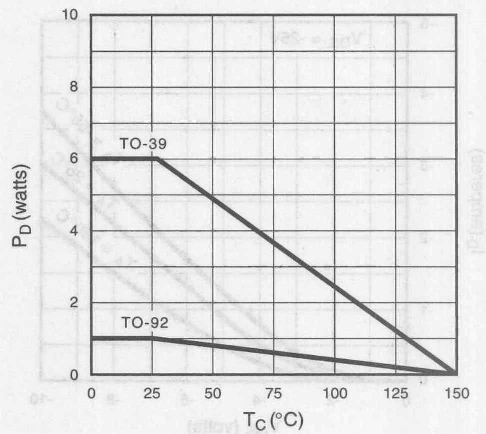
Saturation Characteristics



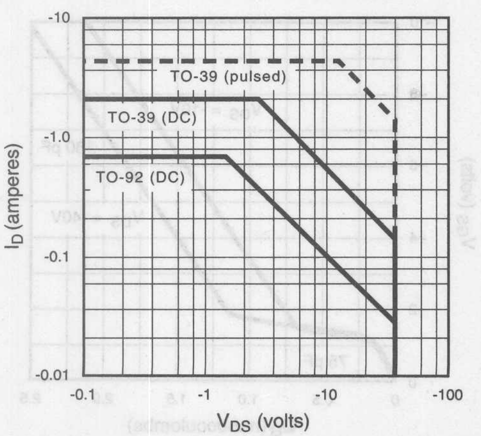
Transconductance vs. Drain Current



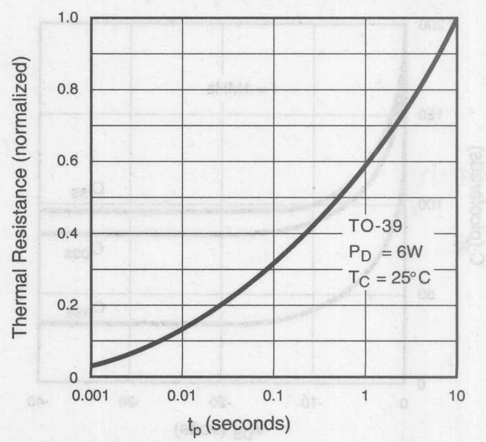
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



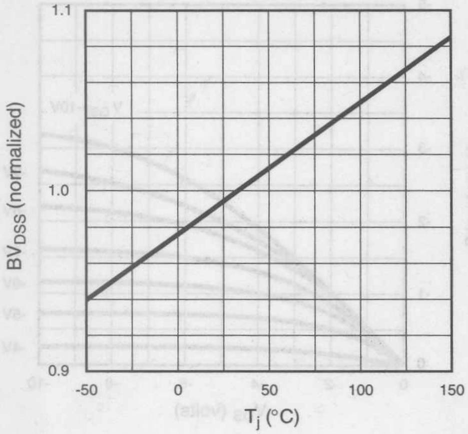
Thermal Response Characteristics



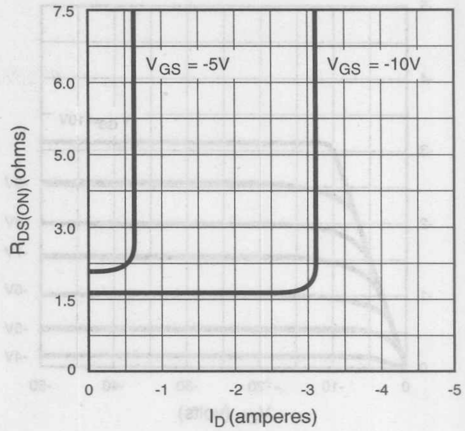
7

Typical Performance Curves

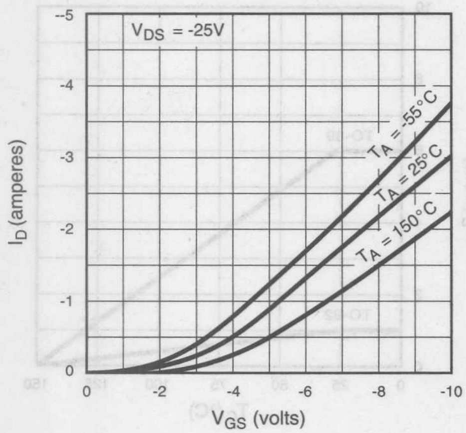
BV$_{DSS}$ Variation with Temperature



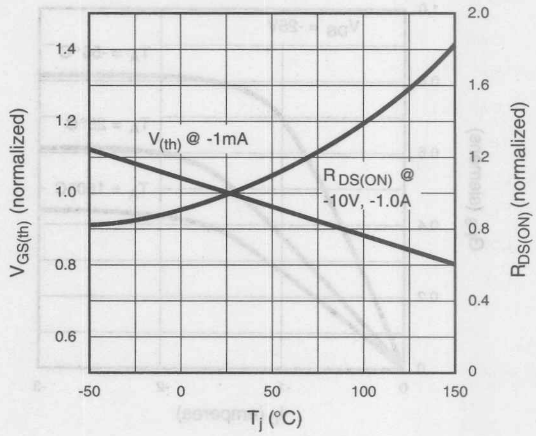
On-Resistance vs. Drain Current



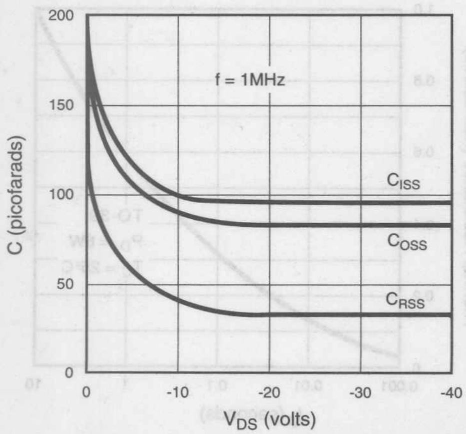
Transfer Characteristics



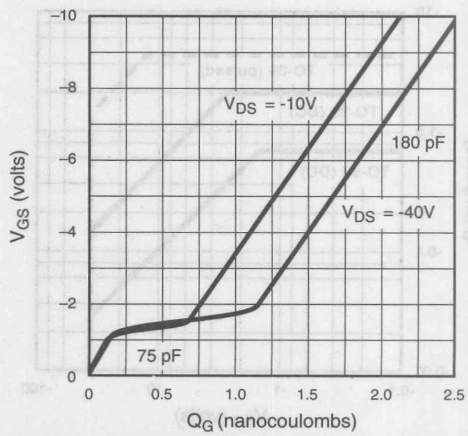
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-60V	3.5Ω	-2.4V	-1.5A	—	TP2506ND
-100V	3.5Ω	-2.4V	-1.5A	TP2510N8	TP2510ND

* Same as SOT-89.
† MIL visual screening available.

Features

- Low threshold — -2.4V max.
- High input impedance
- Low input capacitance — 125 pF max
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

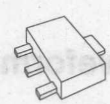
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-1.0A	-2.5A	1.6W†	15	78†	-1.0A	-2.5A

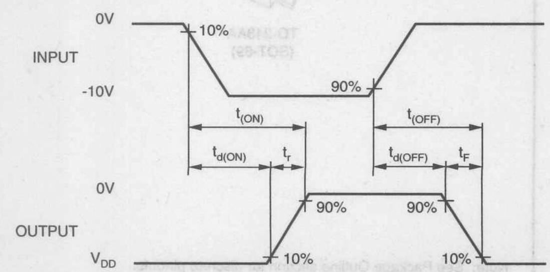
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

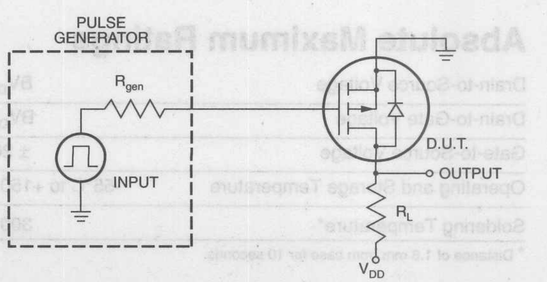
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2510	-100			V	$V_{GS} = 0$, $I_D = -2mA$
		TP2506	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.6		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-1.5	-2.5			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.0	7.0	Ω	$V_{GS} = -5V$, $I_D = -250mA$
				2.0	3.5		$V_{GS} = -10V$, $I_D = -0.75A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	$V_{GS} = -10V$, $I_D = -0.75A$
G_{FS}	Forward Transconductance		300	360		m℧	$V_{DS} = -25V$, $I_D = -0.75A$
C_{ISS}	Input Capacitance			80	125	pF	$V_{GS} = 0$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			40	70		
C_{RSS}	Reverse Transfer Capacitance			10	25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$, $I_D = -1.0A$, $R_{GEN} = 25Ω$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0$, $I_{SD} = -1.0A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = -1.0A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

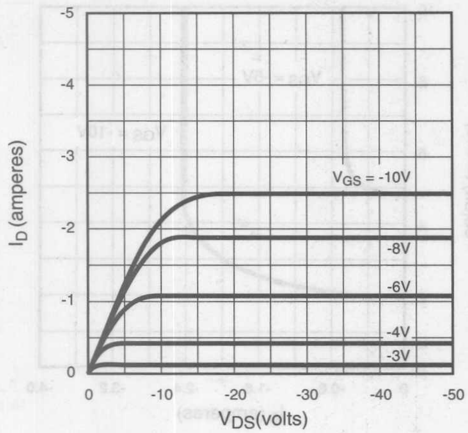
Switching Waveforms and Test Circuit



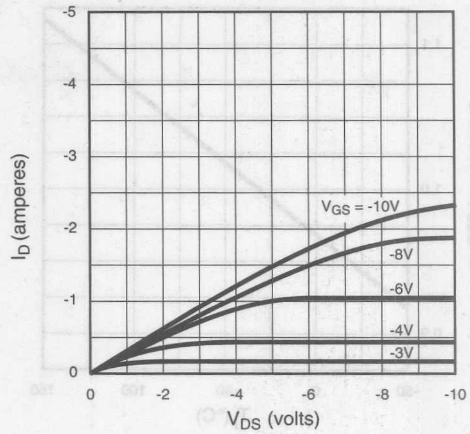


Typical Performance Curves

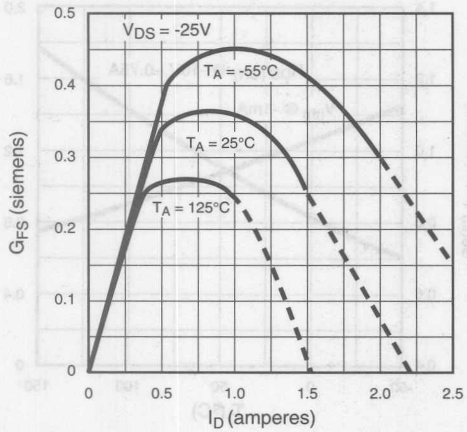
Output Characteristics



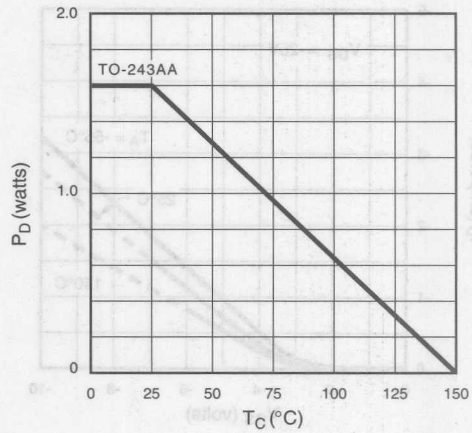
Saturation Characteristics



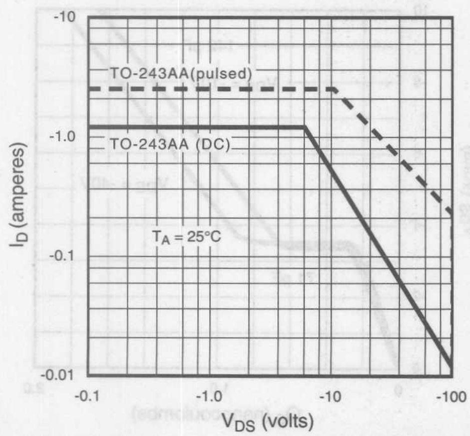
Transconductance vs. Drain Current



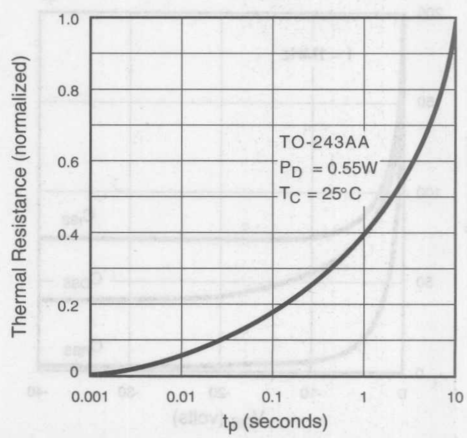
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

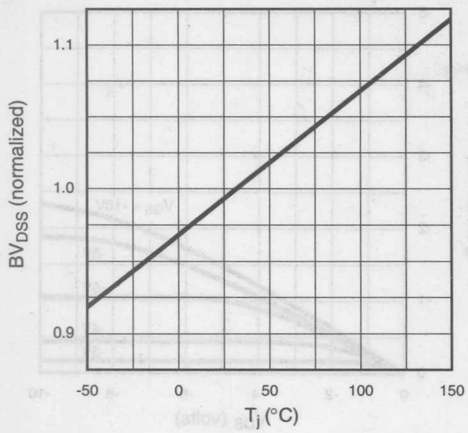


Thermal Response Characteristics

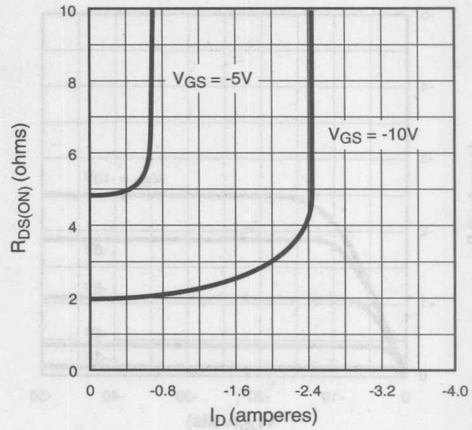


Typical Performance Curves

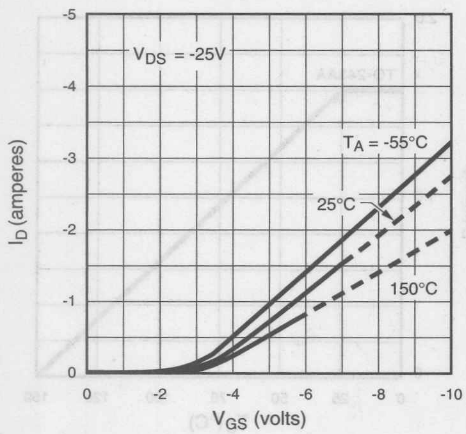
BV$_{DSS}$ Variation with Temperature



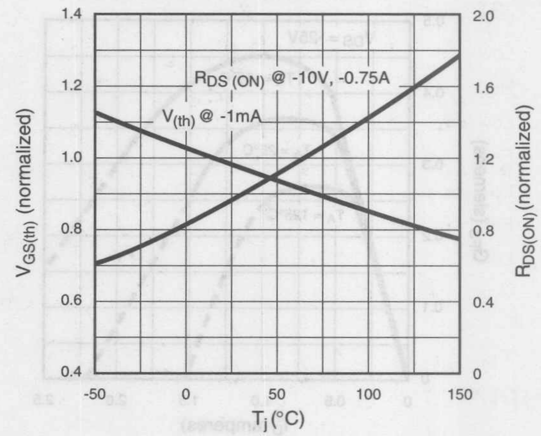
On-Resistance vs. Drain Current



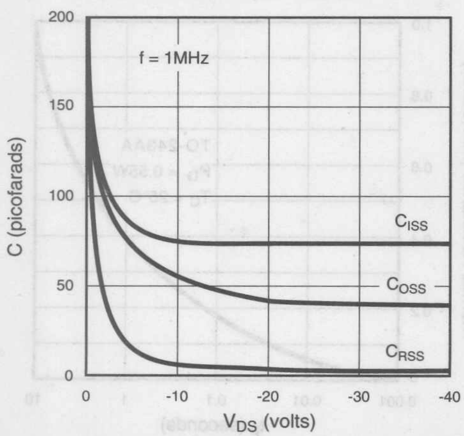
Transfer Characteristics



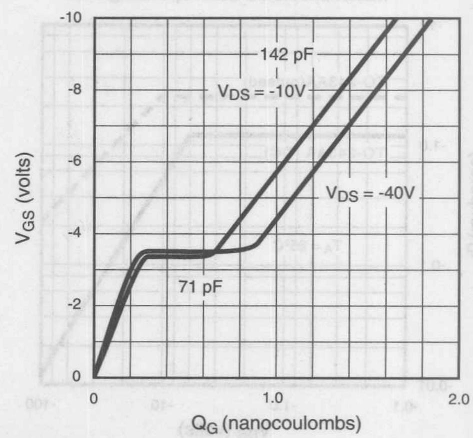
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-160V	12Ω	-2.4V	-0.75A	—	TP2516ND
-200V	12Ω	-2.4V	-0.75A	TP2520N8	TP2520ND

* Same as SOT-89.
† MIL visual screening available.

7

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Low Threshold DMOS Technology

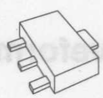
These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-0.57	-2.0	1.6W	15	78†	-0.57A	-2.0A

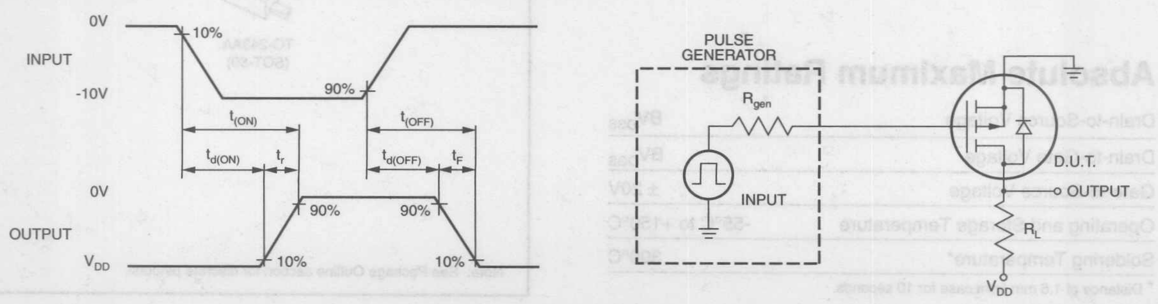
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2520	-200			V	$V_{GS} = 0$, $I_D = -2mA$
		TP2516	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.25	-0.7		A	$V_{GS} = -4.5V$, $V_{DS} = -25V$
			-0.75	-2.1			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10	15	Ω	$V_{GS} = -4.5V$, $I_D = -100mA$
				8.0	12		$V_{GS} = -10V$, $I_D = -200mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	$V_{GS} = -10V$, $I_D = -200mA$
G_{FS}	Forward Transconductance		100	250		m℧	$V_{DS} = -25V$, $I_D = -200mA$
C_{ISS}	Input Capacitance			75	125	pF	$V_{GS} = 0$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	85		
C_{RSS}	Reverse Transfer Capacitance			10	35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$, $I_D = -0.75A$, $R_{GEN} = 25\Omega$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0$, $I_{SD} = -0.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = -0.5A$

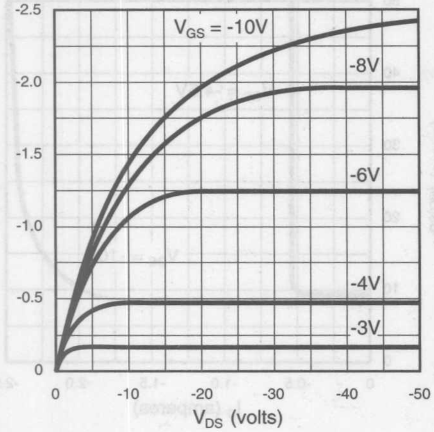
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

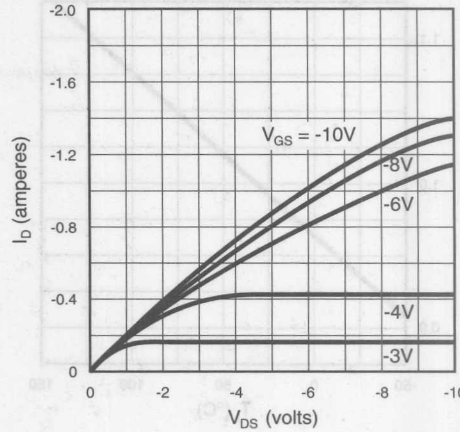


Typical Performance Curves

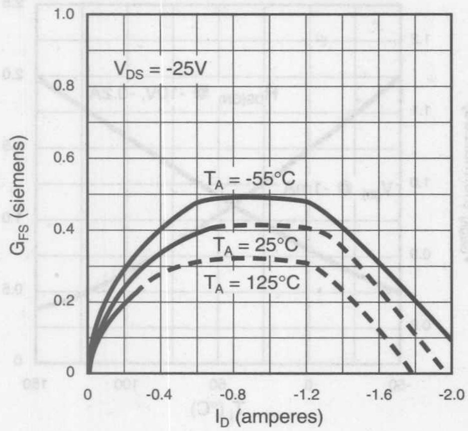
Output Characteristics



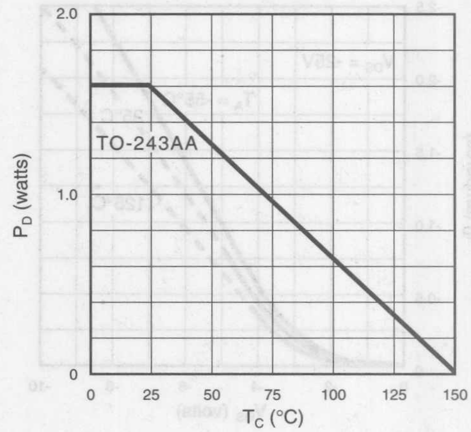
Saturation Characteristics



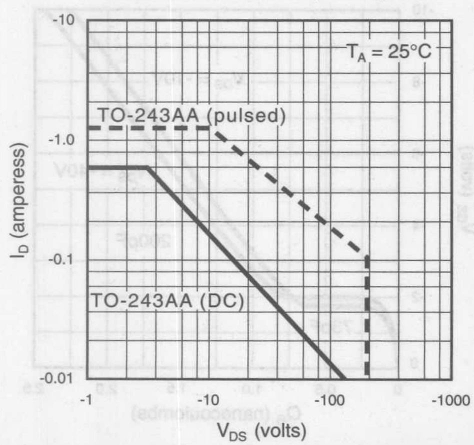
Transconductance vs. Drain Current



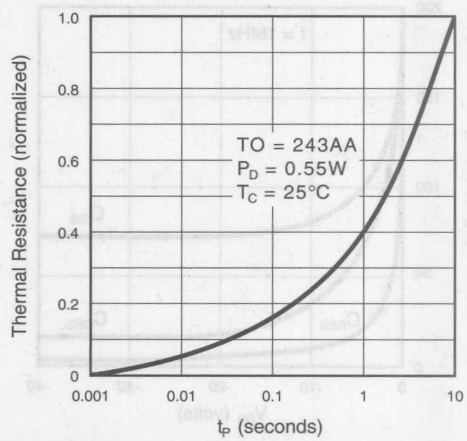
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

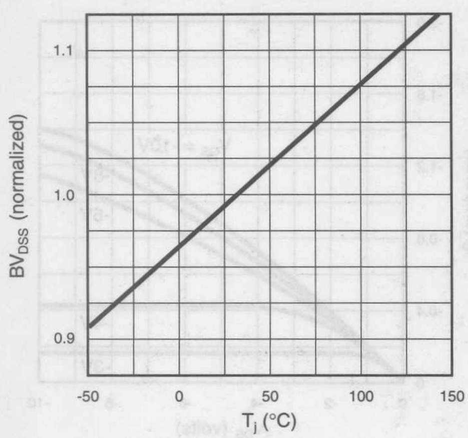


Thermal Response Characteristics

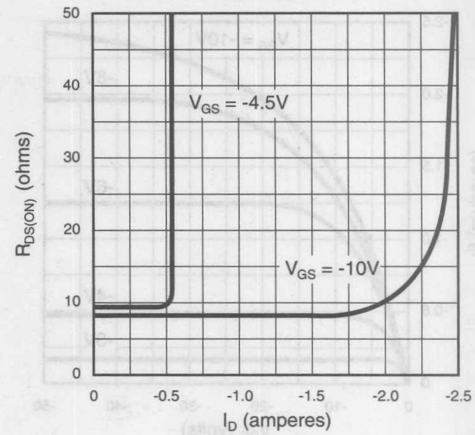


Typical Performance Curves

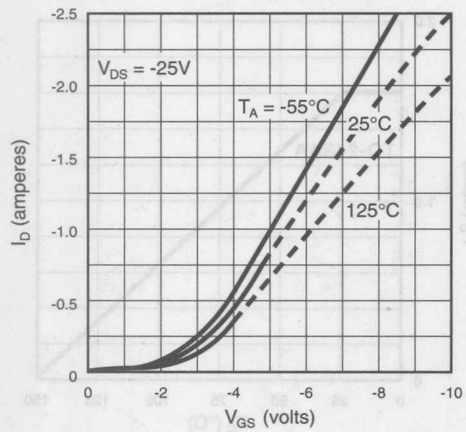
BV$_{DSS}$ Variation with Temperature



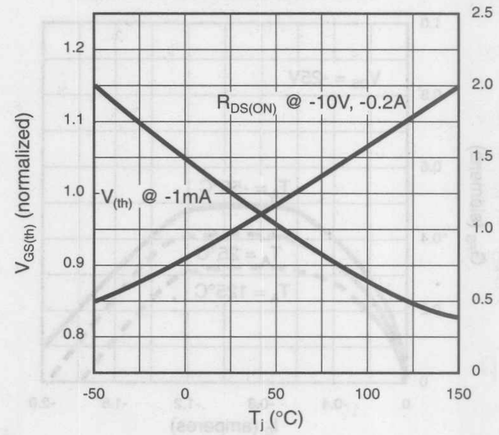
On-Resistance vs. Drain Current



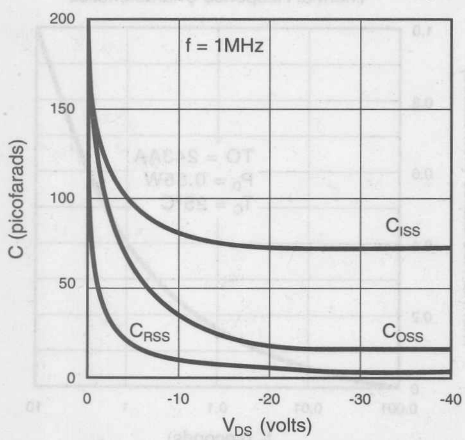
Transfer Characteristics



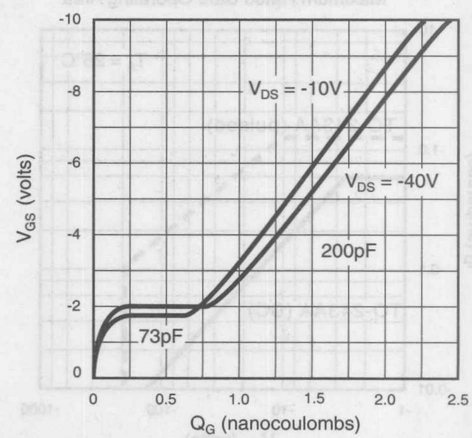
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92	TO-243AA*	DICE†
-350V	25Ω	-2.4V	-0.4A	TP2535N3	—	TP2535ND
-400V	25Ω	-2.4V	-0.4A	TP2540N3	TP2540N8	TP2540ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

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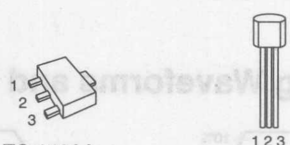
Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA (SOT-89)

TO-92

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.3A	-0.6A	1W	125	170	-0.3A	-0.6A
TO-243AA	-0.4A	-1.2A	—	15	78†	-0.4A	-1.2A

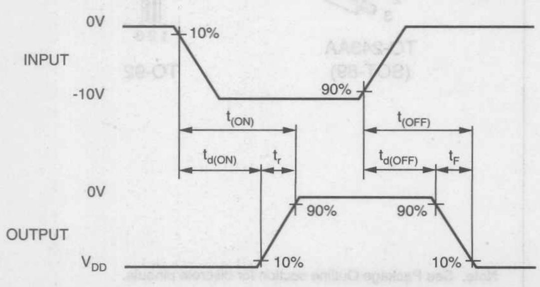
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Signficant P_D increase possible on ceramic substrate.

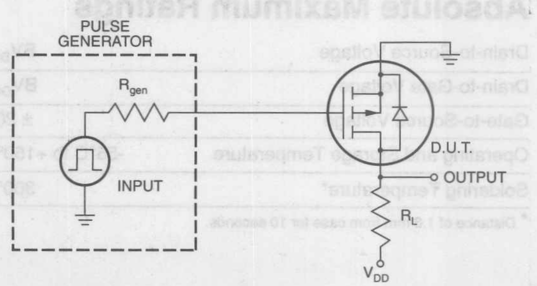
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2540	-400			V	$V_{GS} = 0$, $I_D = -2mA$
		TP2535	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				4.8	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.2	-0.3		A	$V_{GS} = -4.5V$, $V_{DS} = -25V$
			-0.4	-1.1			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	30	Ω	$V_{GS} = -4.5V$, $I_D = -100mA$
				19	25		$V_{GS} = -10V$, $I_D = -100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = -10V$, $I_D = -100mA$
G_{FS}	Forward Transconductance		100	175		m℧	$V_{DS} = -25V$, $I_D = -100mA$
C_{ISS}	Input Capacitance			60	125	pF	$V_{GS} = 0$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	70		
C_{RSS}	Reverse Transfer Capacitance			10	25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$ $I_D = -100mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0$, $I_{SD} = -100mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0$, $I_{SD} = -100mA$

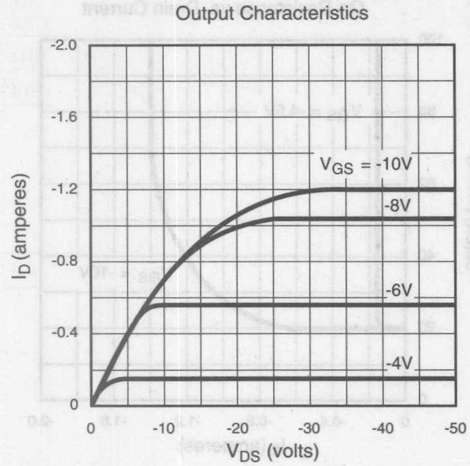
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

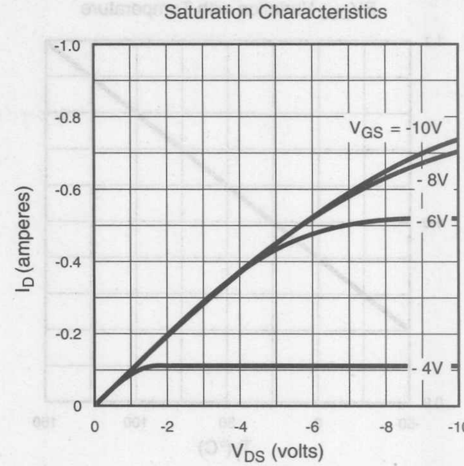
Switching Waveforms and Test Circuit





Typical Performance Curves





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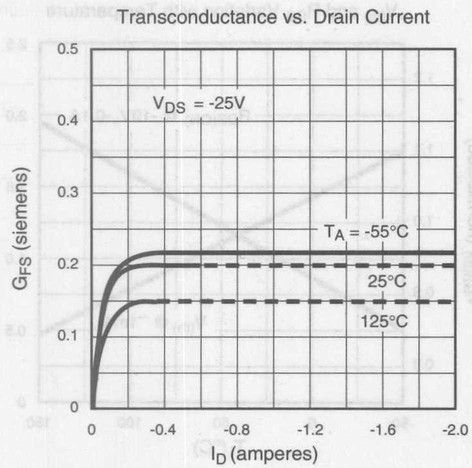
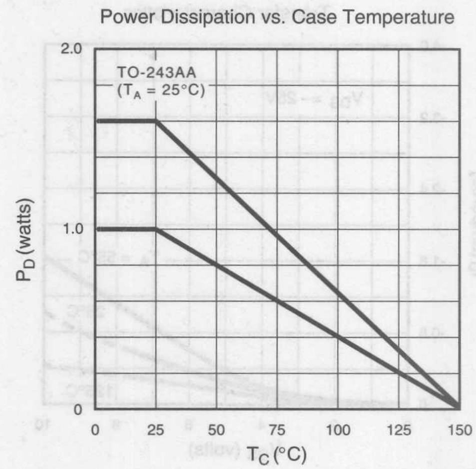
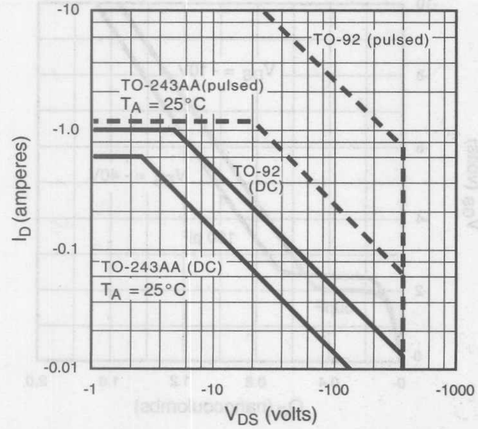
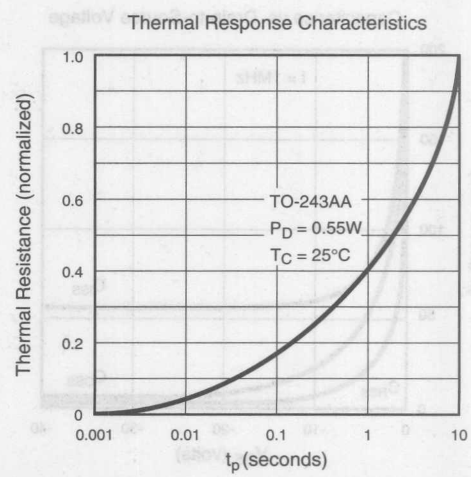


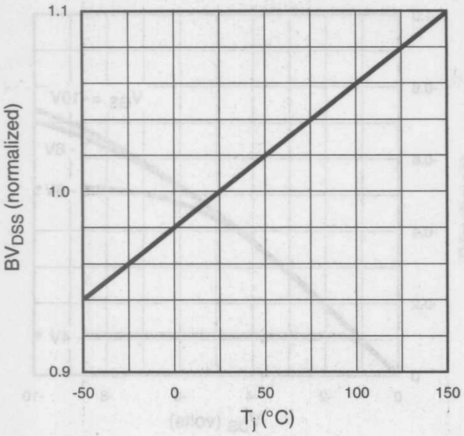




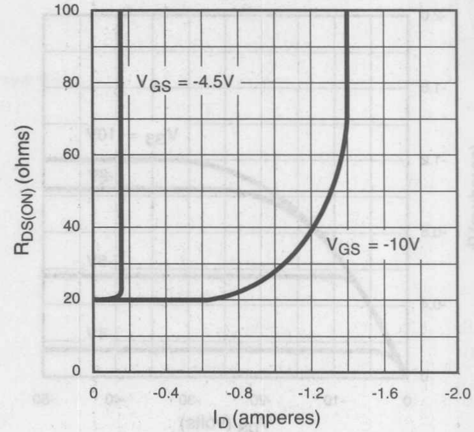


Typical Performance Curves

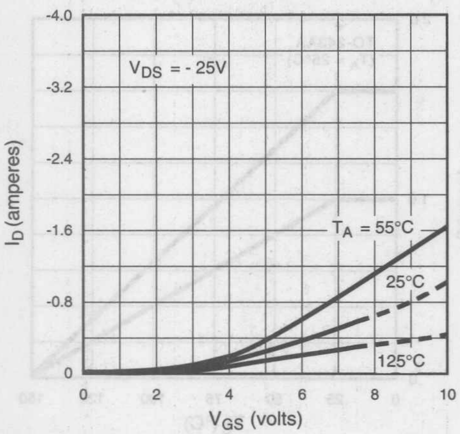
BV$_{DSS}$ Variation with Temperature



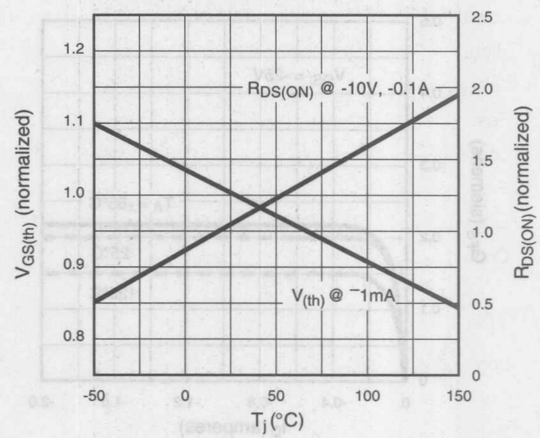
On-Resistance vs. Drain Current



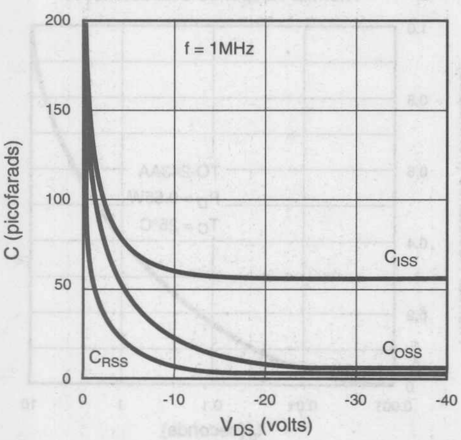
Transfer Characteristics



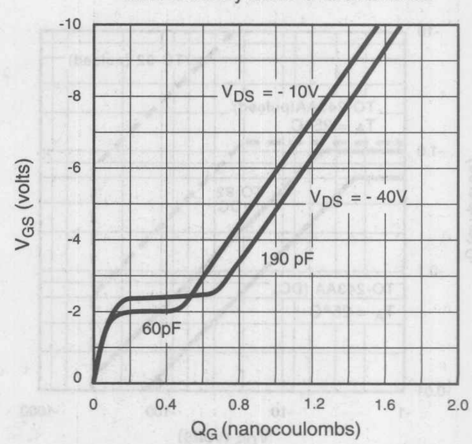
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

TP25L

Low Threshold

Preliminary

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-20V	2.0Ω	-2.4V	-2.0A	TP2502N8	TP2502ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

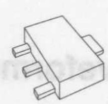
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-1.2A	-3.3A	1.6W†	15	78†	-1.2A	-3.3A

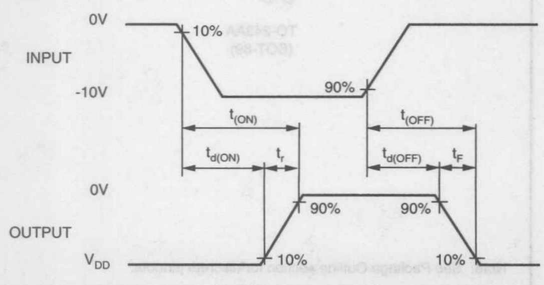
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

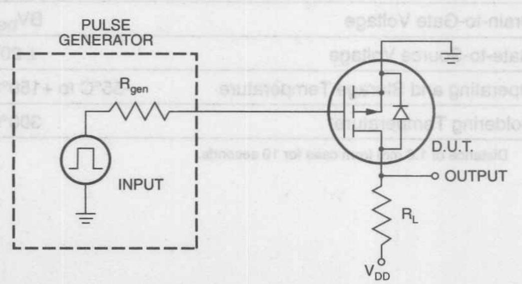
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-20			V	$V_{GS} = 0$, $I_D = -2mA$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		3.0	4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			-10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
				-1.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	-0.4	-0.7		A	$V_{GS} = -5V$, $V_{DS} = -15V$
		-2.0	-3.3			$V_{GS} = -10V$, $V_{DS} = -15V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.0	3.5	Ω	$V_{GS} = -5V$, $I_D = -250mA$
			1.5	2.0		$V_{GS} = -10V$, $I_D = -1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.75	1.2	%/°C	$V_{GS} = -10V$, $I_D = -1A$
G_{FS}	Forward Transconductance	0.3	0.65		℧	$V_{DS} = -15V$, $I_D = -1A$
C_{ISS}	Input Capacitance			125	pF	$V_{GS} = 0$, $V_{DS} = -20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			70		
C_{RSS}	Reverse Transfer Capacitance			25		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -20V$, $I_D = -1.0A$, $R_{GEN} = 25\Omega$
t_r	Rise Time			11		
$t_{d(OFF)}$	Turn-OFF Delay Time			15		
t_f	Fall Time			12		
V_{SD}	Diode Forward Voltage Drop		-1.3	-2.0	V	$V_{GS} = 0$, $I_{SD} = -1.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0$, $I_{SD} = -1.5A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Chapter 8 – DMOS N-Channel Discretes

Supertex inc. 2N6659

N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39
35V	1.8Ω	1.5A	2N6659

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

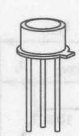
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39

Note 1: See Package Outline section for discrete pinouts.

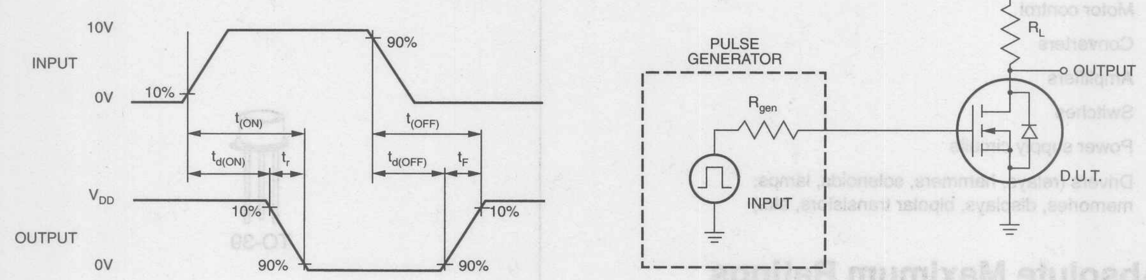
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	35			V	$I_D = 10\mu A$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10		$V_{GS} = 0$, V_{DS} = Max Rating
				500	µA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1.5			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
				1.8		$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance	170			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			50		
C_{OSS}	Common Source Output Capacitance			40	pF	$V_{GS} = 0$, $V_{DS} = 24V$ f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 25V$, $I_D = 1A$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		1.2	1.8	V	$I_{SD} = 1.4A$, $V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Supertex inc.

2N6660
2N6661

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39
60V	3.0Ω	1.5A	2N6660
90V	4.0Ω	1.5A	2N6661

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

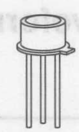
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
2N6660	1.1A	3A	6.25W	20	125	1.1A	3.0A
2N6661	0.9A	3A	6.25W	20	125	0.9A	3.0A

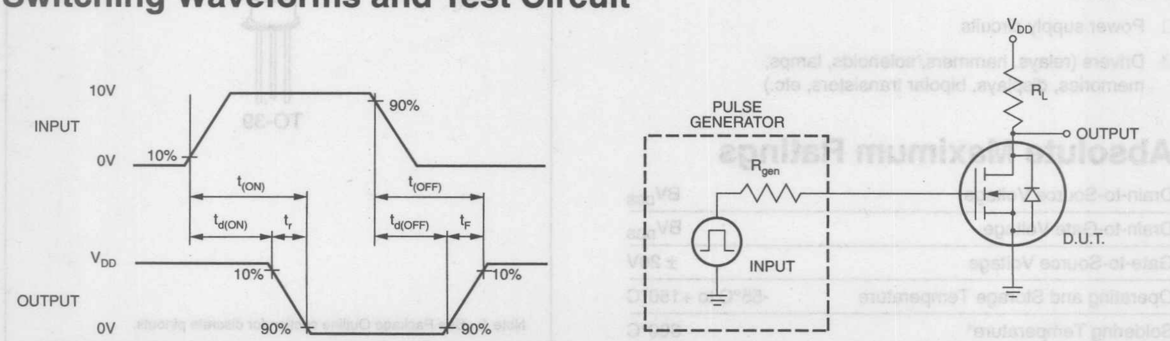
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	2N6660	60			V	$V_{GS} = 0$, $I_D = 10\mu A$
		2N6661	90				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	$V_{GS} = 0$, V_{DS} = Max Rating
					500		$V_{GS} = 0$, V_{DS} = 0.8 Max Rating, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		1.5			A	$V_{GS} = 10$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	All			5.0	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6660			3.0		$V_{GS} = 10V$, $I_D = 1A$
		2N6661			4.0		$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance		170			m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance				50	pF	$V_{GS} = 0$, $V_{DS} = 24V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance				40		
C_{RSS}	Reverse Transfer Capacitance				10		
$t_{(ON)}$	Turn-ON Time				10	ns	$V_{DD} = 25V$, $I_D = 1A$, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time				10		
V_{SD}	Diode Forward Voltage Drop			1.2		V	$V_{GS} = 0$, $I_{SD} = 1A$
t_{rr}	Reverse Recovery Time			350		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Supertex inc.

2N7000

N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92
60V	5Ω	75mA	2N7000

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

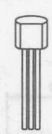
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note 1: See Package Outline section for discrete pinouts.

8

TO-92	200mA	500mA	400mW	312.5	40

* I_D (continuous) is limited by max rated T_j.

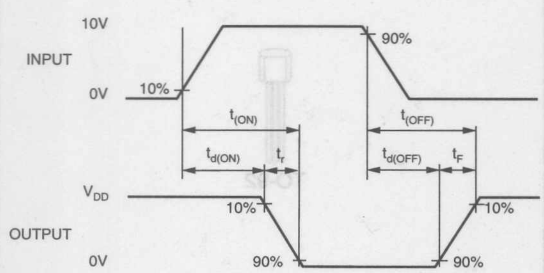
Electrical Characteristics (@ 25°C unless otherwise specified)

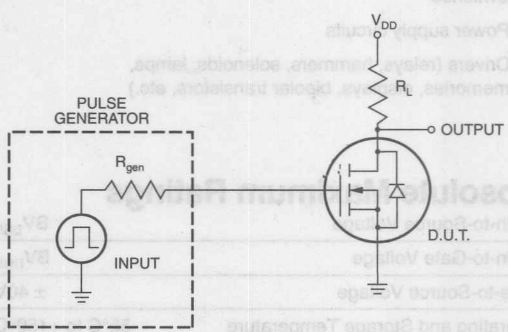
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$I_D = 10\mu A$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		3.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			10	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			1	µA	$V_{GS} = 0$, $V_{DS} = 48V$
				1	mA	$V_{GS} = 0$, $V_{DS} = 48V$ $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	75			mA	$V_{GS} = 4.5V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.3	Ω	$V_{GS} = 4.5V$, $I_D = 75mA$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance	100			m℧	$V_{DS} = 10V$, $I_D = 0.2A$
C_{ISS}	Input Capacitance			60	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 15V$, $I_D = 0.5A$, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.85		V	$I_{SD} = 0.2A$, $V_{GS} = 0$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

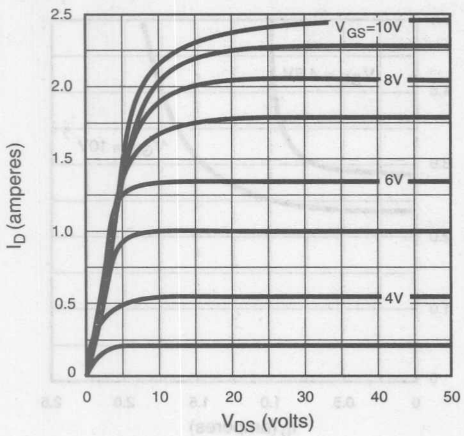
Switching Waveforms and Test Circuit



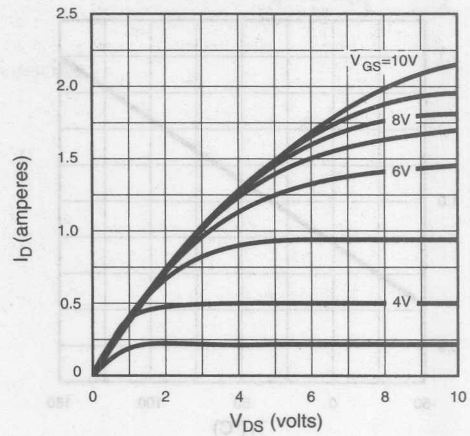


Typical Performance Curves

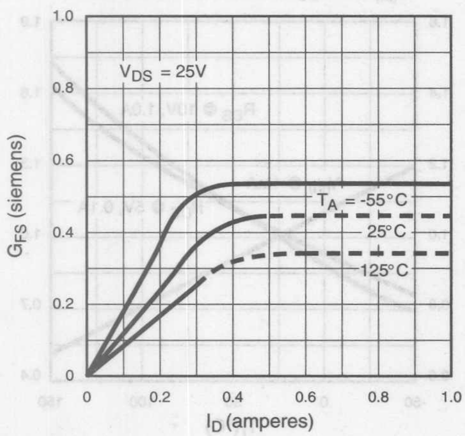
Output Characteristics



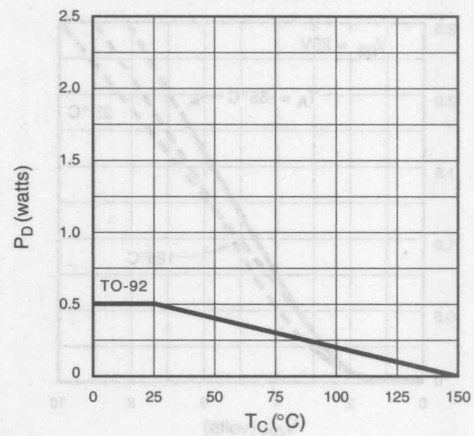
Saturation Characteristics



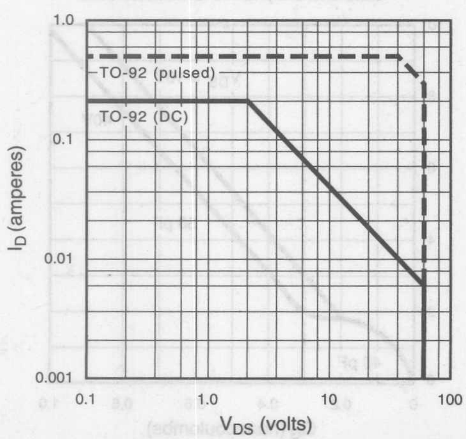
Transconductance vs. Drain Current



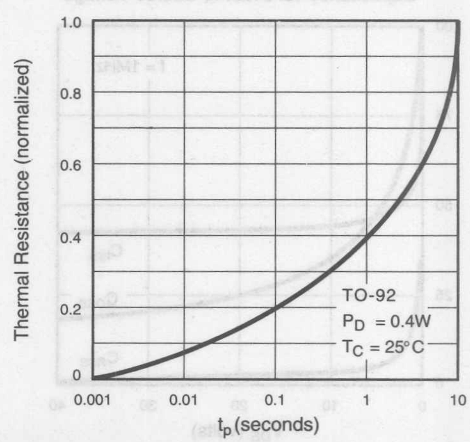
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

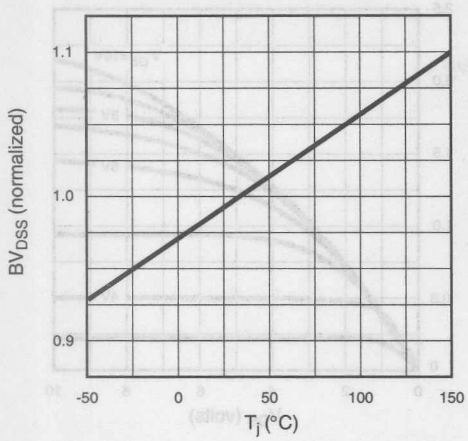


Thermal Response Characteristics

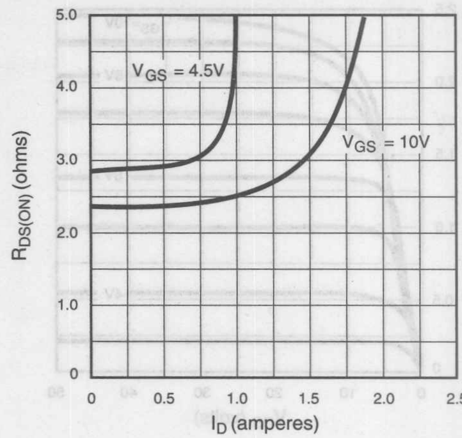


Typical Performance Curves

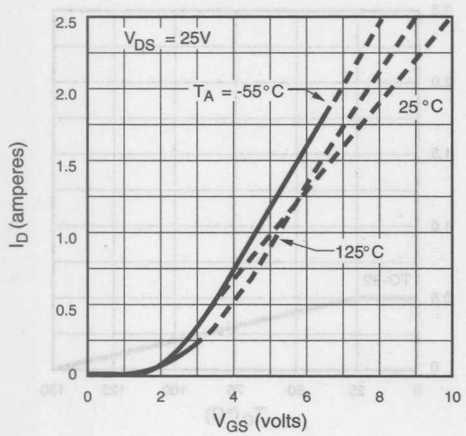
BV$_{DSS}$ Variation with Temperature



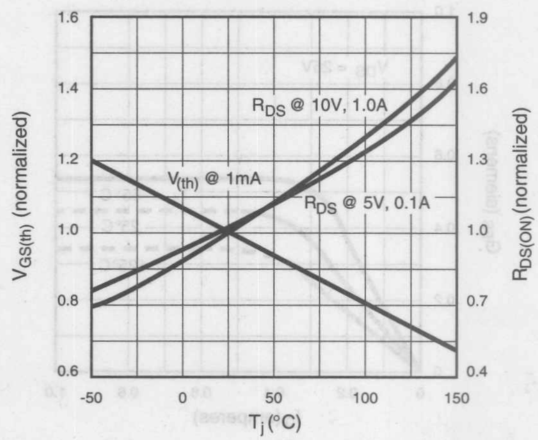
On-Resistance vs. Drain Current



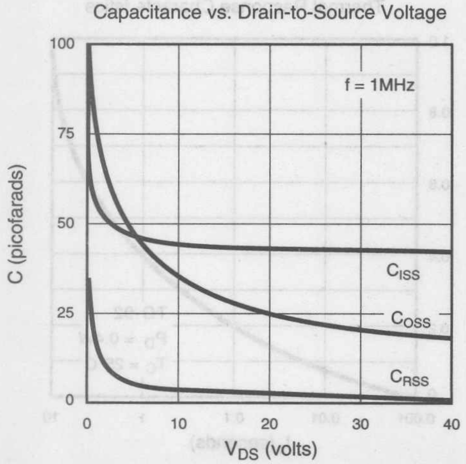
Transfer Characteristics



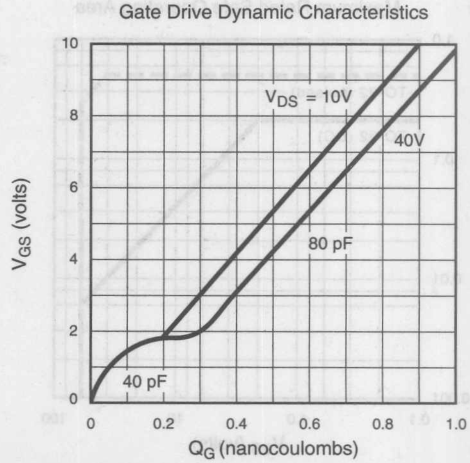
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92
240V	45Ω	150mA	2N7007

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

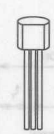
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	65mA	260mA	400mW	312.5	40

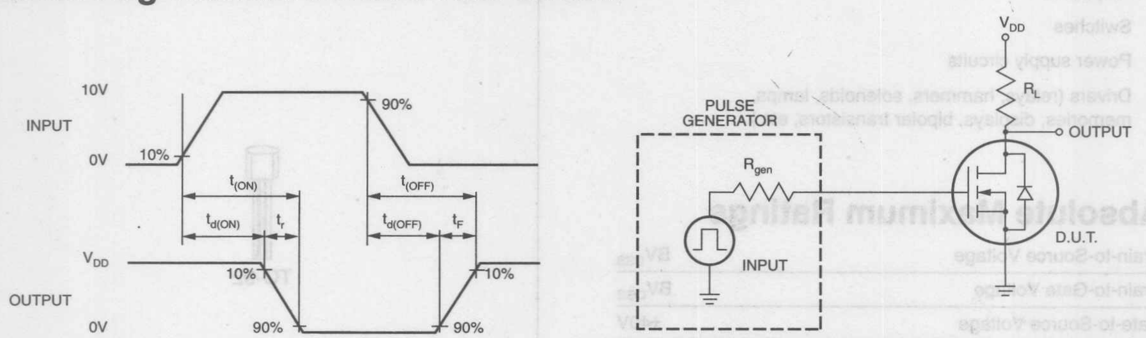
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	240			V	$I_D = 100\mu A$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	1		2.5	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate Body Leakage			10	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			100	nA	$V_{GS} = 0$, $V_{DS} = 120V$
				1	µA	$V_{GS} = 0$, $V_{DS} = 120V$ $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	50			mA	$V_{GS} = 4.5V$, $V_{DS} = 20V$
		150				$V_{GS} = 10V$, $V_{DS} = 20V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			45	Ω	$V_{GS} = 4.5V$, $I_D = 20mA$
				45		$V_{GS} = 10V$, $I_D = 50mA$
G_{FS}	Forward Transconductance	30			m℧	$V_{DS} = 10V$, $I_D = 50mA$
C_{ISS}	Input Capacitance			30	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			15		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			30	ns	$V_{DD} = 60V$, $I_D = 50$ mA, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			20		
V_{SD}	Diode Forward Voltage Drop			1.2	V	$I_{SD} = 65mA$, $V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92
60V	7.5Ω	500mA	2N7008

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

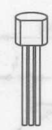
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	150mA	1A	400mW	312.5	40

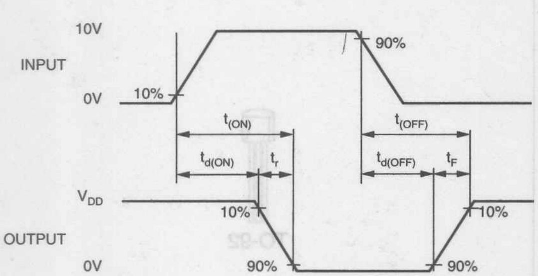
* I_D (continuous) is limited by max rated T_j.

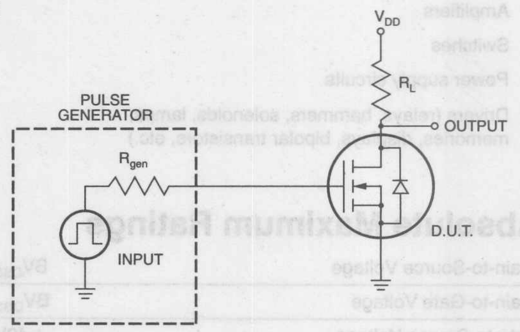
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$I_D = -10\mu A$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	1		2.5	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			1	µA	$V_{GS} = 0$, $V_{DS} = 50V$
				500	µA	$V_{GS} = 0$, $V_{DS} = 50V$, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	500			mA	$V_{GS} = 10V$, $V_{DS} \geq 2V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	$V_{GS} = 5V$, $I_D = 50mA$
				7.5		$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance	80			m℧	$V_{DS} = 10V$, $I_D = 0.2A$
C_{ISS}	Input Capacitance			50	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			20	ns	$V_{DD} = 30V$, $I_D = 200mA$, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			20		
V_{SD}	Diode Forward Voltage Drop			1.5	V	$I_{SD} = 150mA$, $V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

Low Threshold

Preliminary

N-Channel Depletion-Mode Vertical DMOS FETs

Ordering Information

BV_{DSX} / BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)	Order Number / Package				
			TO-39	TO-92	TO-220	TO-243AA*	DIE
350V	25Ω	150mA	DN2535N2	DN2535N3	DN2535N5	—	DN2535ND
400V	25Ω	150mA	DN2540N2	DN2540N3	DN2540N5	DN2540N8	DN2540ND

* Same as SOT-89.

8

Features

- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Normally-on switches
- ☐ Solid state relays
- ☐ Converters
- ☐ Linear amplifiers
- ☐ Constant current sources
- ☐ Power supply circuits
- ☐ Telecom

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

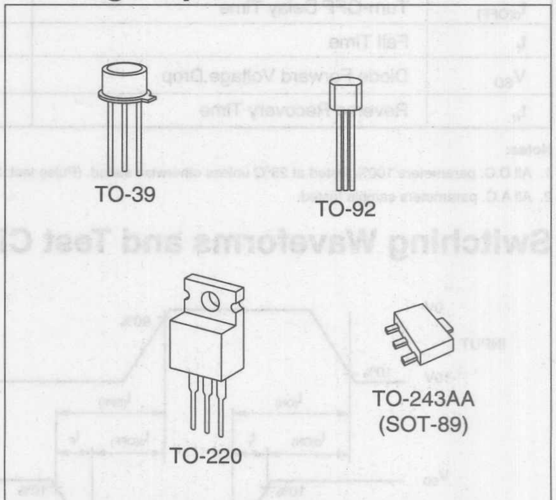
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	300mA	500mA	3.5W	35	125	300mA	500mA
TO-92	120mA	500mA	1.0W	125	120	170mA	500mA
TO-220	500mA	500mA	15.0W	8.3	70	500mA	500mA
TO-243AA	300mA	500mA	—	15	78†	300mA	500mA

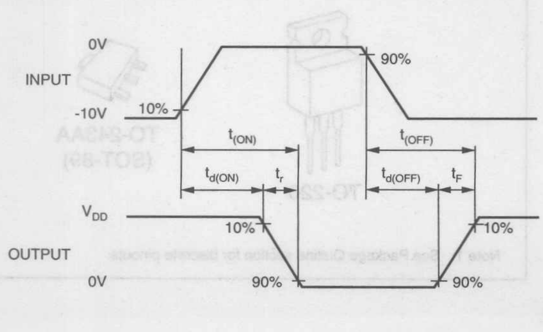
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

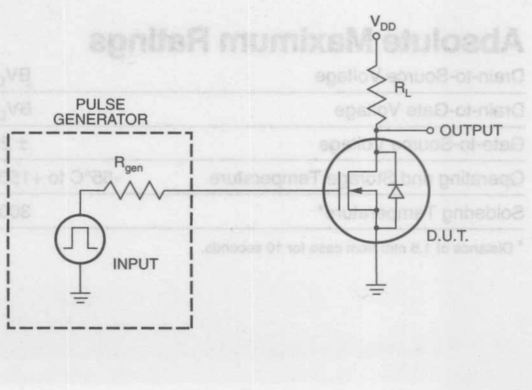
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Source Breakdown Voltage	DN2540	400			V	$V_{GS} = -3.5V$, $I_D = 100\mu A$
		DN2535	350				
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage		-1.0		-5.0	V	$V_{DS} = 25V$, $I_D = 10\mu A$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature				4.5	mV/°C	$V_{DS} = 25V$, $I_D = 10\mu A$
I_{GSS}	Gate Body Leakage Current				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
$I_{D(OFF)}$	Drain-to-Source Leakage Current				10	µA	$V_{GS} = -10V$, V_{DS} = Max Rating
					1	mA	$V_{GS} = -10V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
I_{DSS}	Saturated Drain-to-Source Current		150			mA	$V_{GS} = 0V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			17	25	Ω	$V_{GS} = 0V$, $I_D = 120mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.1	%/°C	$V_{GS} = 0V$, $I_D = 120mA$
G_{FS}	Forward Transconductance			325		m℧	$I_D = 100mA$, $V_{DS} = 10V$
C_{ISS}	Input Capacitance			200	300	pF	$V_{GS} = -10V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			12	30		
C_{RSS}	Reverse Transfer Capacitance			1	5		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 150mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				15		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = -10V$, $I_{SD} = 120mA$
t_{rr}	Reverse Recovery Time			800		ns	$V_{GS} = -10V$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Depletion-Mode MOSFET

Ordering Information

BV_{DSX} / BV_{DGX}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-92	TO-243AA*	Die
500V	1.0KΩ	1.0mA	LND150N3	LND150N8	LND150ND

* Same as SOT-89

Features

- ☐ ESD gate protection
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Excellent thermal stability
- ☐ Integral source-drain diode
- ☐ High input impedance and low C_{ISS}

Applications

- ☐ Solid state relays
- ☐ Normally-on switches
- ☐ Converters
- ☐ Power supply circuits
- ☐ Constant current sources
- ☐ Input protection circuits

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

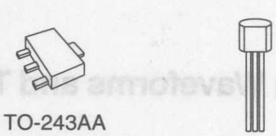
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

The LND1 is a high voltage N-channel depletion mode (normally-on) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND1 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

Package Options



Note 1: See Package Outline section for discrete pinouts.

8

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-92	30mA	30mA	1.0W	125	170	30mA	30mA
TO-243AA	30mA	30mA	—	31	105†	30mA	30mA

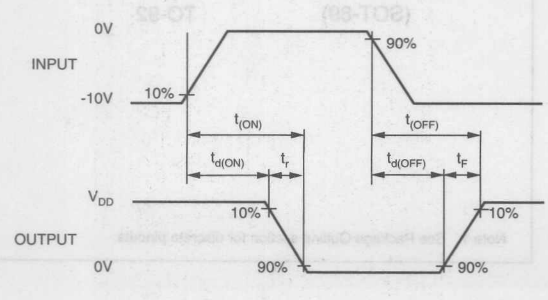
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

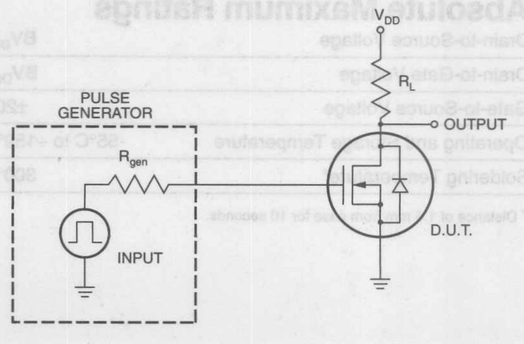
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Source Breakdown Voltage	500			V	V_{GS} = -10V, I_D = 1.0mA
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	-1.0		-3.0	V	V_{DS} = 25V, I_D = 100nA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			5.0	mV/°C	V_{DS} = 25V, I_D = 100nA
I_{GSS}	Gate Body Leakage Current			100	nA	V_{GS} = ±20V, V_{DS} = 0
$I_{D(OFF)}$	Drain-to-Source Leakage Current			100	nA	V_{GS} = -10V, V_{DS} = 450V
				100	µA	V_{GS} = -10V, V_{DS} = 0.8V max rating T_A =125°C
I_{DSS}	Saturated Drain-to-Source Current	1.0		3.0	mA	V_{GS} = 0, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		850	1K	Ω	V_{GS} = 0, I_D = 0.5mA
$\Delta R_{DS(ON)}$	Change in RDS(ON) with Temperature			1.2	%/°C	V_{GS} = 0, I_D = 0.5mA
G_{FS}	Forward Transconductance	1.0	2.0		m℧	V_{GS} = 0, I_D = 1.0mA
C_{ISS}	Input Capacitance		7.5	10.0	pF	V_{GS} = -10V, V_{DS} = 25V f = 1 MHz
C_{OSS}	Output Capacitance		2.0	3.5		
C_{RSS}	Reverse Transfer Capacitance		0.5	1.0		
$t_{d(ON)}$	Turn-ON Delay Time		0.09		µs	V_{DD} = 25V, I_D = 1.0mA, R_{GEN} = 25Ω
tr	Rise Time		0.45			
$t_{d(OFF)}$	Turn-OFF Delay Time		0.1			
t_f	Fall Time		1.3			
V_{SD}	Diode Forward Voltage Drop			0.9	V	V_{GS} = -10V, I_{SD} = 1.0mA
t_{rr}	Reverse Recovery Time		200		ns	V_{GS} = -10V, I_{SD} = 1.0mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

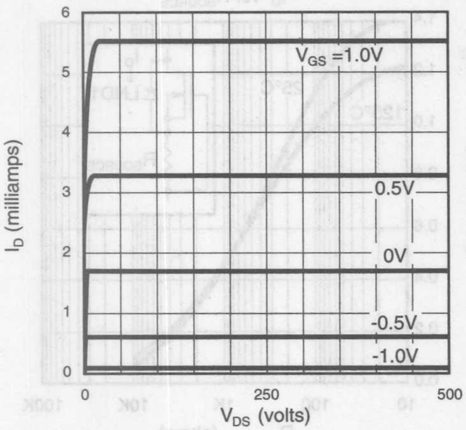
Switching Waveforms and Test Circuit



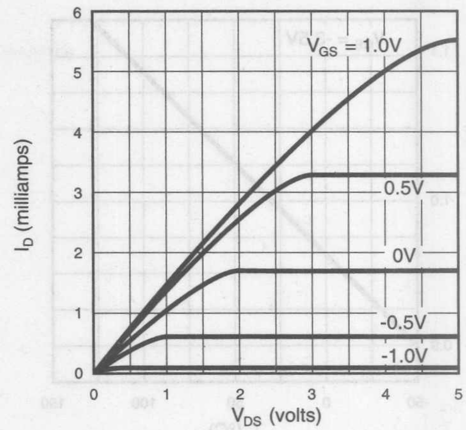


Typical Performance Curves

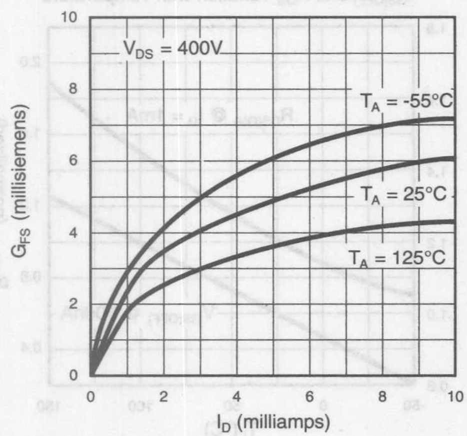
Output Characteristics



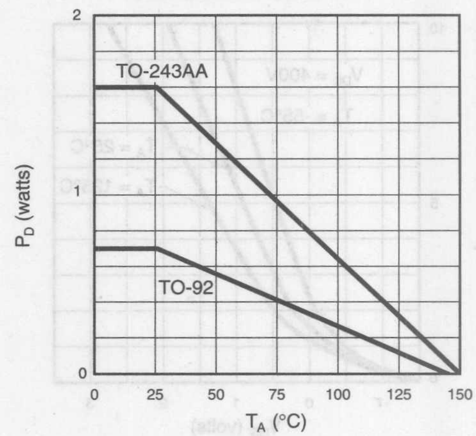
Saturation Characteristics



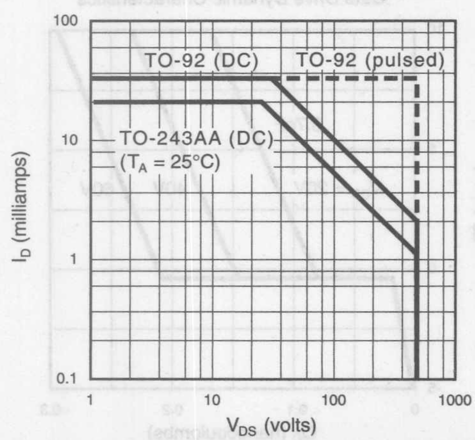
Transconductance vs. Drain Current



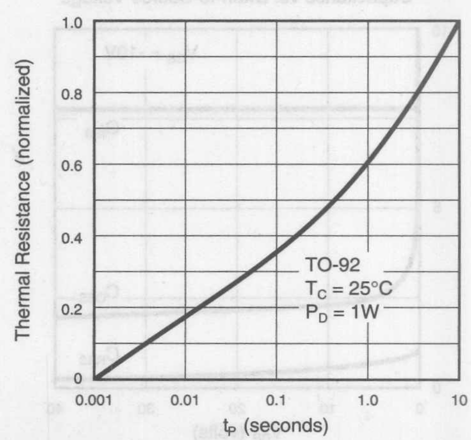
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

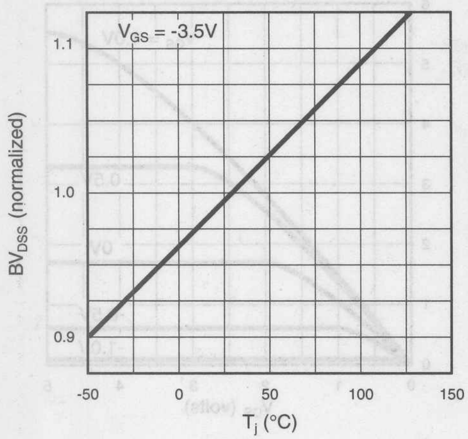


Thermal Response Characteristics

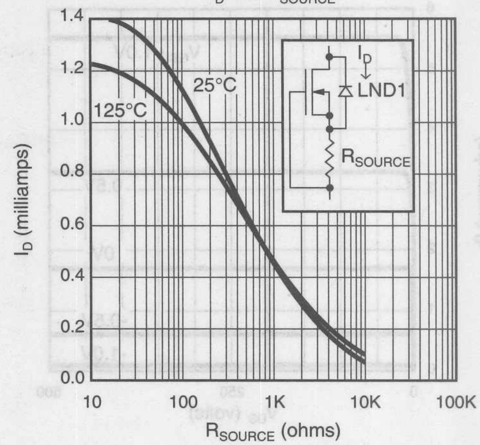


Typical Performance Curves

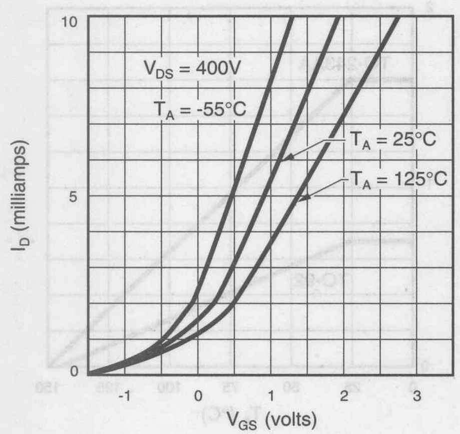
BV_{DSS} Variation with Temperature



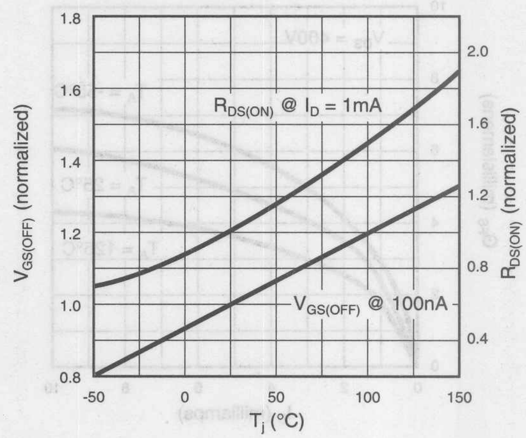
I_D vs. R_{SOURCE}



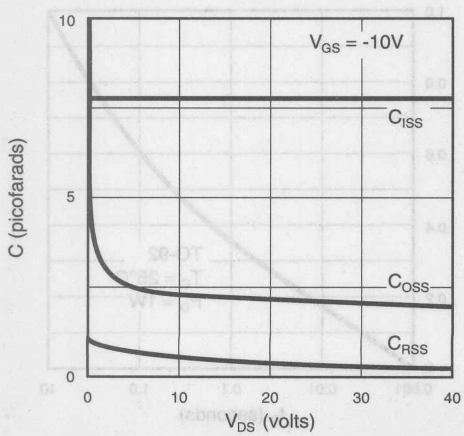
Transfer Characteristics



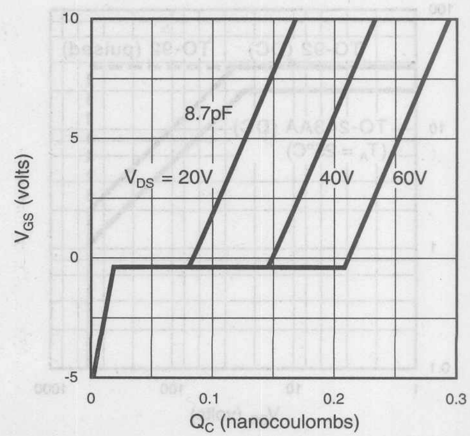
$V_{GS(OFF)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-52	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
40V	3Ω	2.0A	VN0104N2	VN0104N9	VN0104N3	VN0104N5	VN0104N6	VN0104N7	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N9	VN0106N3	VN0106N5	VN0106N6	VN0106N7	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N9	VN0109N3	VN0109N5	—	—	VN0109ND

* 14 pin side brazed ceramic DIP
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

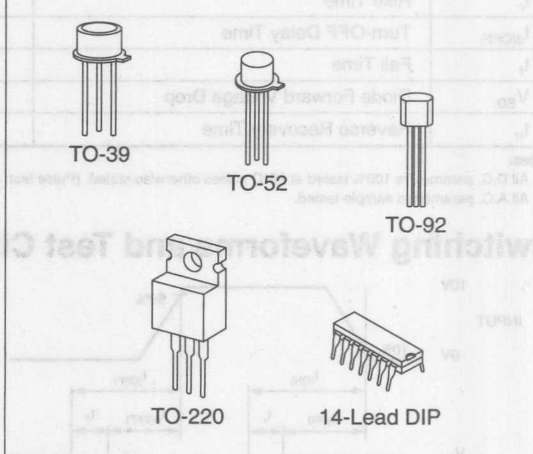
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See package outline section for discrete pinout.
Note 2: See array section for quad pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	0.8A	2.5A	3.5W	125	35	0.8A	2.5A
TO-52	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-220	1.5A	2.5A	15.0W	70	8	1.5A	2.5A
Plastic DIP Ceramic DIP	See DMOS Arrays & Special Functions section						

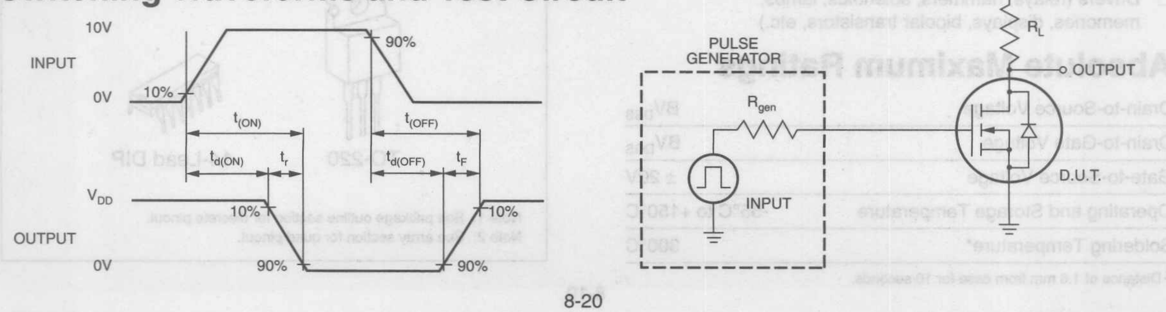
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V	$V_{GS} = 0$, $I_D = 1mA$
		VN0106	60				
		VN0104	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				1	μA	$V_{GS} = 0$, V_{DS} = Max Rating
					100		$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			2.0	2.5			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5	Ω	$V_{GS} = 5V$, $I_D = 250mA$
				2.5	3		$V_{GS} = 10V$, $I_D = 1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1	%/°C	$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance		300	450		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			45	65	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = 25V$ $I_D = 1A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0$, $I_{SD} = 1.0A$

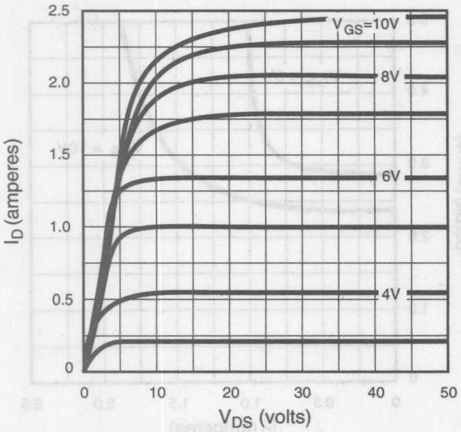
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

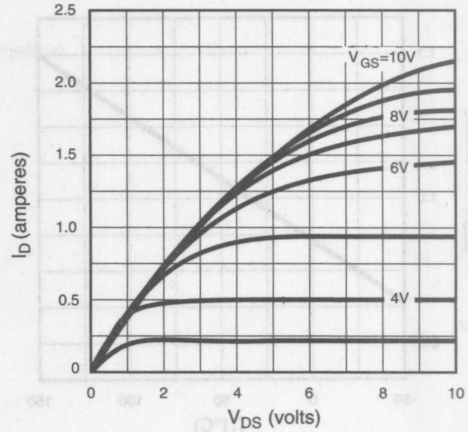


Typical Performance Curves

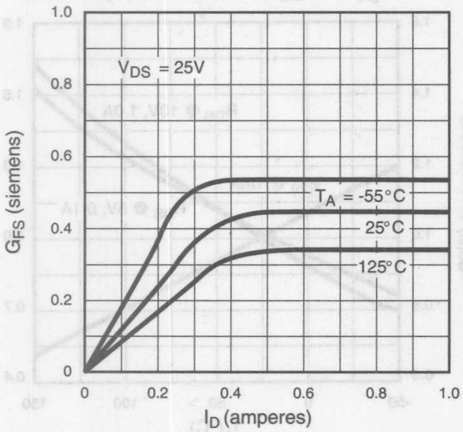
Output Characteristics



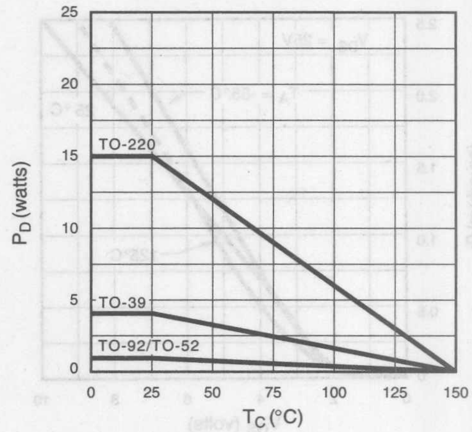
Saturation Characteristics



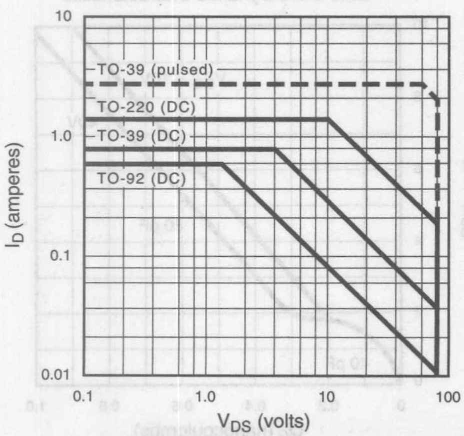
Transconductance vs. Drain Current



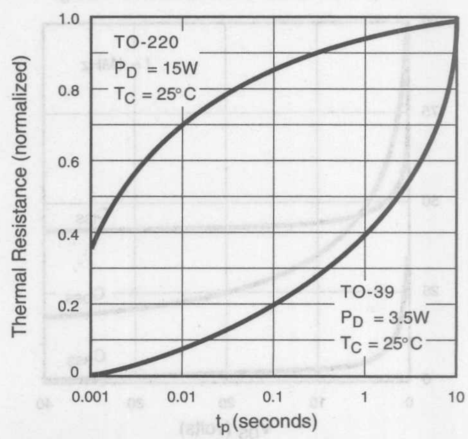
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

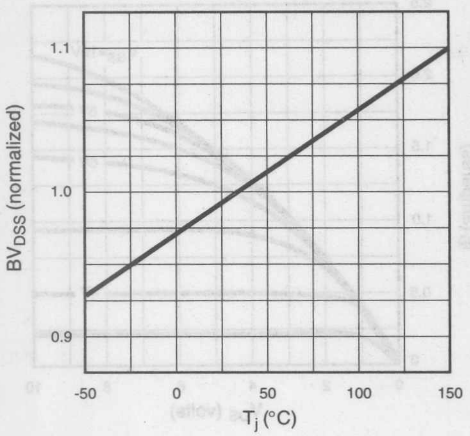


Thermal Response Characteristics

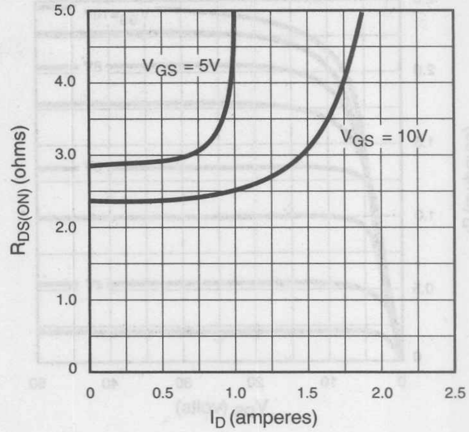


Typical Performance Curves

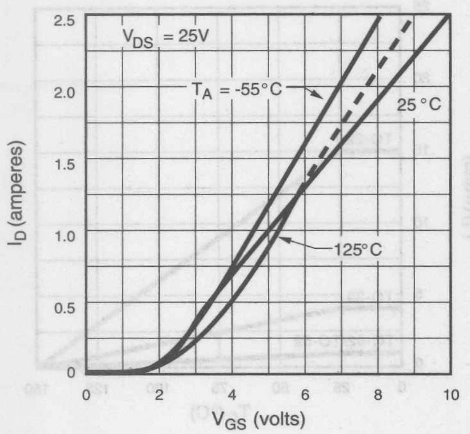
BV_{DSS} Variation with Temperature



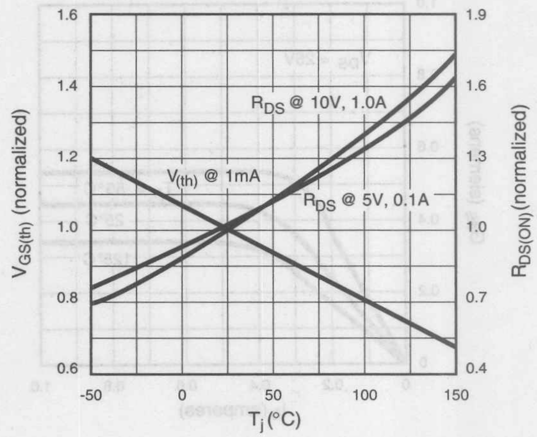
On-Resistance vs. Drain Current



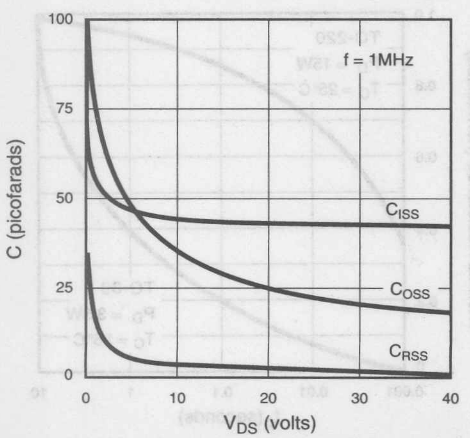
Transfer Characteristics



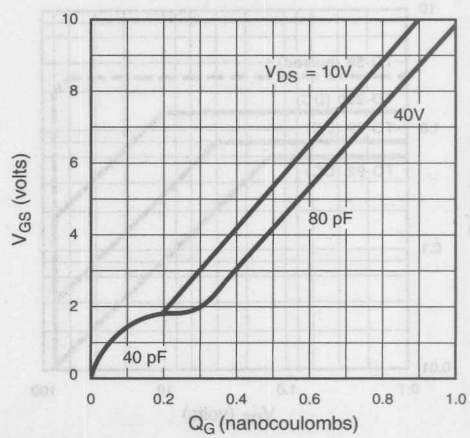
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92	TO-220	Dice†
160V	10Ω	0.4A	VN0116N2	VN0116N3	VN0116N5	VN0116ND
200V	10Ω	0.4A	VN0120N2	VN0120N3	VN0120N5	VN0120ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

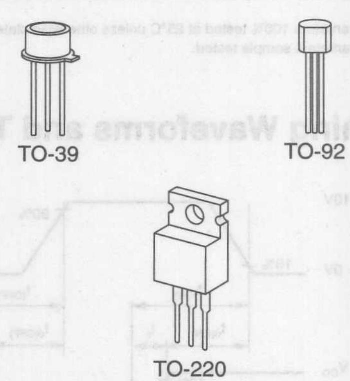
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	350mA	1.0A	3.5W	125	35	350mA	1.0A
TO-92	250mA	0.9A	1.0W	170	125	250mA	0.9A
TO-220	700mA	1.2A	15.0W	70	8.3	700mA	1.2A

* I_D (continuous) is limited by max rated T_j.

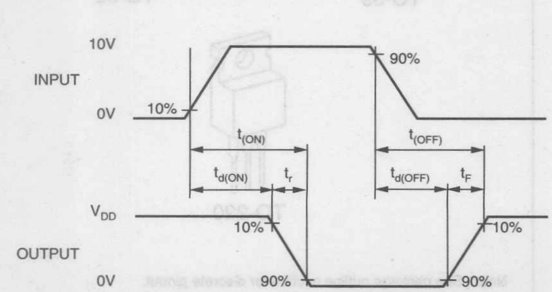
Electrical Characteristics (@ 25°C unless otherwise specified)

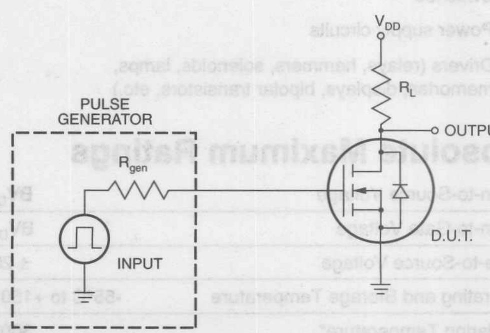
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0120	200			V	$V_{GS} = 0$, $I_D = 1mA$
		VN0116	160				
$V_{GS(th)}$	Gate Threshold Voltage		1		3	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.1	-6.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.3	0.6		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			0.4	0.9			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10	15	Ω	$V_{GS} = 5V$, $I_D = 100mA$
				8	10		$V_{GS} = 10V$, $I_D = 100mA$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			1.0	1.2	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		100	200		m℧	$V_{DS} = 25V$, $I_D = 250mA$
C_{ISS}	Input Capacitance			40	55	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	30		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = 25V$, $I_D = 1A$, $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0$, $I_{SD} = 1.0A$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

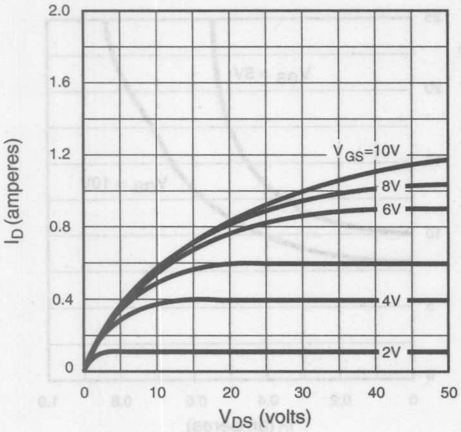
Switching Waveforms and Test Circuit



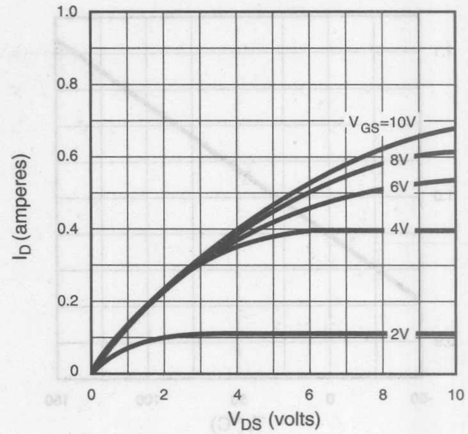


Typical Performance Curves

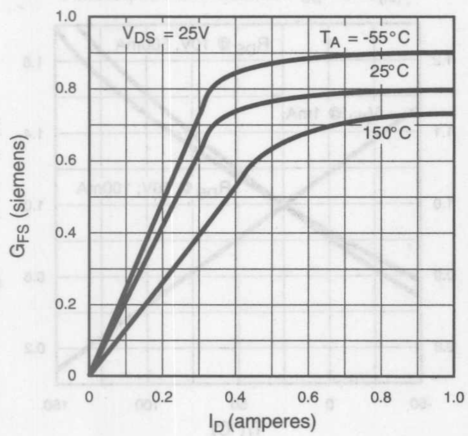
Output Characteristics



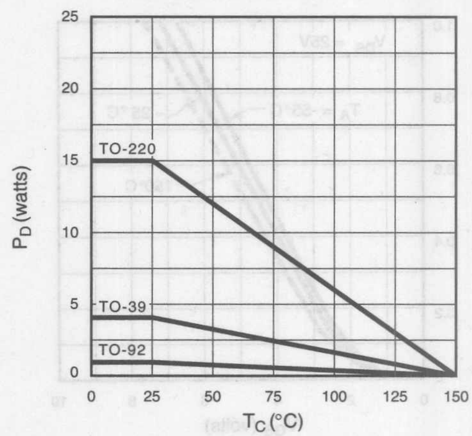
Saturation Characteristics



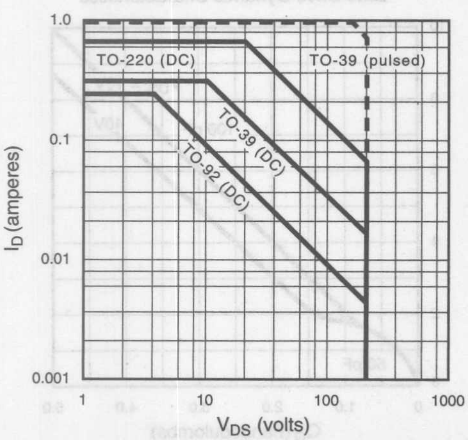
Transconductance vs. Drain Current



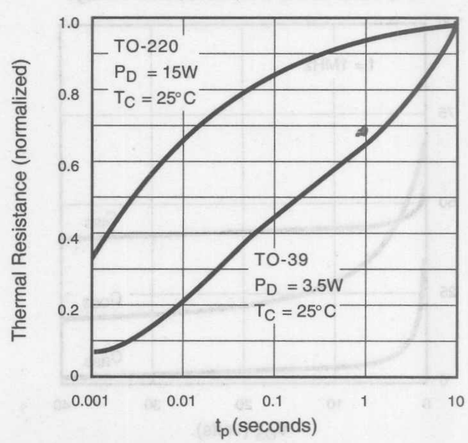
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

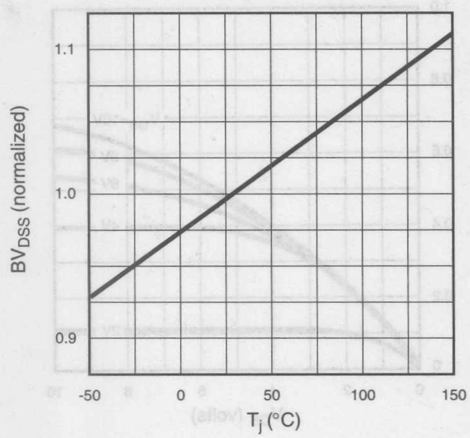


Thermal Response Characteristics

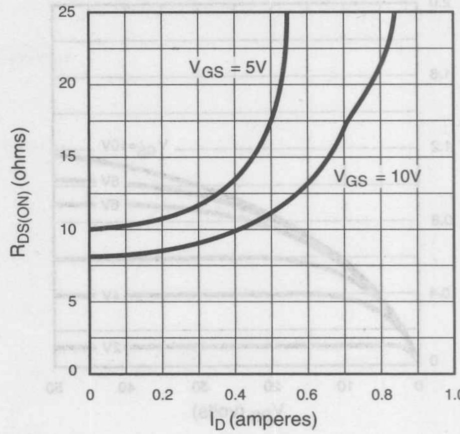


Typical Performance Curves

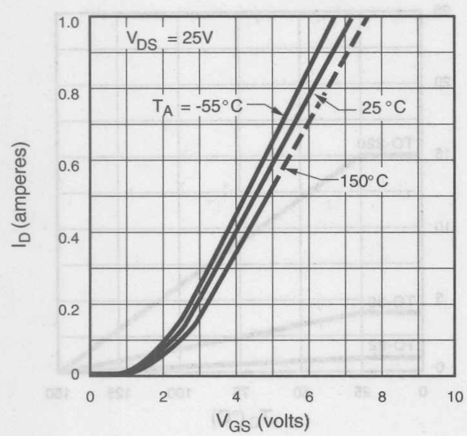
BV_{DSS} Variation with Temperature



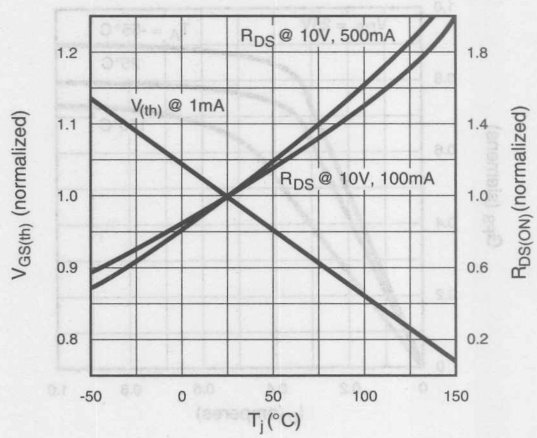
On-Resistance vs. Drain Current



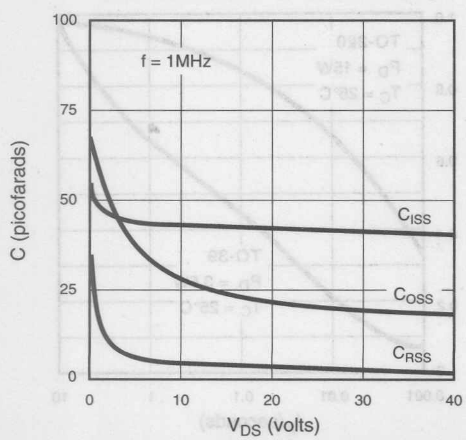
Transfer Characteristics



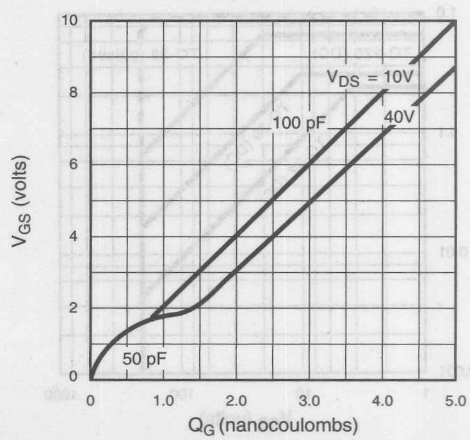
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS}/ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-3	TO-39	TO-220	Dice†
350V	2.5Ω	3A	VN0335N1	VN0335N2	VN0335N5	VN0335ND
400V	2.5Ω	3A	VN0340N1	VN0340N2	VN0340N5	VN0340ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

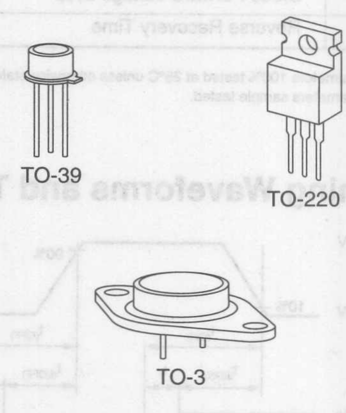
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-3	3.5A	8A	100W	30	1.25	3.5A	8.0A
TO-39	1.0A	7A	6W	125	20.8	1.0A	7.0A
TO-220	2.1A	8A	50W	40	2.5	2.1A	8.0A

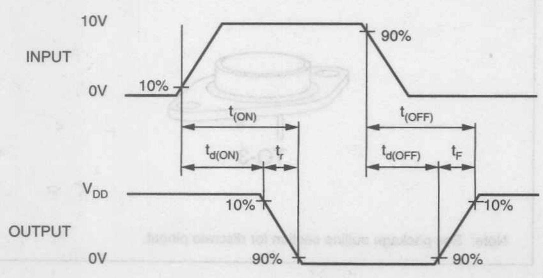
* I_D (continuous) is limited by max rated T_j.

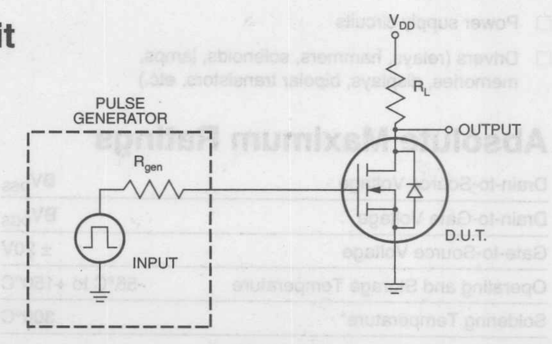
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0340	400			V	$V_{GS} = 0$, $I_D = 10mA$
		VN0335	350				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}$, $I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	-6.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 10mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					2.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			5.0		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			3.0	6.0			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.2		Ω	$V_{GS} = 5V$, $I_D = 0.5A$
				1.8	2.5		$V_{GS} = 10V$, $I_D = 1A$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			1	2	%/°C	$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance		1	1.25		℧	$V_{DS} = 25V$, $I_D = 1A$
C_{ISS}	Input Capacitance			550	650	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75	125		
C_{RSS}	Reverse Transfer Capacitance			25	50		
$t_{d(ON)}$	Turn-ON Delay Time			12	20	ns	$V_{DD} = 25V$, $I_D = 1A$, $R_{GEN} = 10\Omega$
t_r	Rise Time			12	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			20	30		
V_{SD}	Diode Forward Voltage Drop			1.1	1.5	V	$V_{GS} = 0$, $I_{SD} = 1A$
t_{rr}	Reverse Recovery Time			450		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

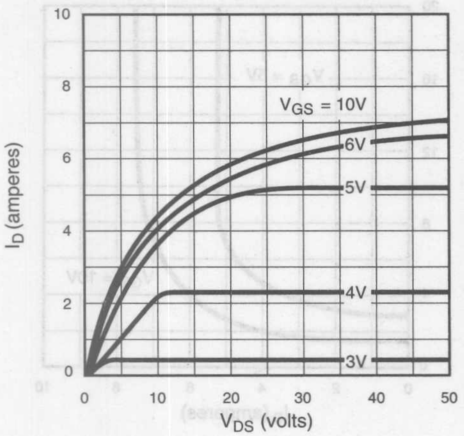
Switching Waveforms and Test Circuit



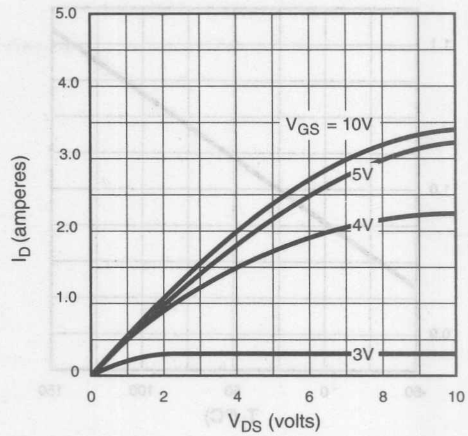


Typical Performance Curves

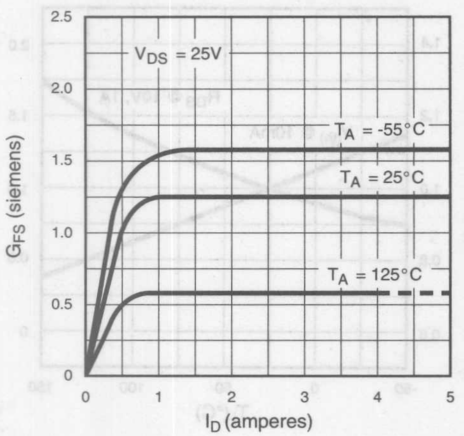
Output Characteristics



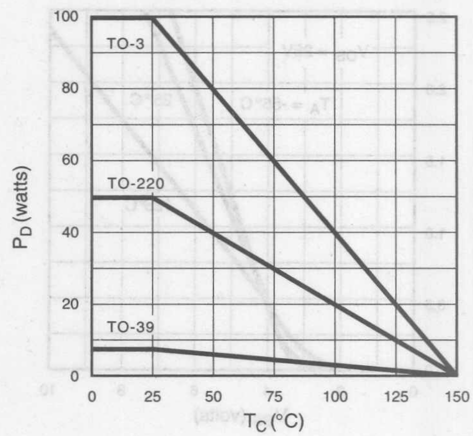
Saturation Characteristics



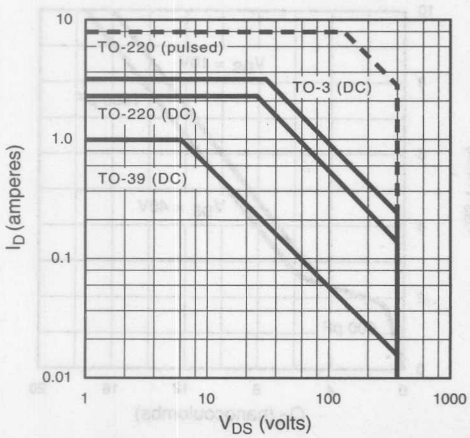
Transconductance vs. Drain Current



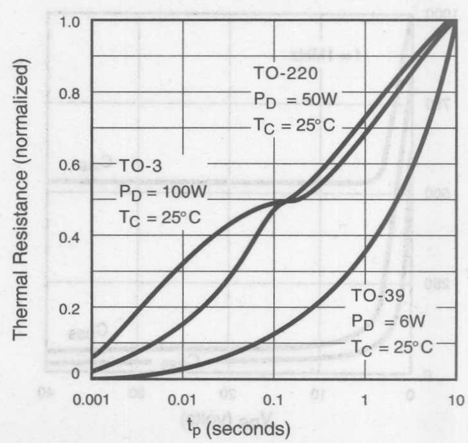
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

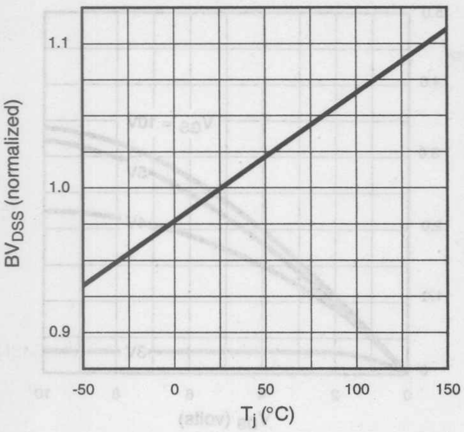


Thermal Response Characteristics

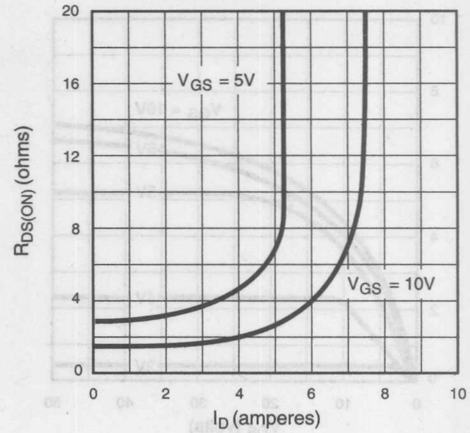


Typical Performance Curves

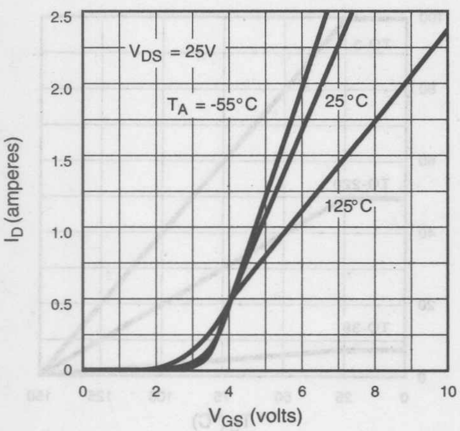
BV$_{DSS}$ Variation with Temperature



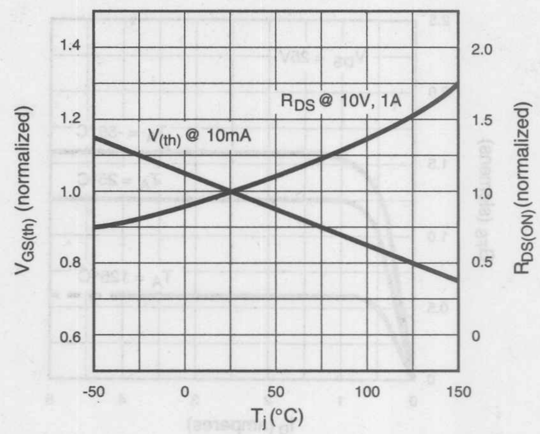
On-Resistance vs. Drain Current



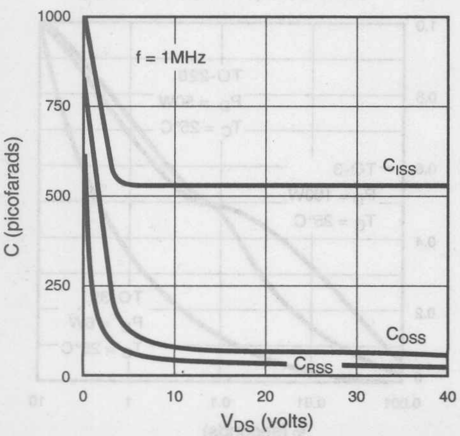
Transfer Characteristics



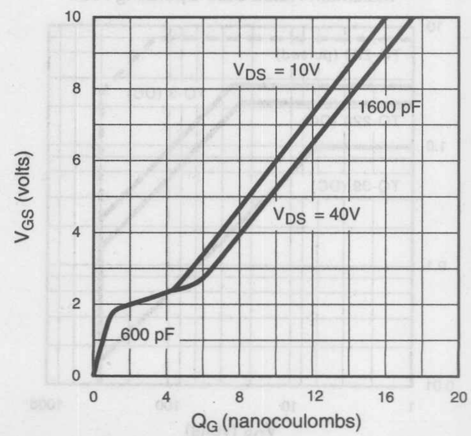
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-3	TO-39	TO-220	Dice†
450V	4Ω	2A	VN0345N1	VN0345N2	VN0345N5	VN0345ND
500V	4Ω	2A	VN0350N1	VN0350N2	VN0350N5	VN0350ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

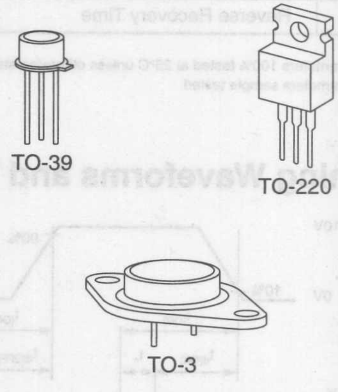
Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

8

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-3	2.5A	5.0A	100W	30	1.25	2.5A	5.0A
TO-39	0.35A	4.5A	6W	125	20.8	0.35A	4.5A
TO-220	1.5A	5.0A	50W	40	2.5	1.5A	5.0A

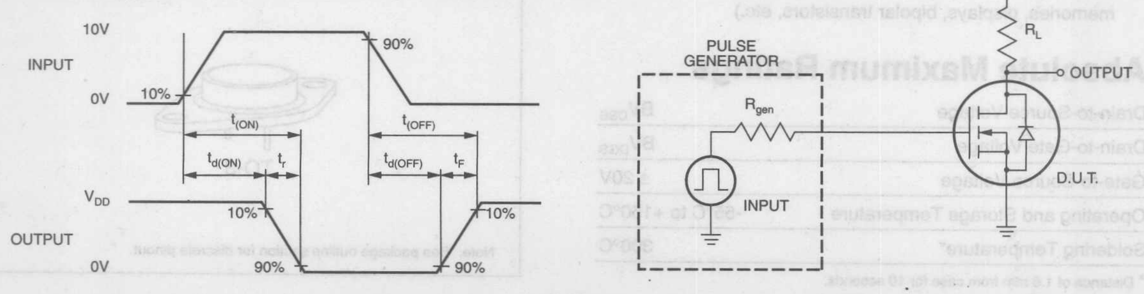
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0350	500			V	$V_{GS} = 0$, $I_D = 10mA$
		VN0345	450				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}$, $I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-7.0	-9.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 10mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					2.0	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			2.6		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			2.0	6.5			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.5		Ω	$V_{GS} = 5V$, $I_D = 0.5A$
				2.8	4.0		$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			1	1.5	%/°C	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance		500	1000		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			550	650	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			90	125		
C_{RSS}	Reverse Transfer Capacitance			15	50		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	$V_{DD} = 25V$, $I_D = 1A$, $R_{GEN} = 10\Omega$
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			15	25		
V_{SD}	Diode Forward Voltage Drop			1.3	1.8	V	$V_{GS} = 0$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			450		ns	$V_{GS} = 0$, $I_{SD} = 0.5A$

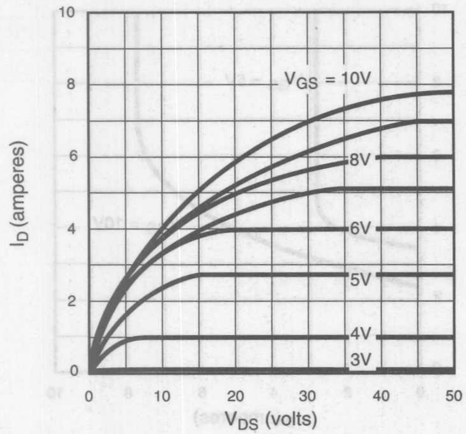
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

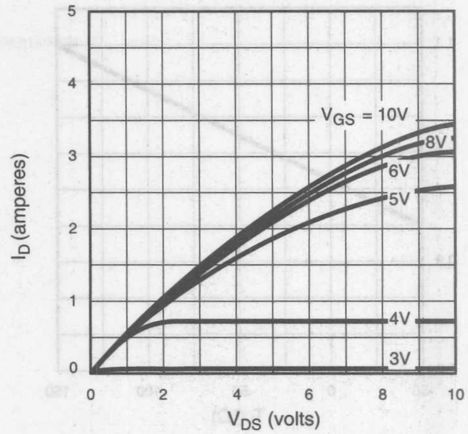


Typical Performance Curves

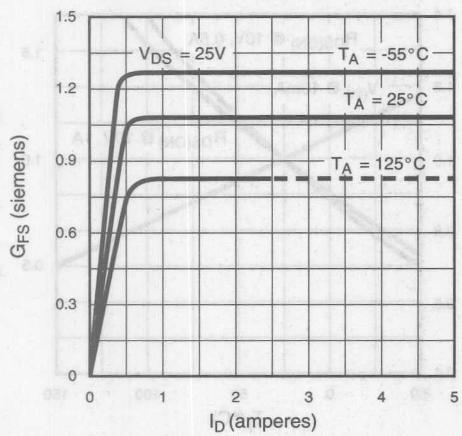
Output Characteristics



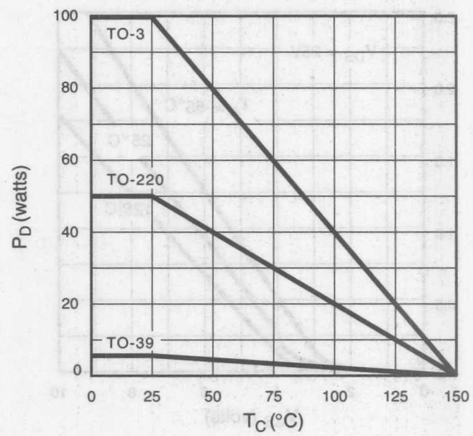
Saturation Characteristics



Transconductance vs. Drain Current



Power Dissipation vs. Case Temperature



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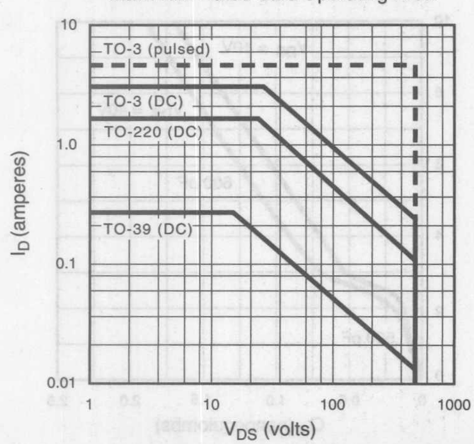
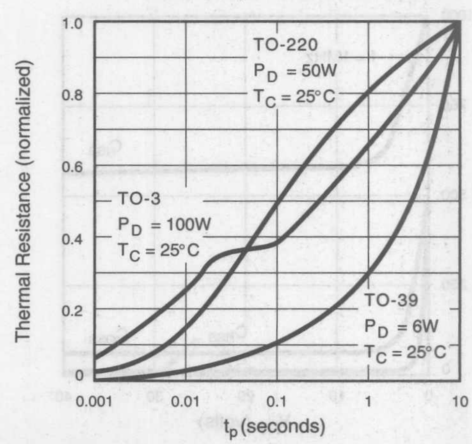
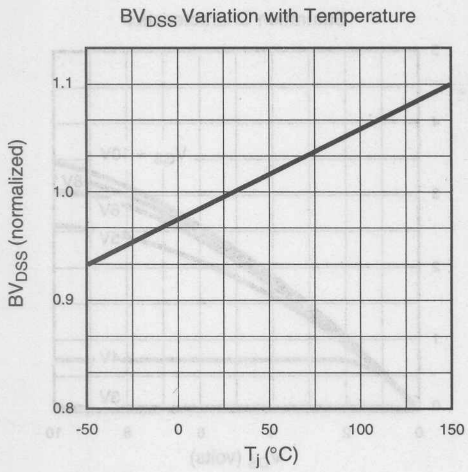
Maximum Rated Safe Operating Area

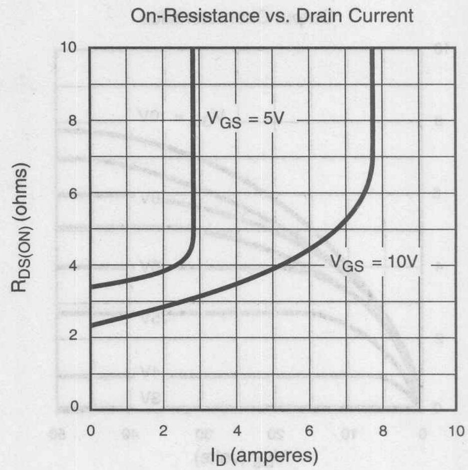


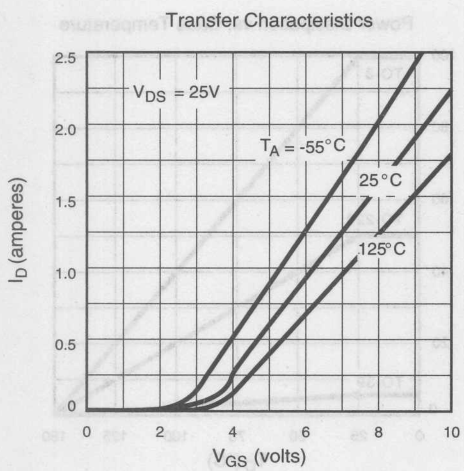
Thermal Response Characteristics

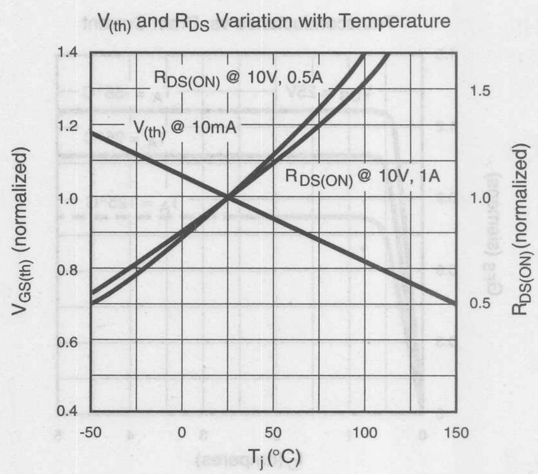


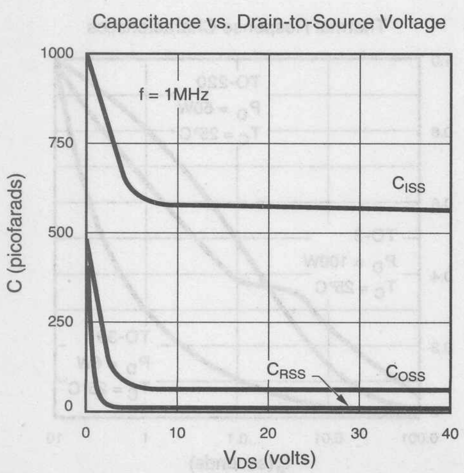
Typical Performance Curves

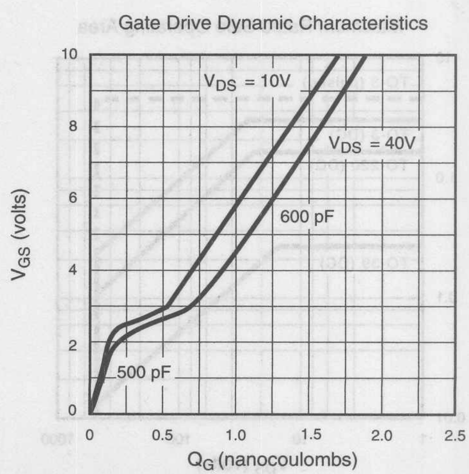












N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-3	TO-220	Dice†
550V	6Ω	1.5A	VN0355N1	VN0355N5	VN0355ND
600V	6Ω	1.5A	VN0360N1	VN0360N5	VN0360ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

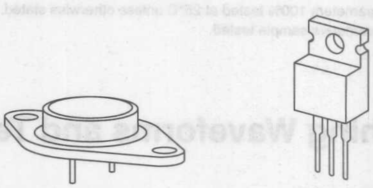
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-3 TO-220

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-3	2.5A	6A	100W	2.5	1.25	2.5A	6.0A
TO-220	1.5A	6A	50W	30	2.5	1.5A	6.0A

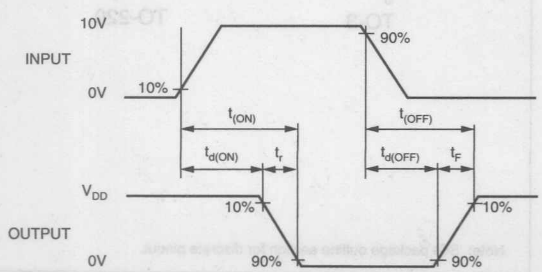
* I_D (continuous) is limited by max rated T_j.

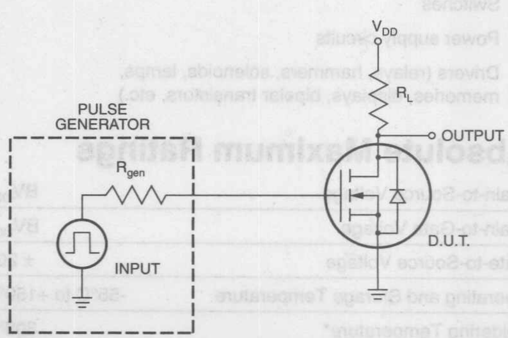
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0360	600			V	$V_{GS} = 0, I_D = 10mA$
		VN0355	550				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}, I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	-6.0	mV/°C	$V_{GS} = V_{DS}, I_D = 10mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	$V_{GS} = 0, V_{DS}$ = Max Rating
					2.0	mA	$V_{GS} = 0, V_{DS}$ = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			2.1		A	$V_{GS} = 5V, V_{DS} = 25V$
			1.5	3.2			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.5		Ω	$V_{GS} = 5V, I_D = 0.5A$
				4.0	6.0		$V_{GS} = 10V, I_D = 0.5A$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			1	2	%/°C	$V_{GS} = 10V, I_D = 0.5A$
G_{FS}	Forward Transconductance		0.5	0.6		℧	$V_{DS} = 25V, I_D = 0.5A$
C_{ISS}	Input Capacitance			550	650	pF	$V_{GS} = 0, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75	125		
C_{RSS}	Reverse Transfer Capacitance			25	50		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	$V_{DD} = 25V$, $I_D = 0.5A$, $R_{GEN} = 10\Omega$
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			12	25		
V_{SD}	Diode Forward Voltage Drop			1.1	1.5	V	$V_{GS} = 0, I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time			450		ns	$V_{GS} = 0, I_{SD} = 0.5A$

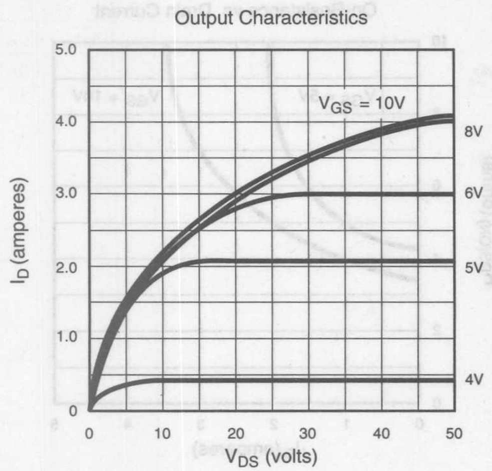
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

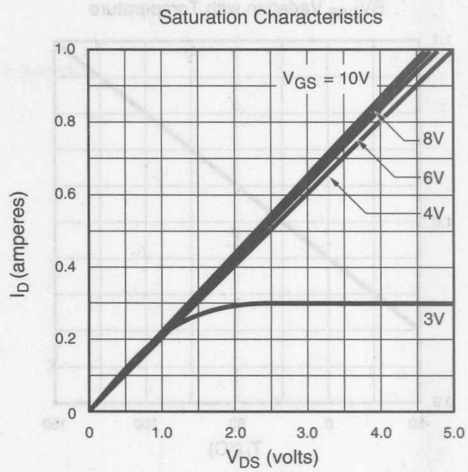
Switching Waveforms and Test Circuit

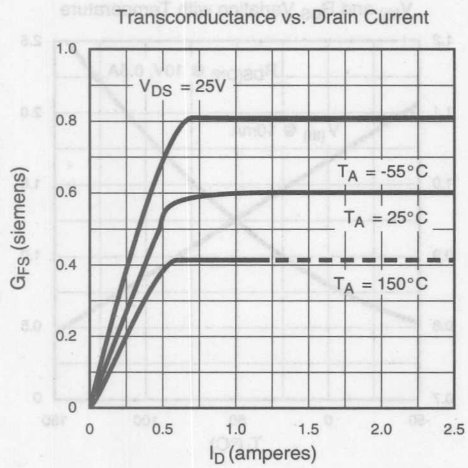


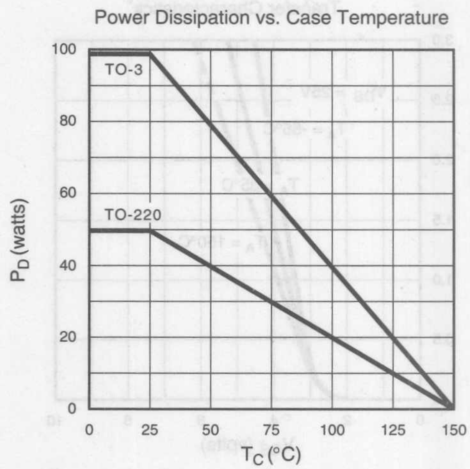


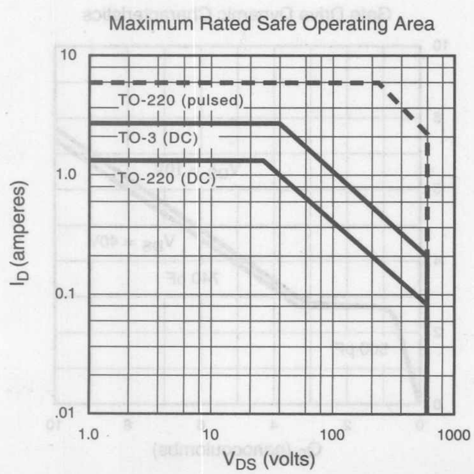
Typical Performance Curves

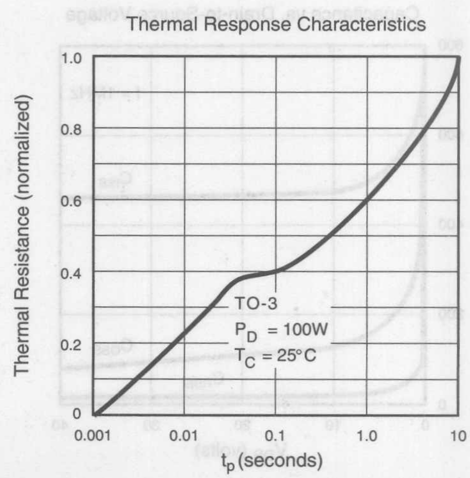


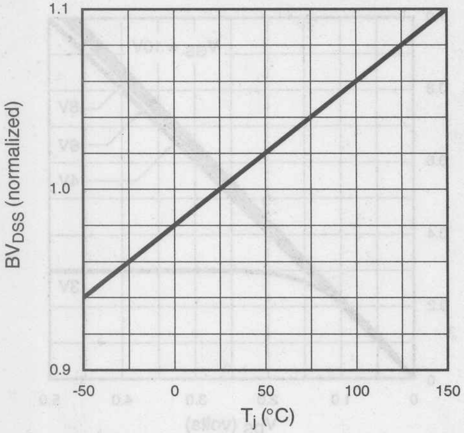


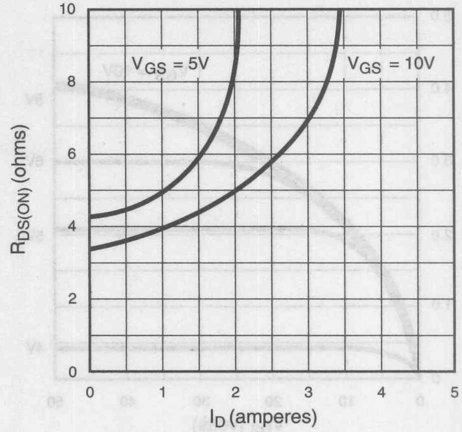




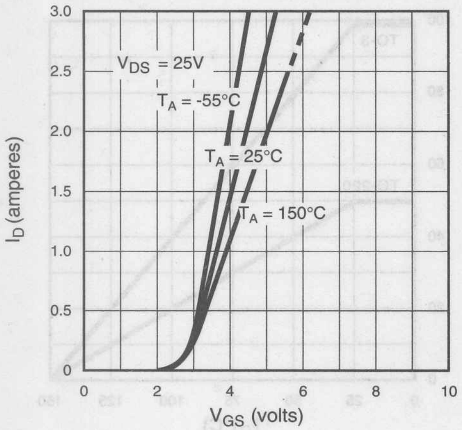




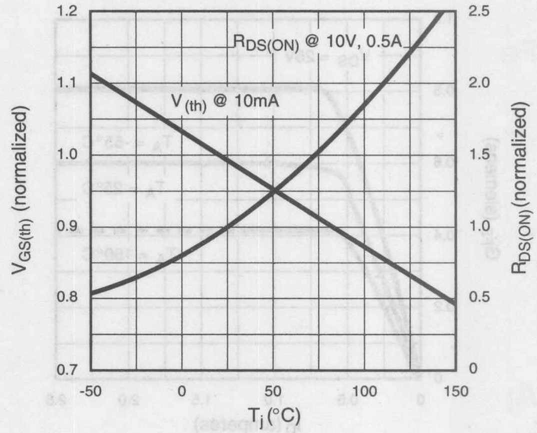




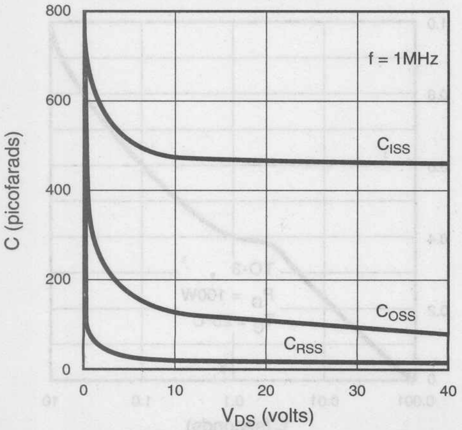
Transfer Characteristics



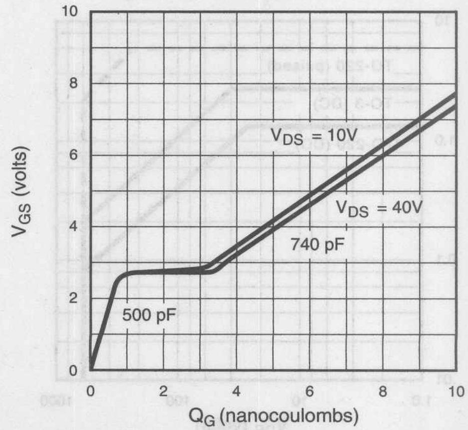
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
30V	1.2Ω	1.0A	VN0300B	VN0300L

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

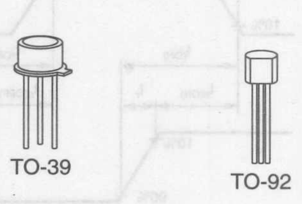
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	1.51A	3A	5W	170	20
TO-92	0.64A	3A	2W	156	40

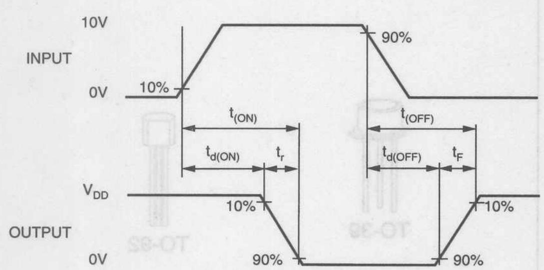
* I_D (continuous) is limited by max rated T_j.

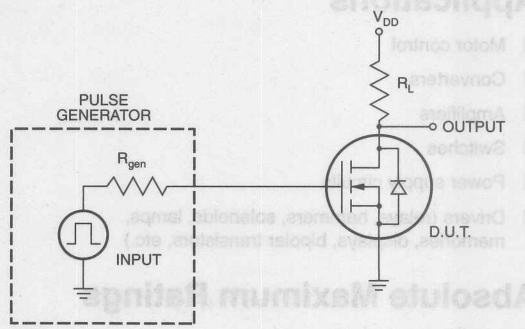
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30			V	$V_{GS} = 0$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
				500		$V_{GS} = 0$, $V_{DS} = 30V$ $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1			A	$V_{GS} = 0.1V$, $V_{DS} \geq 2V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resostance			3.3	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
				1.2		$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance	200			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			190	pF	$V_{GS} = 0V$, $V_{DS} = 20V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			110		
C_{RSS}	Reverse Transfer Capacitance			50		
$t_{(ON)}$	Turn-ON Time			30	ns	$V_{DD} = 25V$, $I_D = 1.0A$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		0.9		V	$I_{SD} = 0.63A$, $V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	Dice†
350V	35Ω	250mA	VN0535N2	VN0535N3	VN0535ND
400V	35Ω	250mA	VN0540N2	VN0540N3	VN0540ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

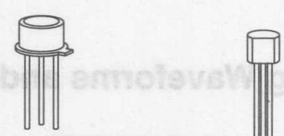
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39 TO-92

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	250mA	500mA	6.0W	125	20.8	250mA	500mA
TO-92	100mA	400mA	1.0W	170	125	100mA	400mA

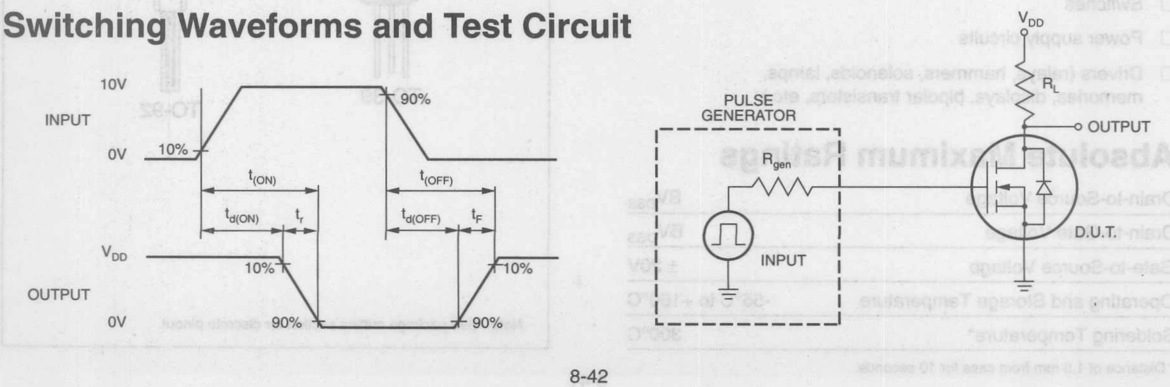
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0540	400			V	$V_{GS} = 0$, $I_D = 1mA$
		VN0535	350				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					500		$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			300		mA	$V_{GS} = 5V$, $V_{DS} = 25V$
			250	340			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			30		Ω	$V_{GS} = 5V$, $I_D = 20mA$
				25	35		$V_{GS} = 10V$, $I_D = 0.1A$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			0.9	1.5	%/°C	$V_{GS} = 10V$, $I_D = 0.1A$
G_{FS}	Forward Transconductance		100	180		m℧	$V_{DS} = 25V$, $I_D = 0.1A$
C_{ISS}	Input Capacitance			45	55	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			8	10		
C_{RSS}	Reverse Transfer Capacitance			2	5		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 250mA$ $R_{GEN} = 25Ω$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				10		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop			0.8		V	$V_{GS} = 0$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0$, $I_{SD} = 0.5A$

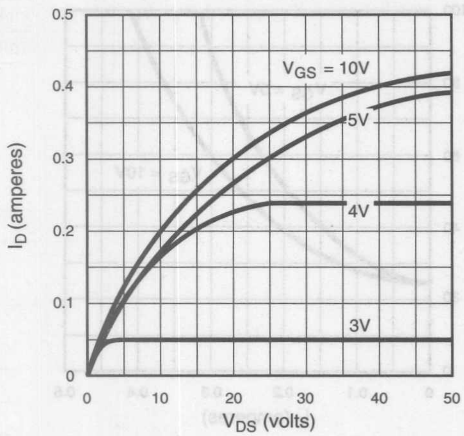
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

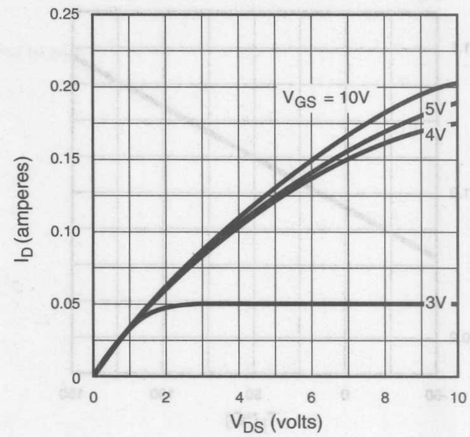


Typical Performance Curves

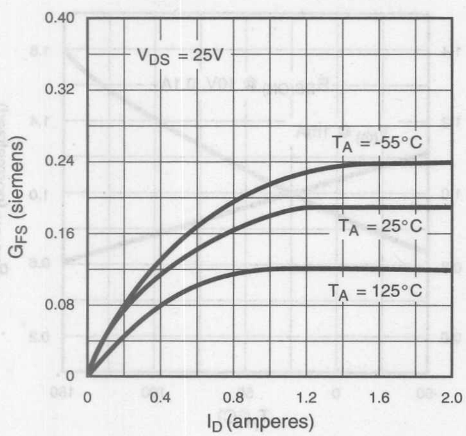
Output Characteristics



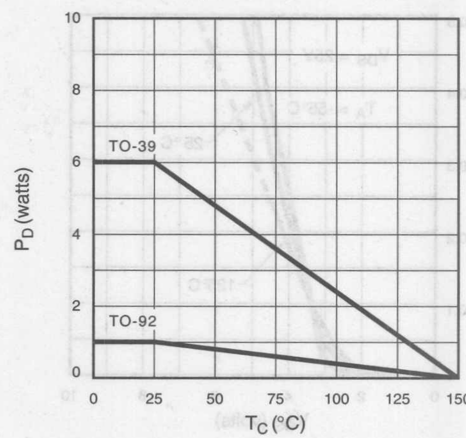
Saturation Characteristics



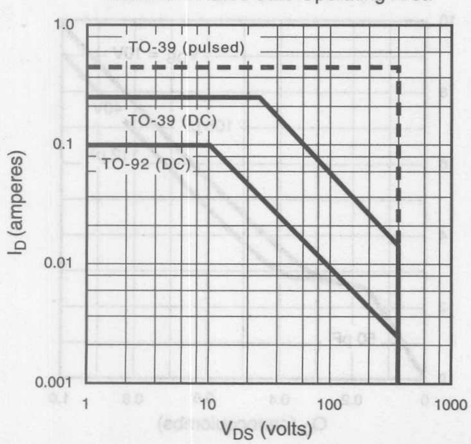
Transconductance vs. Drain Current



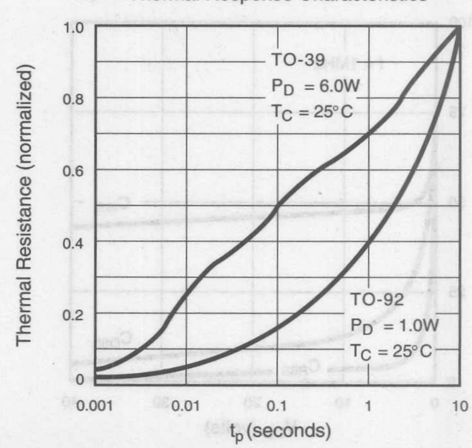
Power Dissipation vs. Case Temperature



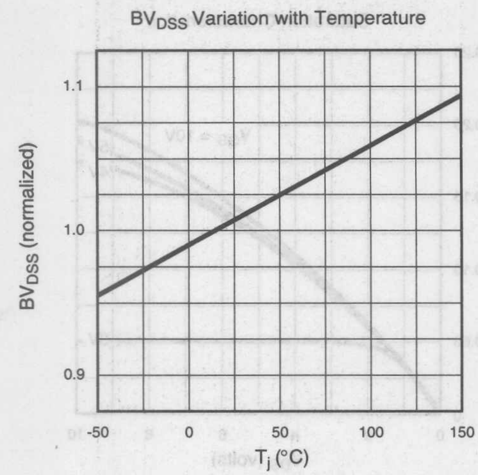
Maximum Rated Safe Operating Area

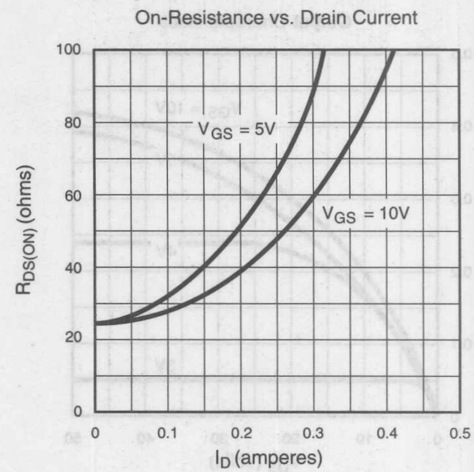


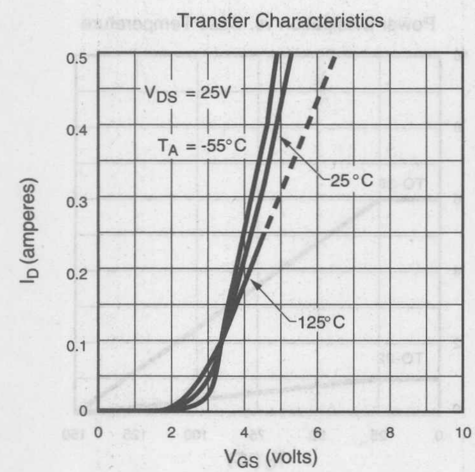
Thermal Response Characteristics

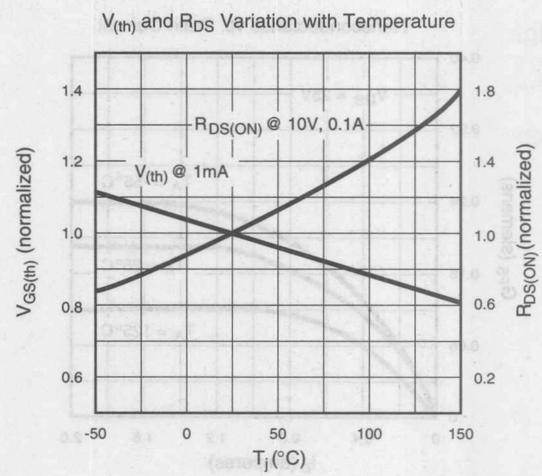


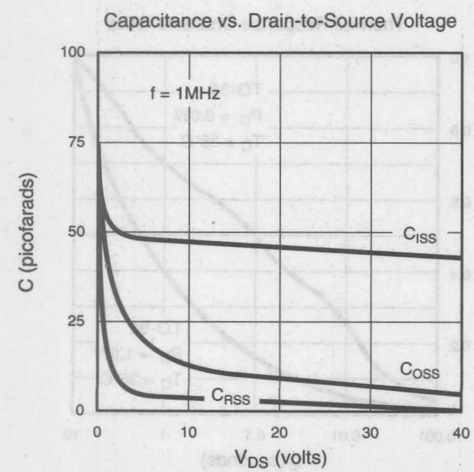
Typical Performance Curves

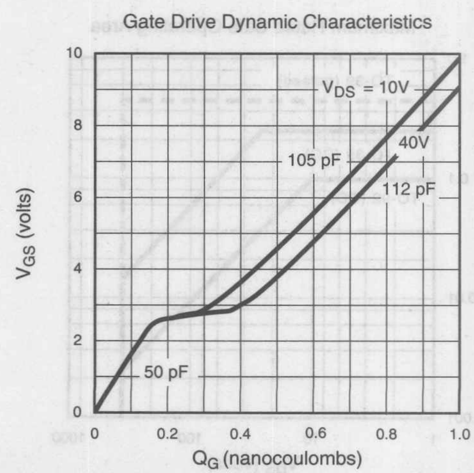












N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	Dice†
450V	60Ω	150mA	VN0545N2	VN0545N3	VN0545ND
500V	60Ω	150mA	VN0550N2	VN0550N3	VN0550ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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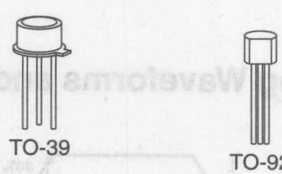
Package Options



Note: See package outline section for discrete pinout.

TO-39	100mA	300mA	6.0W	125	20	100mA	300mA
TO-92	50mA	250mA	1.0W	170	125	50mA	250mA

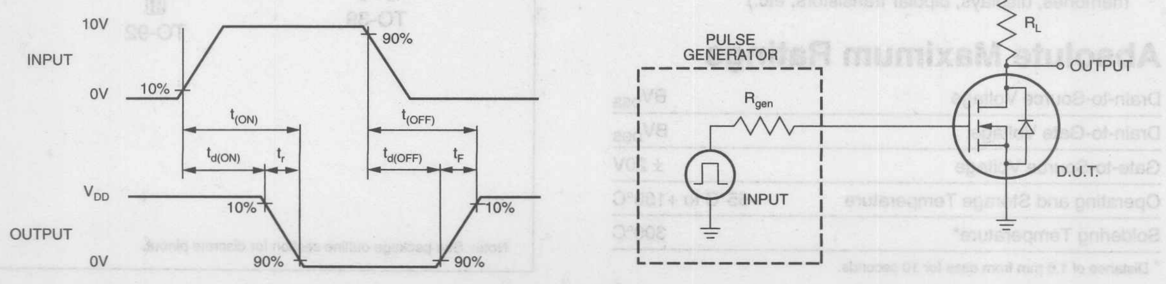
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage — VN0550	500			V	$V_{GS} = 0V$, $I_D = 1mA$
	VN0545	450				
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8	-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
				1000		$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		100		mA	$V_{GS} = 5V$, $V_{DS} = 25V$
		150	350			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		45		Ω	$V_{GS} = 5V$, $I_D = 50mA$
			40	60		$V_{GS} = 10V$, $I_D = 50mA$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature		1	1.7	%/°C	$V_{GS} = 10V$, $I_D = 50mA$
G_{FS}	Forward Transconductance	50	100		m℧	$V_{DS} = 25V$, $I_D = 50mA$
C_{ISS}	Input Capacitance		45	55	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance		8	10		
C_{RSS}	Reverse Transfer Capacitance		2	5		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V$, $I_D = 150mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			10		
t_f	Fall Time			10		
V_{SD}	Diode Forward Voltage Drop		0.8		V	$V_{GS} = 0V$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V$, $I_{SD} = 0.5A$

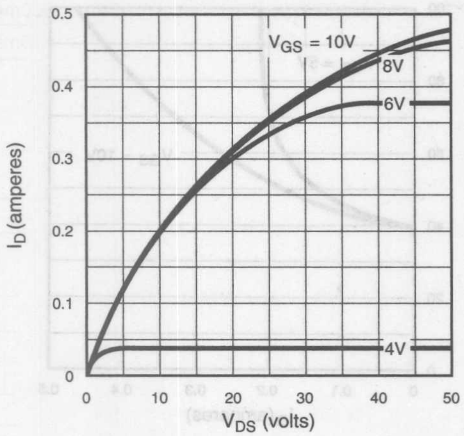
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

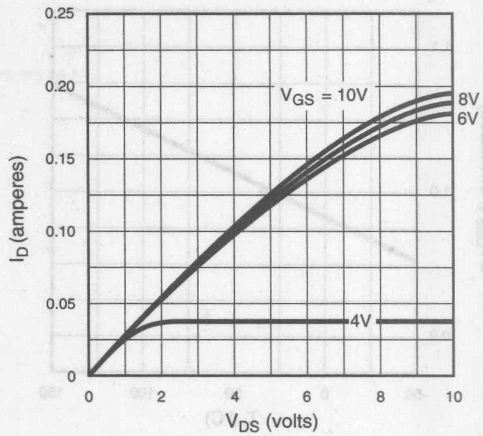


Typical Performance Curves

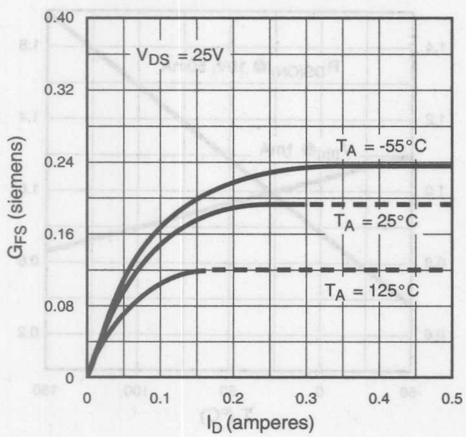
Output Characteristics



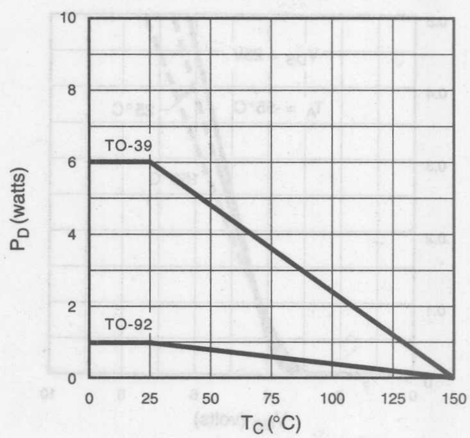
Saturation Characteristics



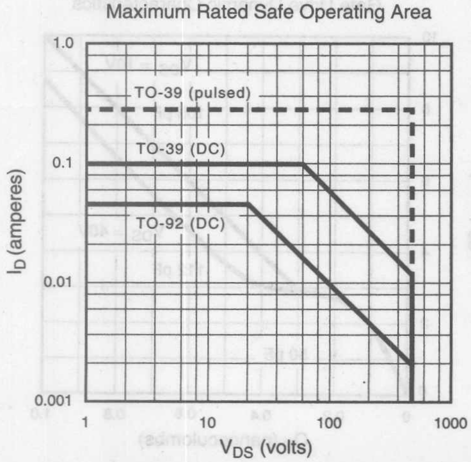
Transconductance vs. Drain Current



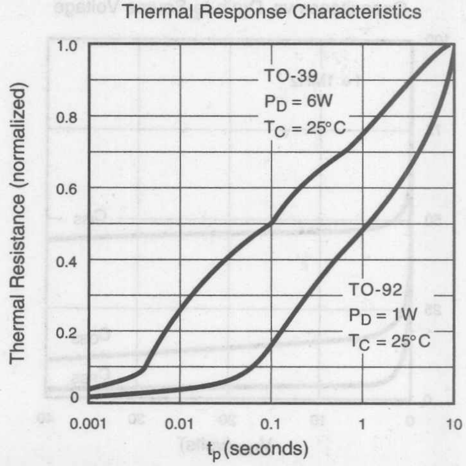
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

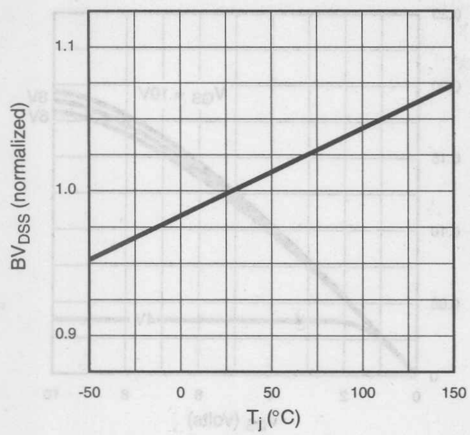


Thermal Response Characteristics

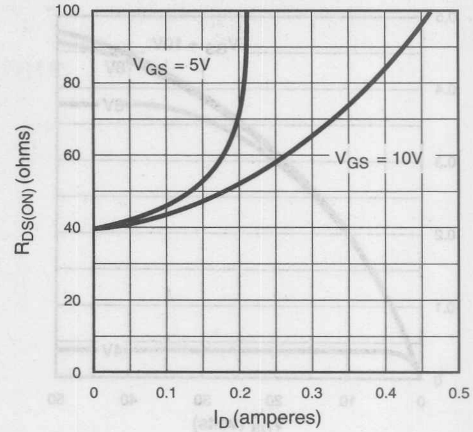


Typical Performance Curves

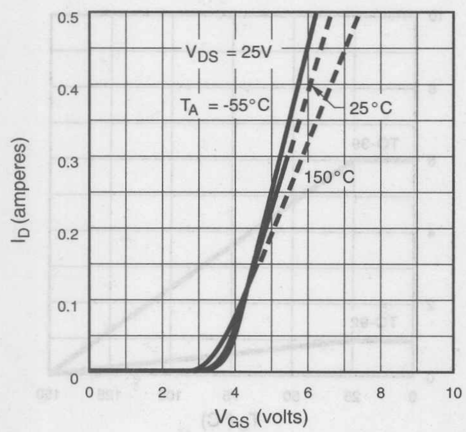
BV$_{DSS}$ Variation with Temperature



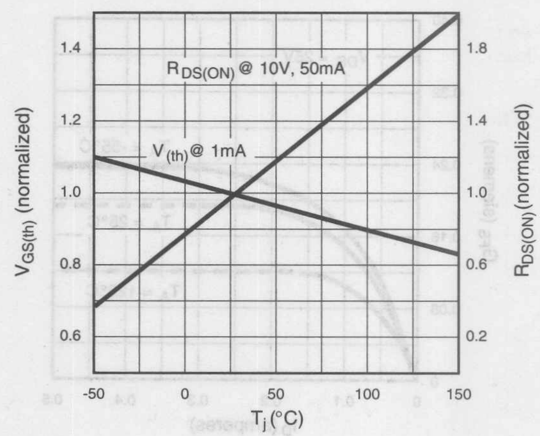
On-Resistance vs. Drain Current



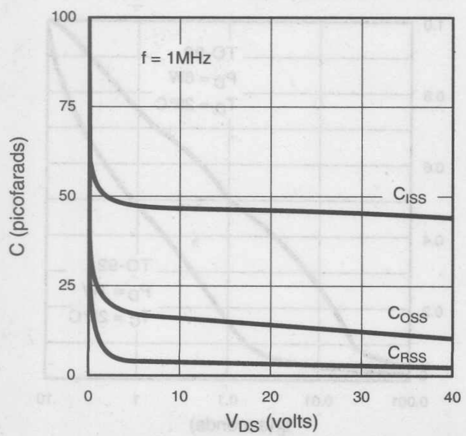
Transfer Characteristics



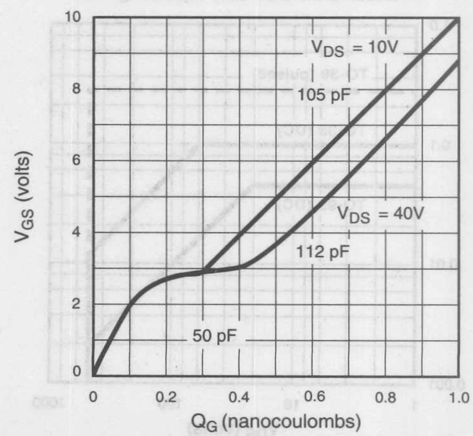
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	Dice†
350V	10Ω	0.75A	VN0635N2	VN0635N3	VN0635N5	VN0635ND
400V	10Ω	0.75A	VN0640N2	VN0640N3	VN0640N5	VN0640ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

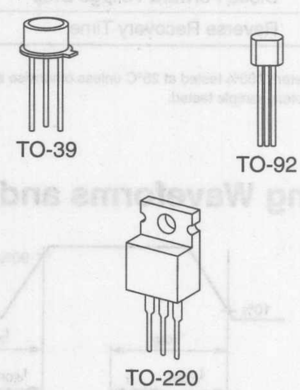
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

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TO-39	0.6A	2.5A	6W	125	21	0.6A	2.5A
TO-92	0.25A	1.5A	1W	170	125	0.25A	1.5A
TO-220	1.6A	2.5A	45W	70	2.7	1.6A	2.5A

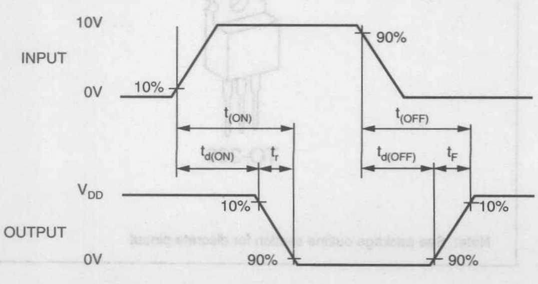
* I_D (continuous) is limited by max rated T_j.

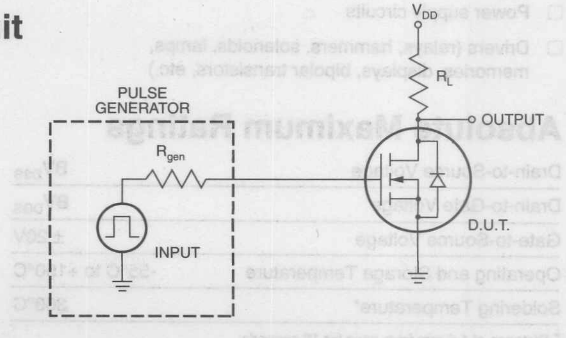
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0635	350			V	$V_{GS} = 0V$, $I_D = 2mA$
		VN0640	400				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}$, $I_D = 2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 2mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			0.6		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			0.75				$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8		Ω	$V_{GS} = 5V$, $I_D = 100mA$
				8	10		$V_{GS} = 10V$, $I_D = 500mA$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		100	160		m℧	$V_{DS} = 25V$, $I_D = 500mA$
C_{ISS}	Input Capacitance			105	130	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 0.5A$, $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0V$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0V$, $I_{SD} = 0.5A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

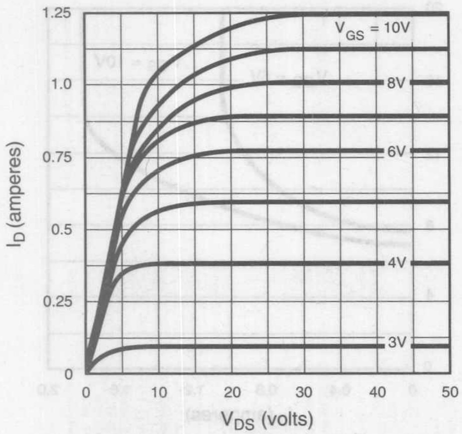
Switching Waveforms and Test Circuit



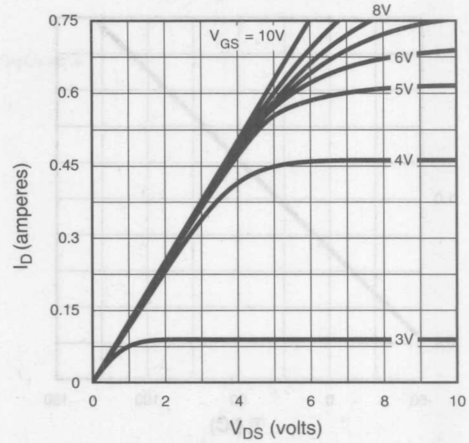


Typical Performance Curves

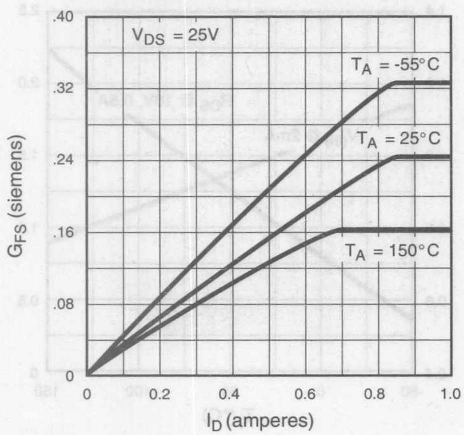
Output Characteristics



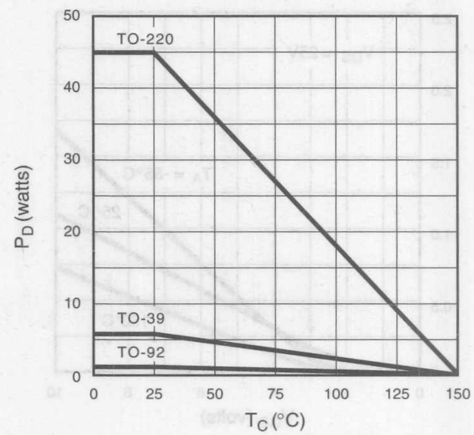
Saturation Characteristics



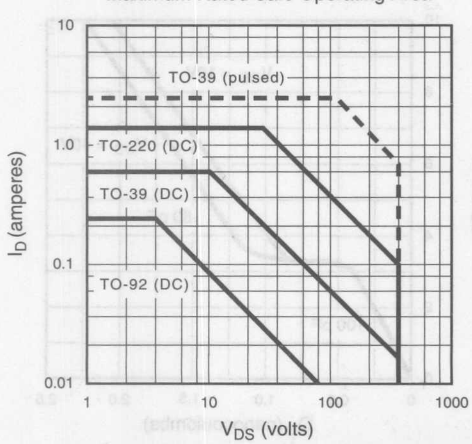
Transconductance vs. Drain Current



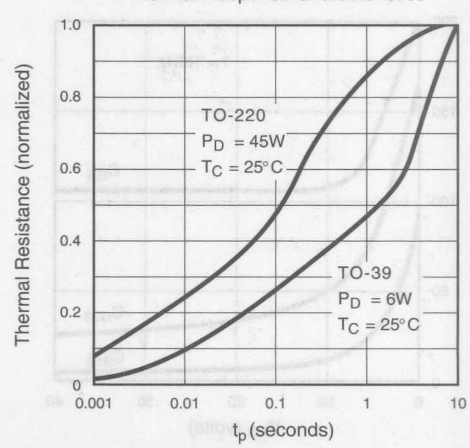
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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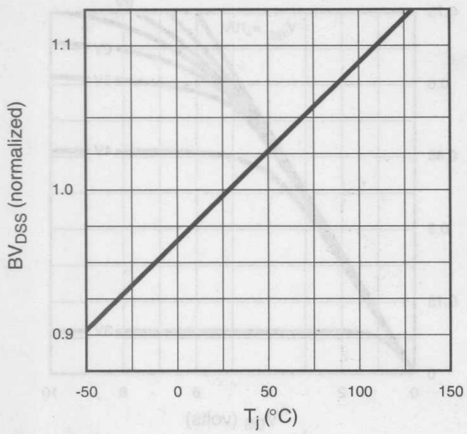
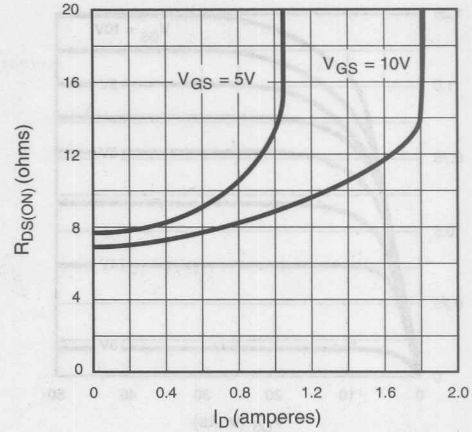
Typical Performance Curves

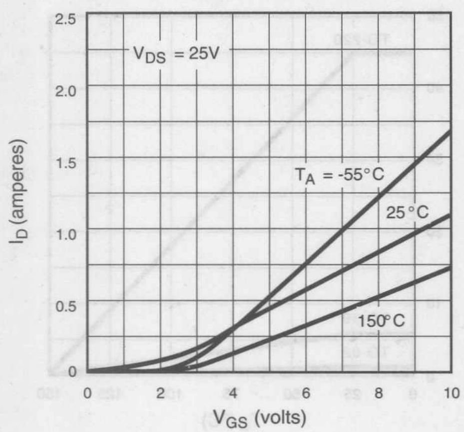
BV$_{DSS}$ Variation with Temperature



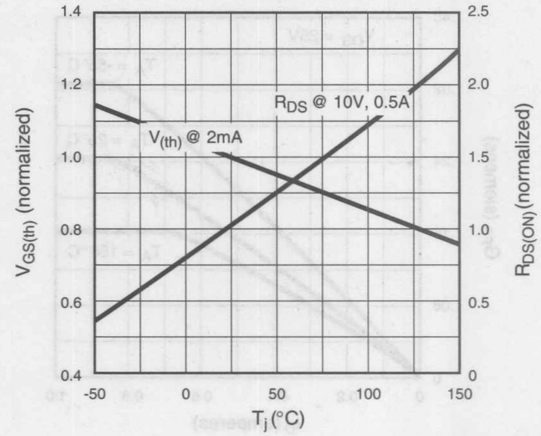
On-Resistance vs. Drain Current



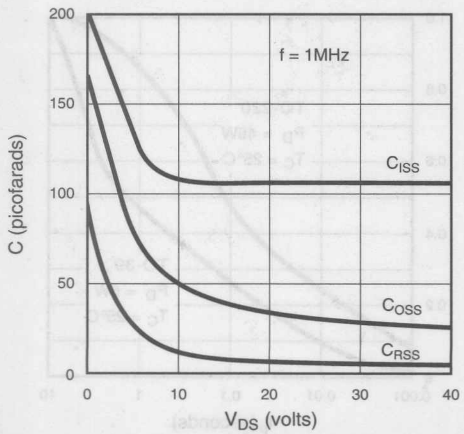
Transfer Characteristics



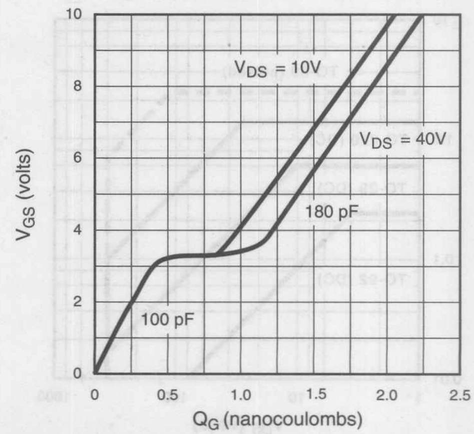
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92	TO-220	Dice†
450V	16Ω	0.5A	VN0645N2	VN0645N3	VN0645N5	VN0645ND
500V	16Ω	0.5A	VN0650N2	VN0650N3	VN0650N5	VN0650ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

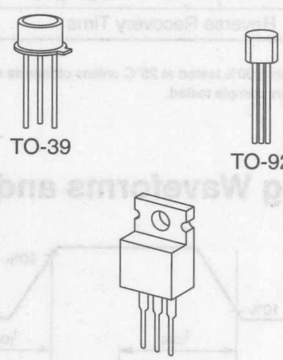
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

TO-92	0.2A	1.0A	1W	170	125	0.2A	1.0A
TO-220	1.0A	1.5A	45W	70	2.7	1.0A	1.5A

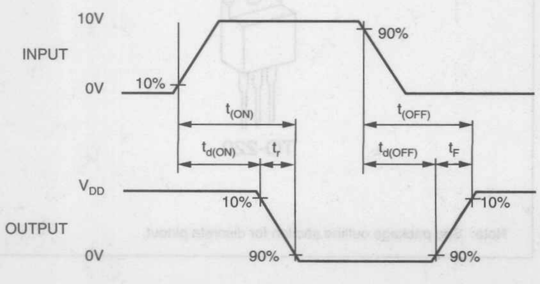
* I_D (continuous) is limited by max rated T_j.

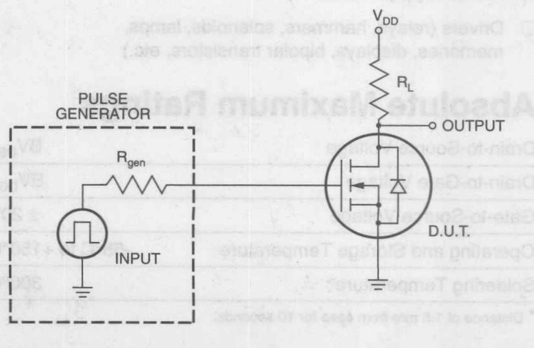
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0645	450			V	$V_{GS} = 0V$, $I_D = 2mA$
		VN0650	500				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}$, $I_D = 2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 2mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			0.8		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			0.5	1.1			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			12		Ω	$V_{GS} = 5V$, $I_D = 100mA$
				11	16		$V_{GS} = 10V$, $I_D = 400mA$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V$, $I_D = 400mA$
G_{FS}	Forward Transconductance		100			m℧	$V_{DS} = 25V$, $I_D = 400mA$
C_{ISS}	Input Capacitance			120	130	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			20	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 0.5A$, $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0V$, $I_{SD} = 0.4A$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0V$, $I_{SD} = 0.4A$

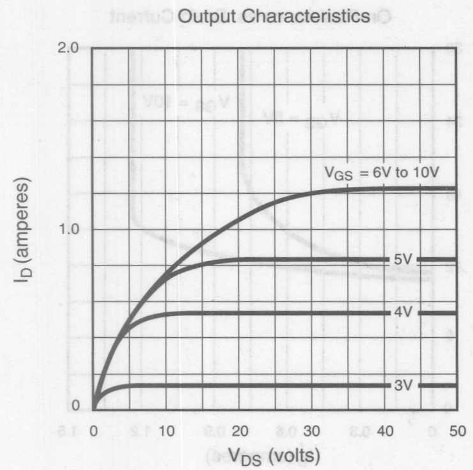
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

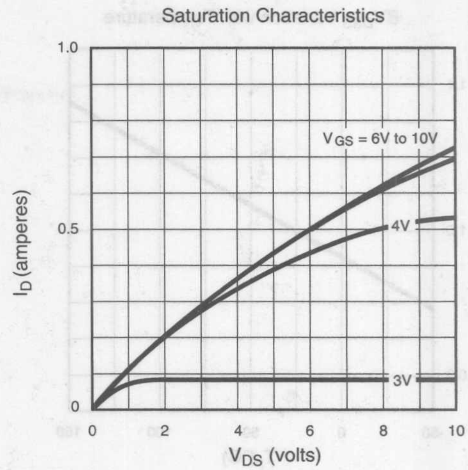
Switching Waveforms and Test Circuit

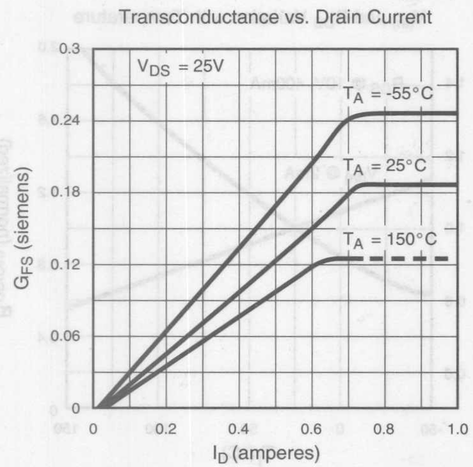


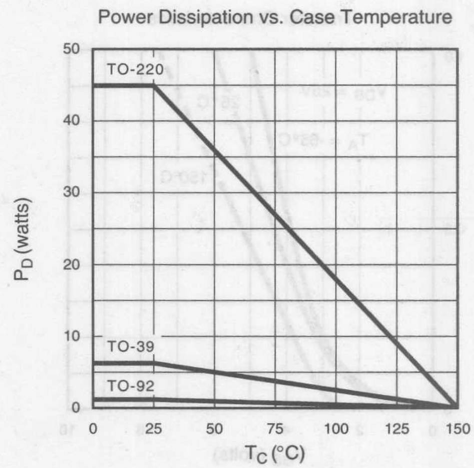


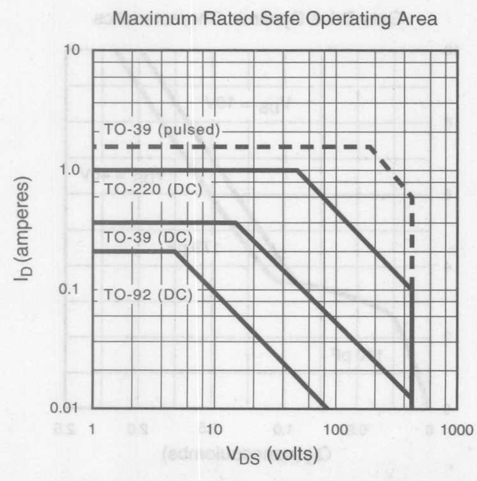
Typical Performance Curves

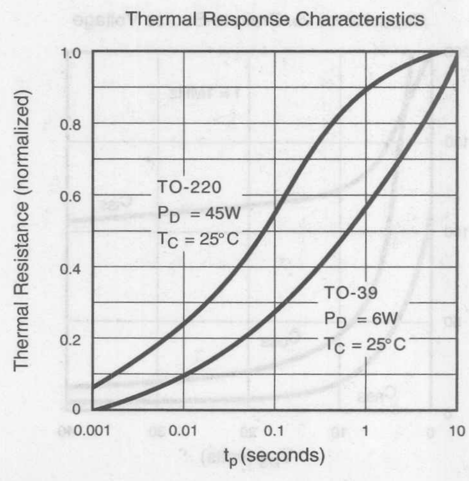






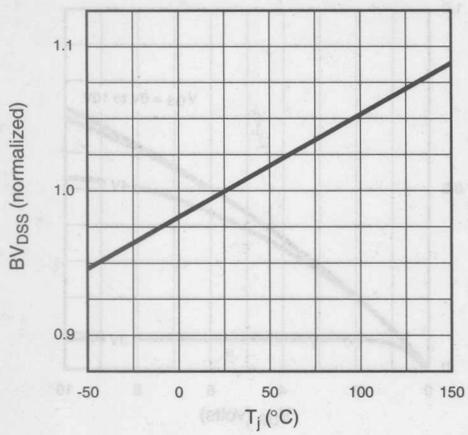




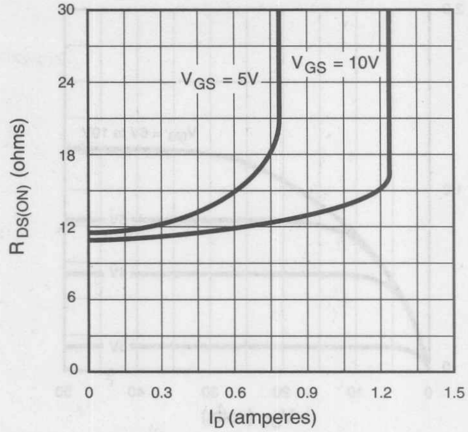


Typical Performance Curves

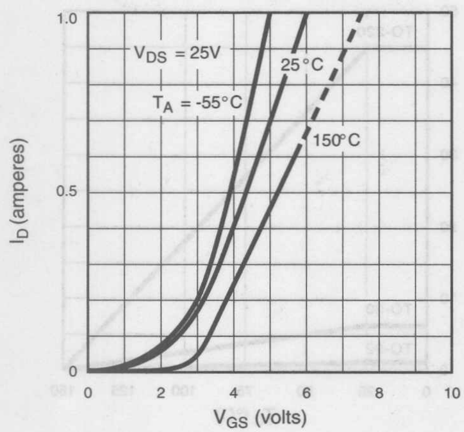
BV_{DSS} Variation with Temperature



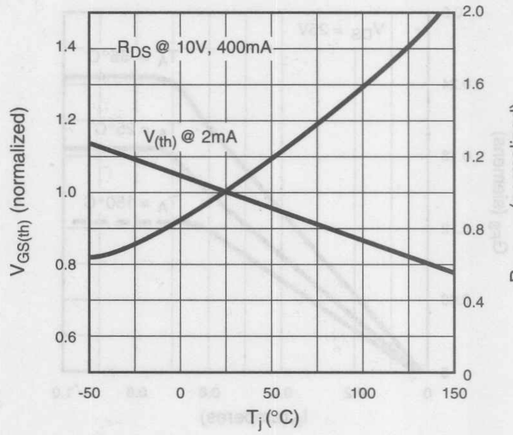
On-Resistance vs. Drain Current



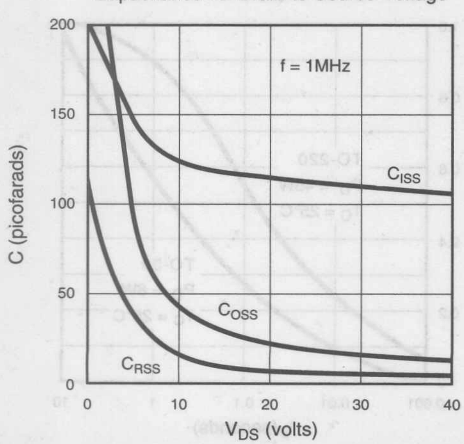
Transfer Characteristics



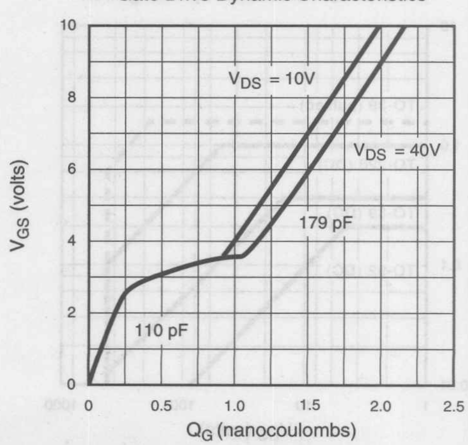
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92	TO-220	Dice†
550V	20Ω	0.25A	VN0655N2	VN0655N3	VN0655N5	VN0655ND
600V	20Ω	0.25A	VN0660N2	VN0660N3	VN0660N5	VN0660ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

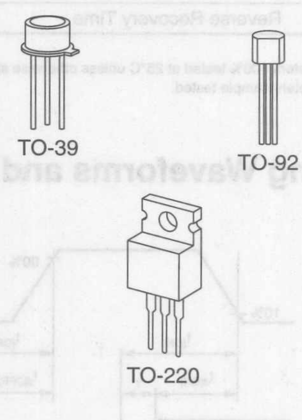
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

8

TO-39	0.35A	1.0A	6W	125	21	0.35A	1.0A
TO-92	0.15A	0.5A	1W	170	125	0.15A	0.5A
TO-220	0.75A	1.5A	45W	70	5	0.75A	1.5A

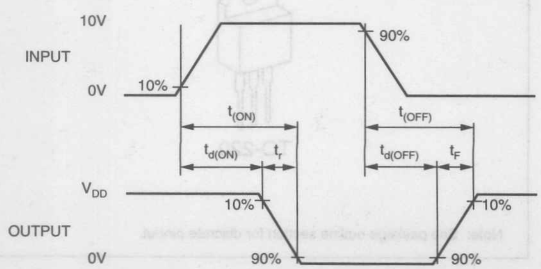
* I_D (continuous) is limited by max rated T_j.

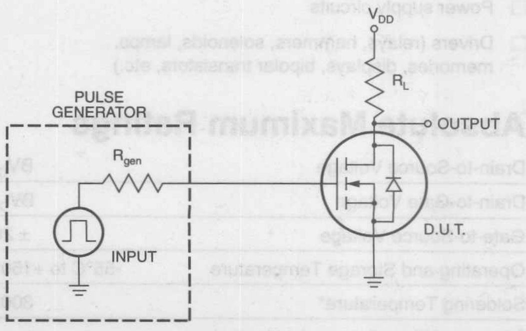
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0655	550			V	$V_{GS} = 0, I_D = 2mA$
		VN0660	600				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}, I_D = 2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	$V_{GS} = V_{DS}, I_D = 2mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0, V_{DS}$ = Max Rating
					1	mA	$V_{GS} = 0, V_{DS}$ = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			0.8		A	$V_{GS} = 5V, V_{DS} = 25V$
			0.25	1.0			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			17		Ω	$V_{GS} = 5V, I_D = 100mA$
				16	20		$V_{GS} = 10V, I_D = 100mA$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature				0.75	%/°C	$V_{GS} = 10V, I_D = 100mA$
G_{FS}	Forward Transconductance		50	75		m℧	$V_{DS} = 25V, I_D = 100mA$
C_{ISS}	Input Capacitance			85	130	pF	$V_{GS} = 0, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = 25V$, $I_D = 0.25A$ $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop				1.8	V	$V_{GS} = 0, I_{SD} = 100mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0, I_{SD} = 100mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

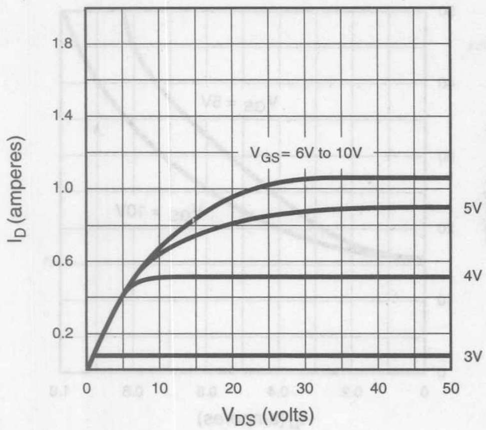
Switching Waveforms and Test Circuit



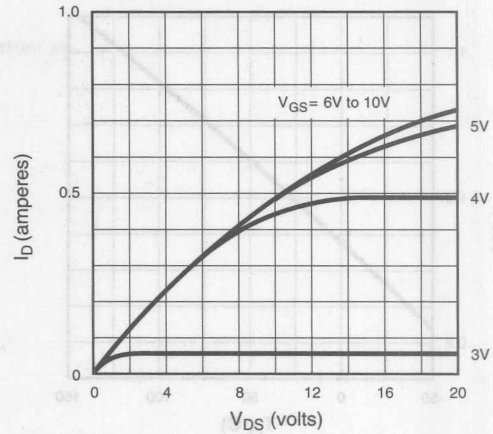


Typical Performance Curves

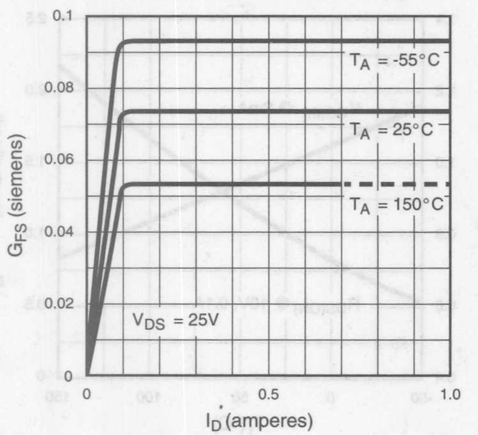
Output Characteristics



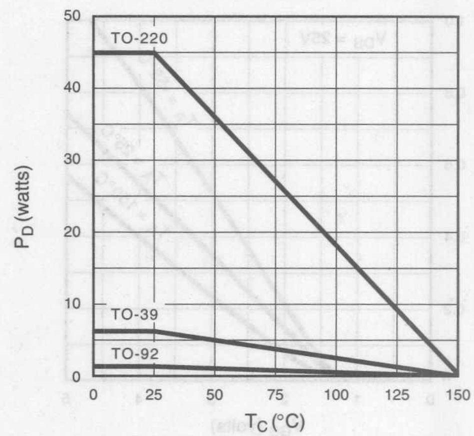
Saturation Characteristics



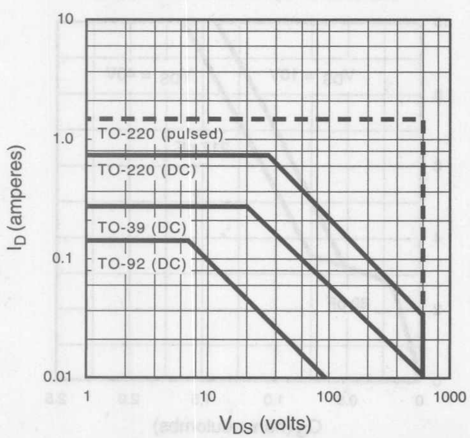
Transconductance vs. Drain Current



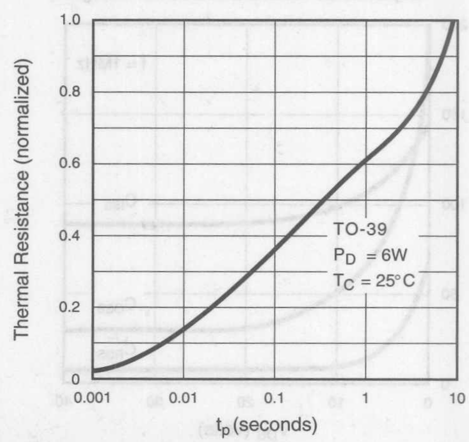
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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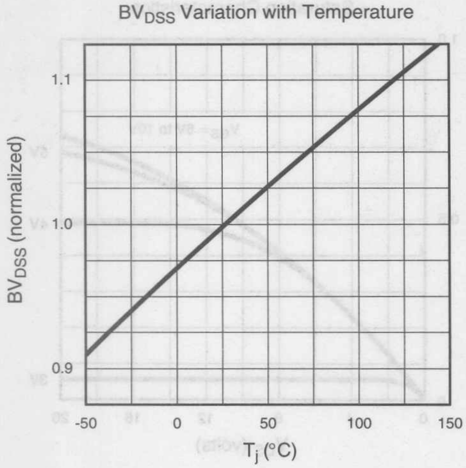
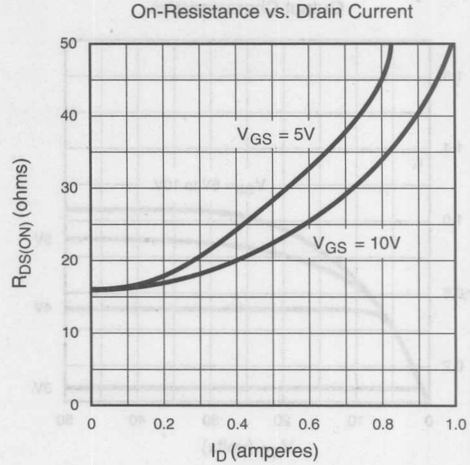
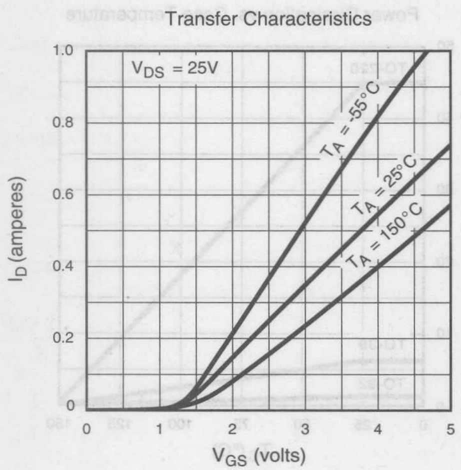
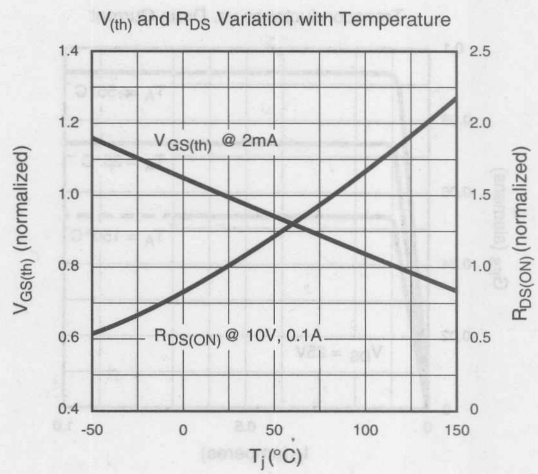
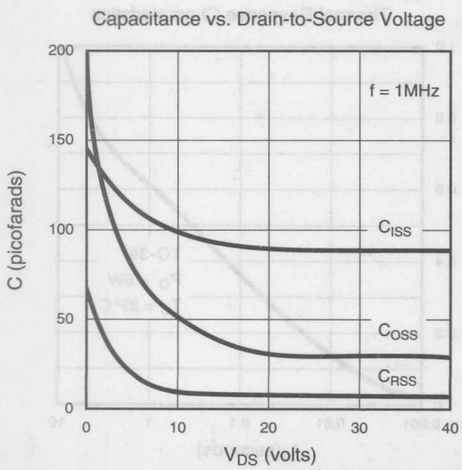
Typical Performance Curves

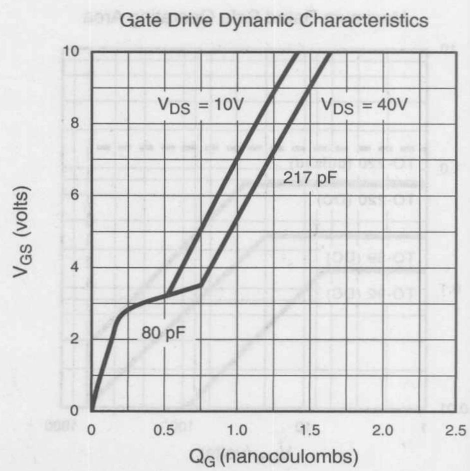












N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92
60V	3Ω	1.5A	VN0606L
60V	5Ω	0.75A	VN0610LL

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

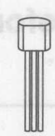
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	0.31A	1A	1W	156	51

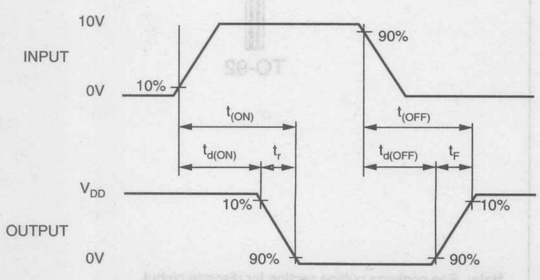
* I_D (continuous) is limited by max rated T_j.

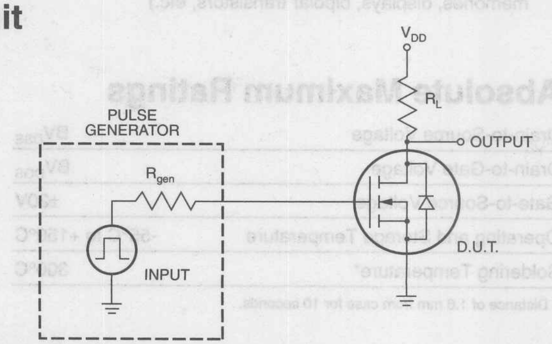
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0610	60			V	$V_{GS} = 0$, $I_D = 100\mu A$
		VN0606	60				$V_{GS} = 0$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	VN0610	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
		VN0606	0.8		2.0		
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0$, $V_{DS} = 50V$
					500		$V_{GS} = 0$, $V_{DS} = 50V$, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	VN0610	0.75			A	$V_{GS} = 10$, $V_{DS} = 10V$
		VN0606	1.5				$V_{GS} = 10$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	VN0610			7.5		$V_{GS} = 5V$, $I_D = 0.2A$
		VN0610			5.0	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
		VN0606			3.0		$V_{GS} = 10V$, $I_D = 1A$
G_{FS}	Forward Transconductance		170			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance				50	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance				25		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{(ON)}$	Turn-ON Time				10	ns	$V_{DD} = 25V$, $I_D = 0.6A$, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time				10		
V_{SD}	Diode Forward Voltage Drop	VN0610		1.2		V	$V_{GS} = 0$, $I_{SD} = 0.47A$
		VN0606		0.85			$V_{GS} = 0$, $I_{SD} = 0.47A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92
80V	4Ω	1.5A	VN0808L

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Advanced DMOS Technology

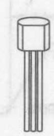
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Package Options



TO-92

Note: See package outline section for discrete pinout.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	.26A	2.0A	1W	125	26.4

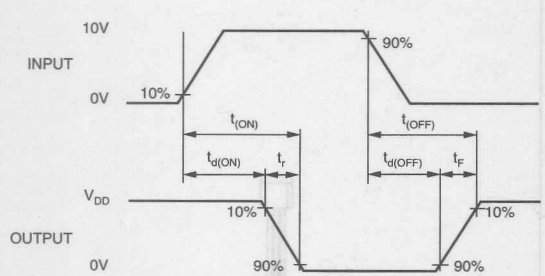
* I_D (continuous) is limited by max rated T_j.

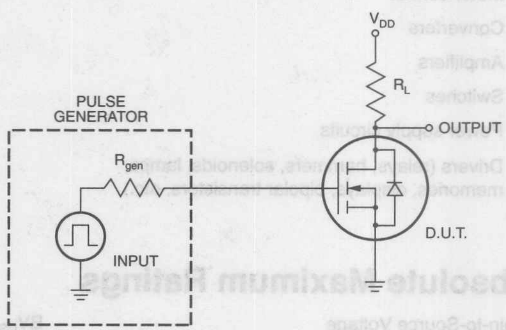
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	80			V	$I_D = 10\mu A, V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}, I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm15V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0, V_{DS} = 80V$
				500		$V_{GS} = 0, V_{DS} = 0.8$ x Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1.5			A	$V_{GS} = 10V, V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4	Ω	$V_{GS} = 10V, I_D = 1A$
G_{FS}	Forward Transconductance	170			m℧	$V_{DS} = 10V, I_D = 0.5A$
C_{ISS}	Input Capacitance			50	pF	$V_{GS} = 0V, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			40		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 25V, I_D = 1A$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.85		V	$I_{SD} = 0.35A, V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-52	TO-92
60V	5Ω	0.75A	VN10KN9	VN10KN3

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- TTL/CMOS compatibility
- Low input capacitance
- Fast switching speeds
- Reliable TO-92 package compatible with auto-insertion
- Complements VP01A P-channel devices

Applications

- Inductive load driver
- Display driver
- Line driver
- Analog switch
- Alternative to VN0106N3

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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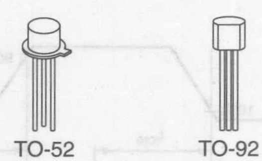
Package Options



Note: See package outline section for discrete pinout.

TO-52	0.3A	1.0A	1.0W	170	125	1.5A	1.0A
TO-92	0.3A	1.0A	1.0W	170	125	1.5A	1.0A

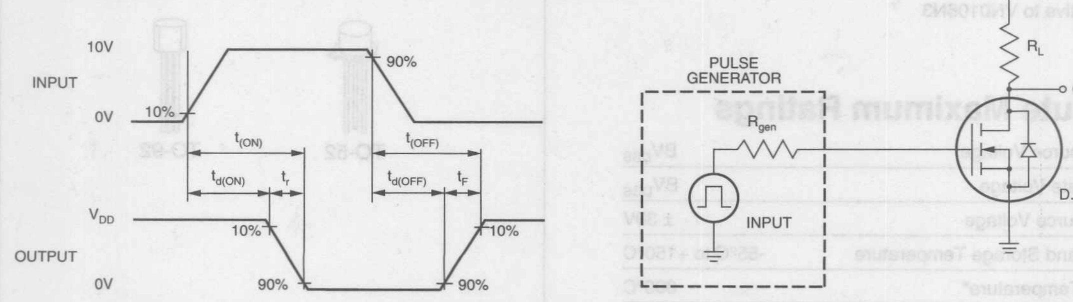
Notes:
1. I_D (continuous) is limited by max rated T_j.
2. VN0106N3 can be used if an I_D (continuous) of 0.5 is needed.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage — VN10K	60			V	$V_{GS} = 0V$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8		mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0V$, $V_{DS} = 48V$
				500	µA	$V_{GS} = 0V$, $V_{DS} = 48V$, T_A 125°C
$I_{D(ON)}$	ON-State Drain Current	0.75			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	$V_{GS} = 5V$, $I_D = 0.2A$
				5.0	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature		0.7		%/°C	$V_{GS} = 10V$, $I_D = 500mA$,
G_{FS}	Forward Transconductance	100			m℧	$V_{DS} = 10V$, $I_D = 500mA$
C_{ISS}	Input Capacitance		48	60	pF	$V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance		16	25	pF	$V_{DS} = 25V$, f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance		2	5	pF	$V_{DS} = 25V$, f = 1 MHz
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 15V$, $I_D = 0.6A$, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10	ns	$V_{DD} = 15V$, $I_D = 0.6A$, $R_{GEN} = 25\Omega$
V_{SD}	Diode Forward Voltage Drop		0.8		V	$V_{GS} = 0V$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time		160		ns	$V_{GS} = 0$, $I_{SD} = 0.5A$

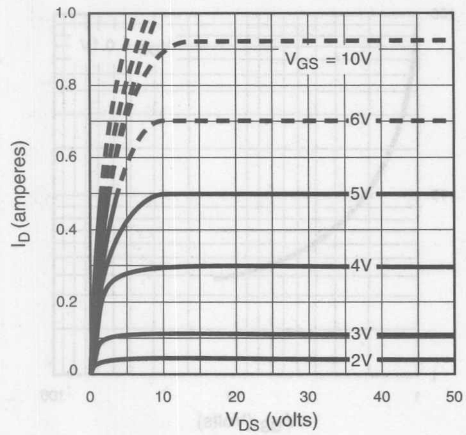
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

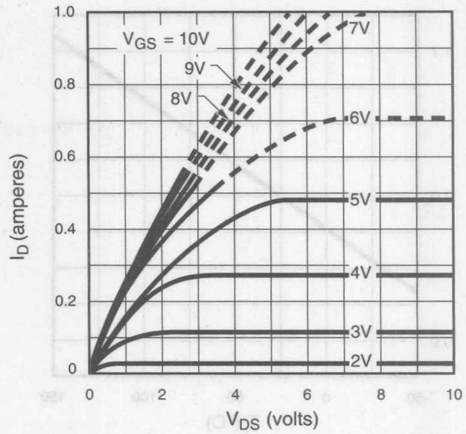


Typical Performance Curves

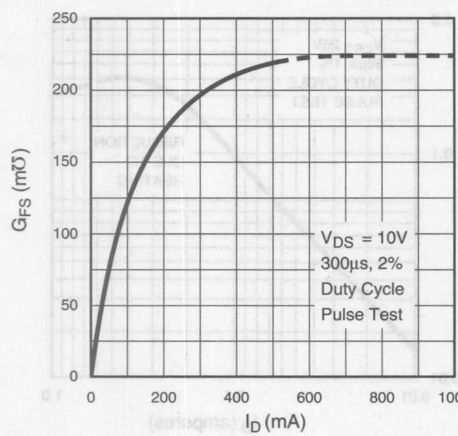
Output Characteristics



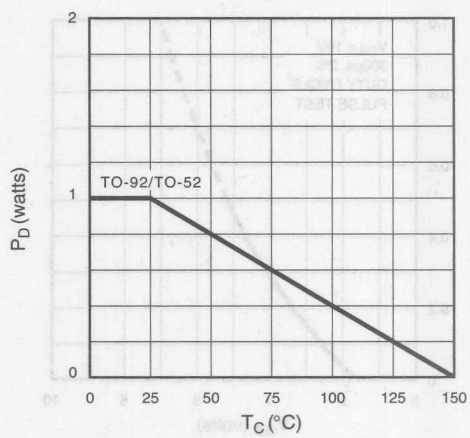
Saturation Characteristics



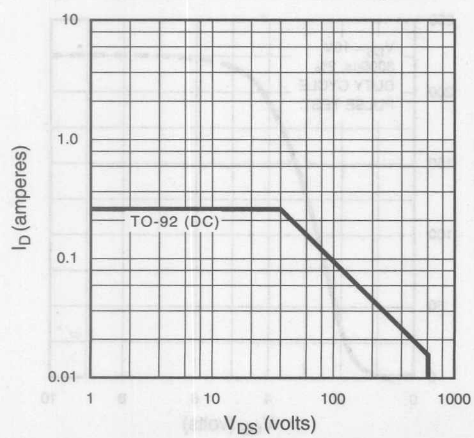
Transconductance vs. Drain Current



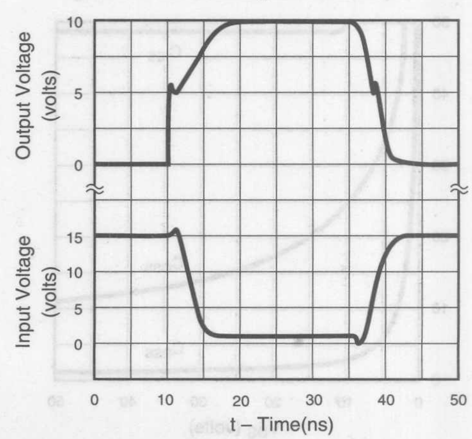
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

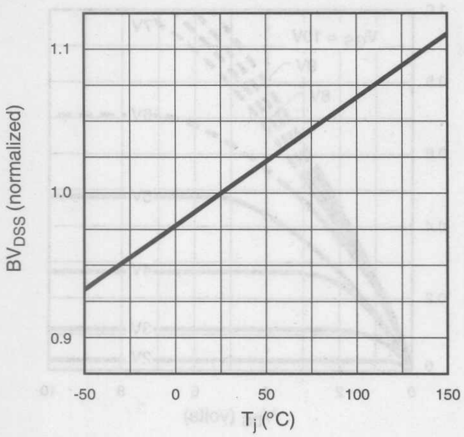


Switching Waveform

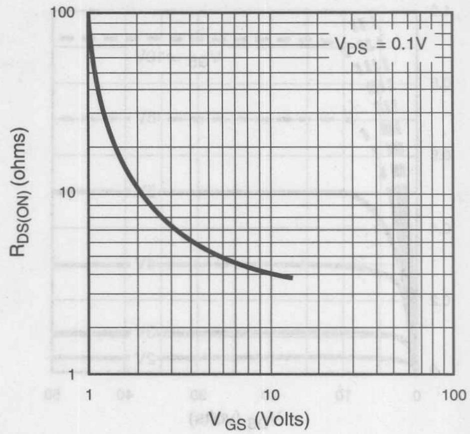


Typical Performance Curves

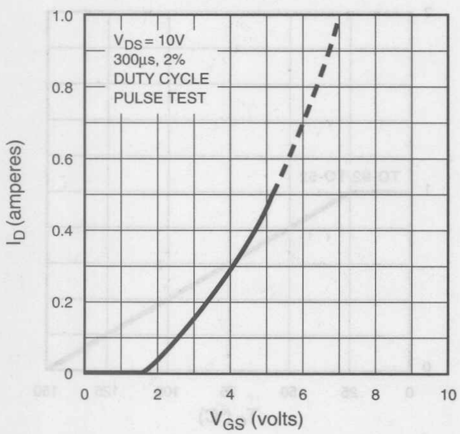
BV_{DSS} Variation with Temperature



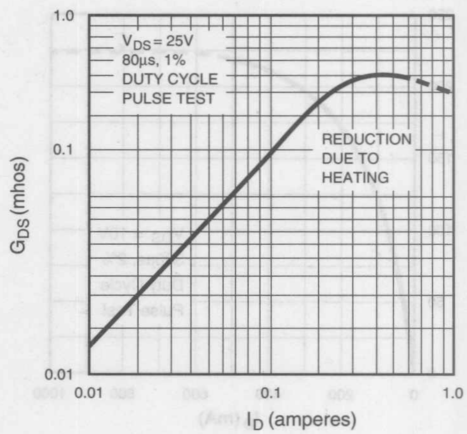
On-Resistance vs. Gate-to-Source Voltage



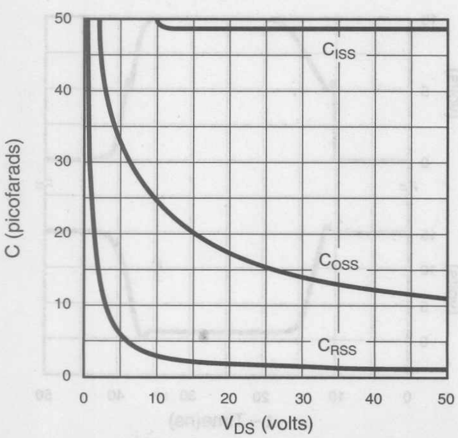
Transfer Characteristics



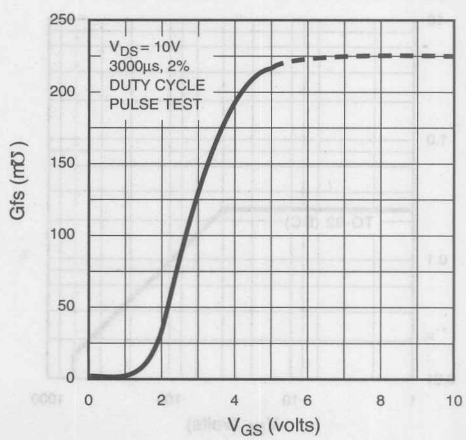
Output Conductance vs Drain Current



Capacitance vs. Drain-to-Source Voltage



Transconductance vs Gate-Source Voltage



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-220	Dice†
60V	0.7Ω	8.0A	VN1106N2	VN1106N5	VN1106ND
100V	0.7Ω	8.0A	VN1110N2	VN1110N5	VN1110ND

†MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

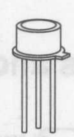
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

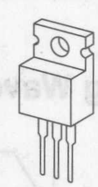
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39



TO-220

Note: See package outline section for discrete pinout.

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TO-39	2.5A	6A	6W	125	20.8	2.5A	6A
TO-220	7.0A	18A	45W	70	2.7	7.0A	18A

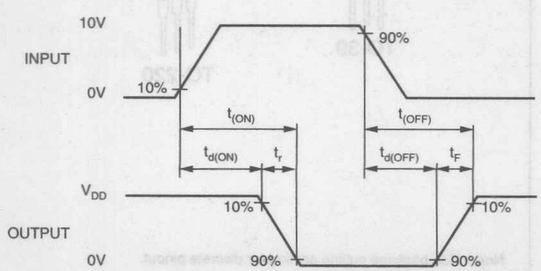
* I_D (continuous) is limited by max rated T_j.

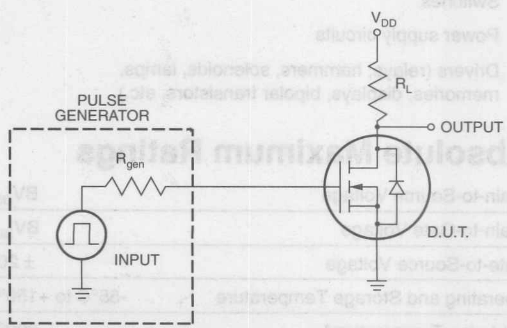
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1110	100			V	V_{GS} = 0V, I_D = 5mA
		VN1106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}$, I_D = 2mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4	-6	mV/°C	$V_{GS} = V_{DS}$, I_D = 2mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				50	µA	V_{GS} = 0V, V_{DS} = Max Rating
					1	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		3	5		A	V_{GS} = 5V, V_{DS} = 25V
			8	18			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.7	1.0	Ω	V_{GS} = 5V, I_D = 3A
				0.4	0.7		V_{GS} = 10V, I_D = 5A
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			0.3	0.8	%/°C	V_{GS} = 10V, I_D = 5A
G_{FS}	Forward Transconductance		1	2		℧	V_{DS} = 25V, I_D = 3A
C_{ISS}	Input Capacitance			240	350	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			150	200		
C_{RSS}	Reverse Transfer Capacitance			16	25		
$t_{d(ON)}$	Turn-ON Delay Time			10	45	ns	V_{DD} = 25V, I_D = 3A, R_{GEN} = 10Ω
t_r	Rise Time			5	14		
$t_{d(OFF)}$	Turn-OFF Delay Time			35	45		
t_f	Fall Time			20	35		
V_{SD}	Diode Forward Voltage Drop			1.2	1.6	V	V_{GS} = 0V, I_{SD} = 1A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0V, I_{SD} = 1A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

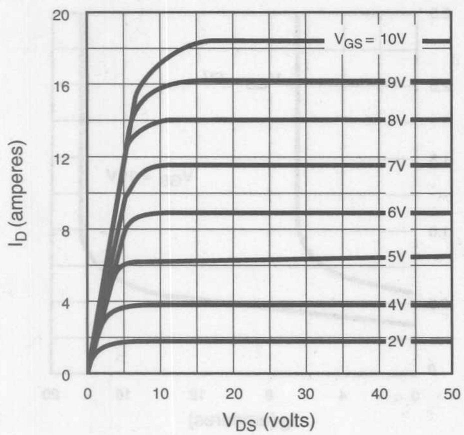
Switching Waveforms and Test Circuit



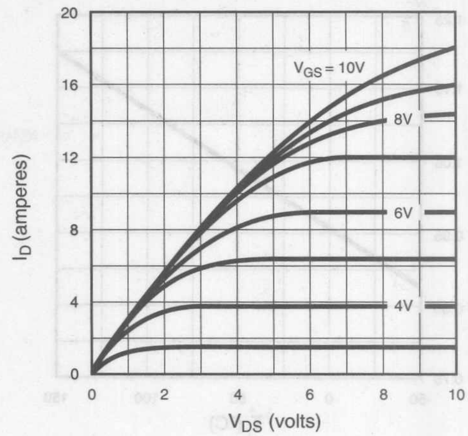


Typical Performance Curves

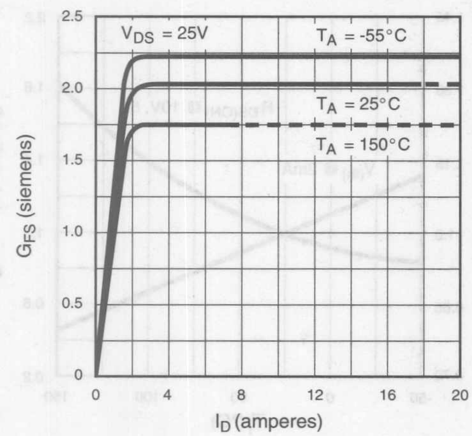
Output Characteristics



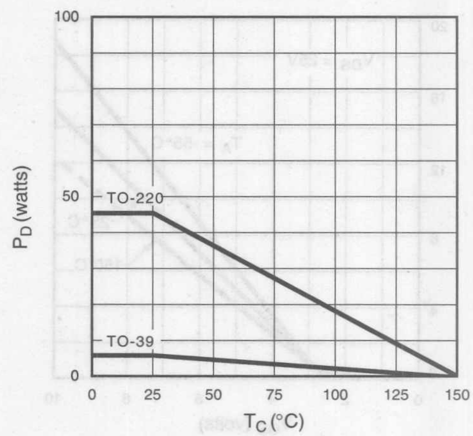
Saturation Characteristics



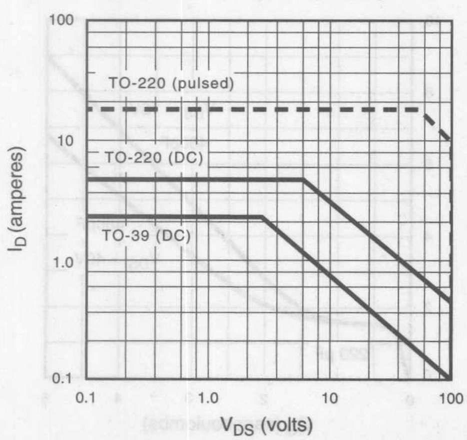
Transconductance vs. Drain Current



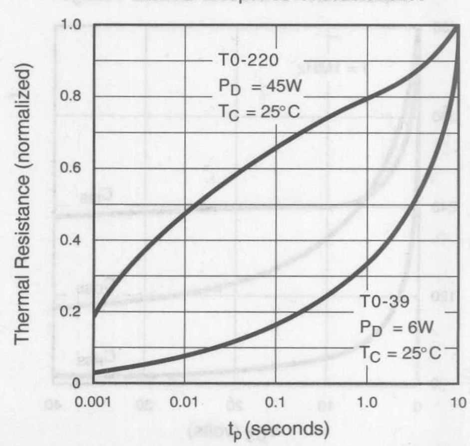
Power Dissipation vs. Case Temperature



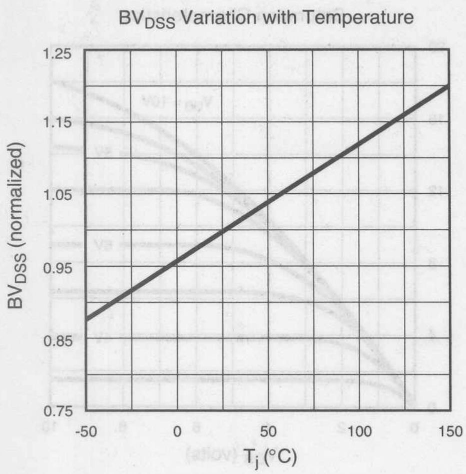
Maximum Rated Safe Operating Area

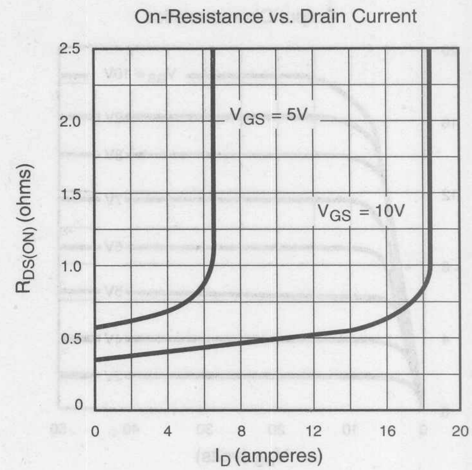


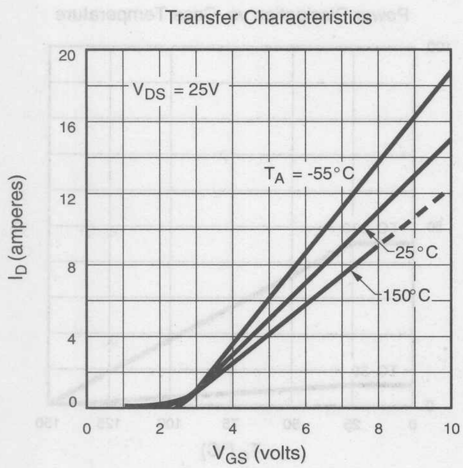
Thermal Response Characteristics

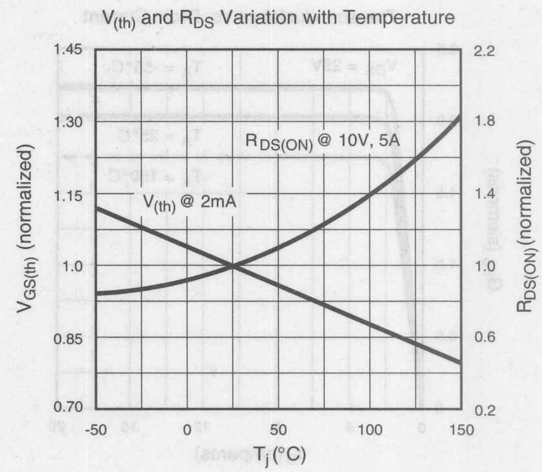


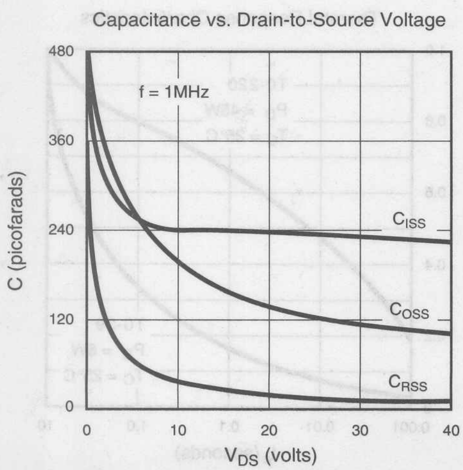
Typical Performance Curves

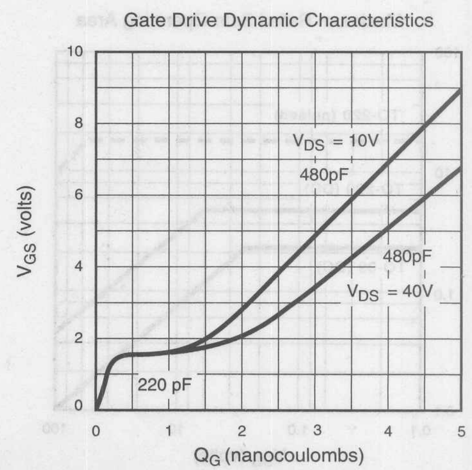












N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-220	Dice†
40V	0.3Ω	20A	VN1204N2	VN1204N5	VN1204ND
60V	0.3Ω	20A	VN1206N2	VN1206N5	VN1206ND
100V	0.3Ω	20A	VN1210N2	VN1210N5	VN1210ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

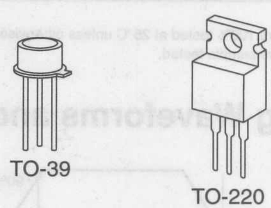
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	3.5A	15A	6.5W	125	20	3.5A	15A
TO-220	9A	35A	45W	70	2.75	9A	35A

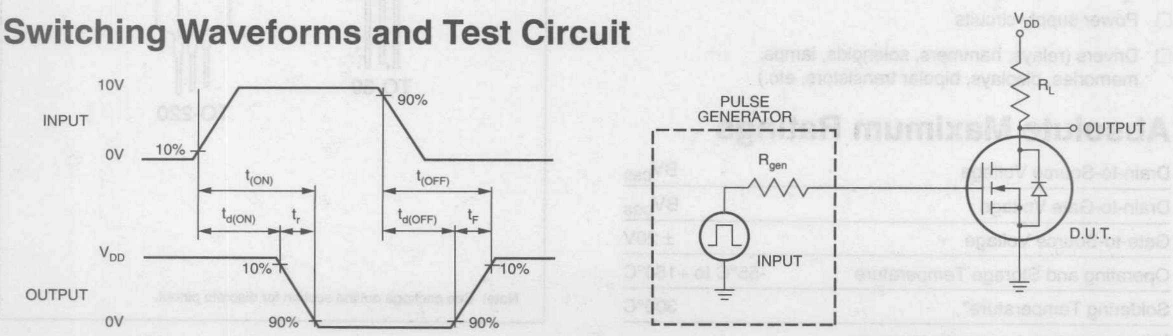
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1210	100			V	$V_{GS} = 0$, $I_D = 10mA$
		VN1206	60				
		VN1204	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.3	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 10mA$
I_{GSS}	Gate Body Leakage			1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	$V_{GS} = 0$, V_{DS} = Max Rating
					10	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		5	12		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			20	36			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.22	0.45	Ω	$V_{GS} = 5V$, $I_D = 2A$
				0.2	0.3		$V_{GS} = 10V$, $I_D = 10A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	$V_{GS} = 10V$, $I_D = 10A$
G_{FS}	Forward Transconductance		4.0			℧	$V_{DS} = 25V$, $I_D = 5A$
C_{ISS}	Input Capacitance			700	850	pF	$V_{GS} = 0$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			300	350		
C_{RSS}	Reverse Transfer Capacitance			45	75		
$t_{d(ON)}$	Turn-ON Delay Time			8	20	ns	$V_{DD} = 25V$ $I_D = 5A$ $R_{GEN} = 10\Omega$
t_r	Rise Time			8	30		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	90		
t_f	Fall Time			40	60		
V_{SD}	Diode Forward Voltage Drop			1.2	1.4	V	$V_{GS} = 0$, $I_{SD} = 10A$
t_{rr}	Reverse Recovery Time			500		ns	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Typical Performance Curves

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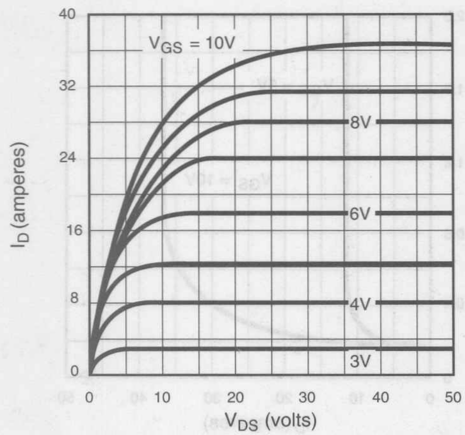
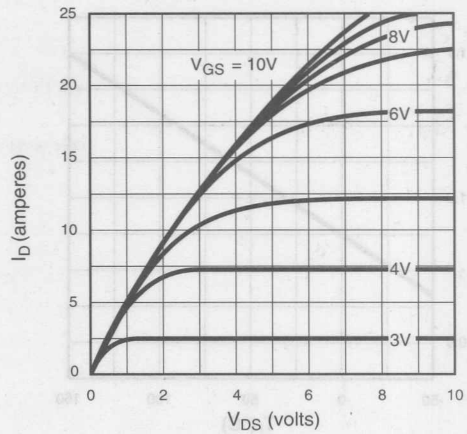
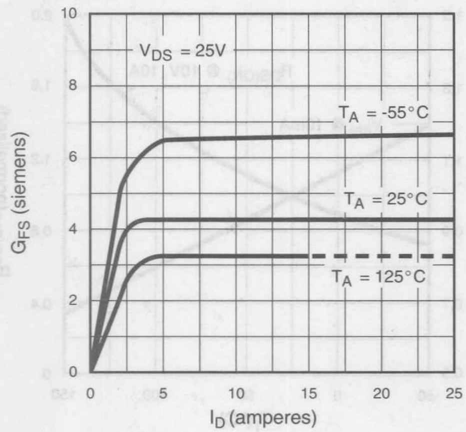
Output Characteristics



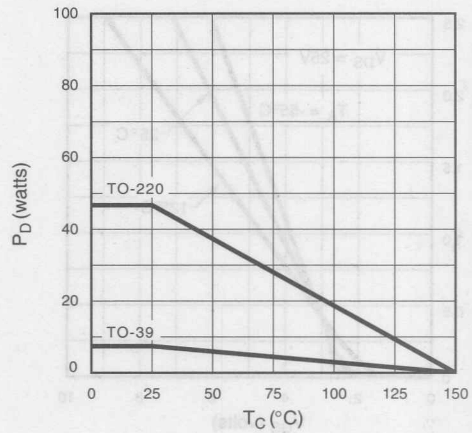
Saturation Characteristics



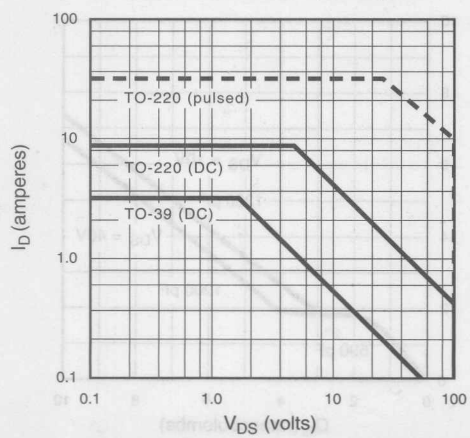
Transconductance vs. Drain Current



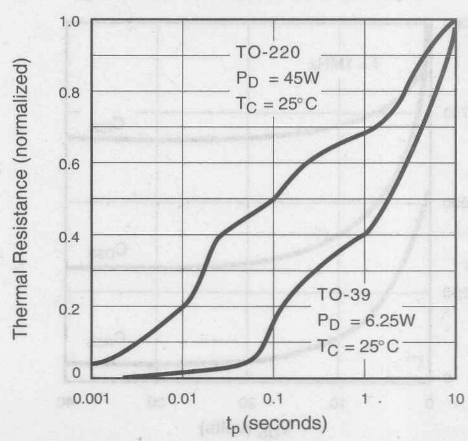
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

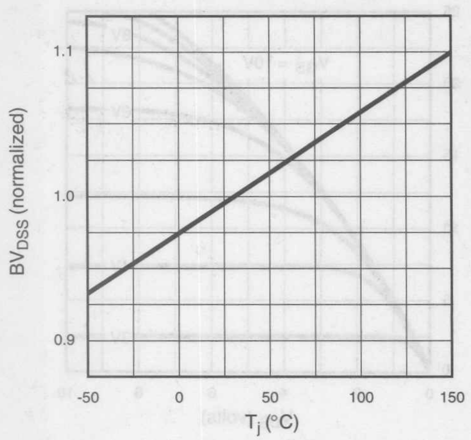


Thermal Response Characteristics

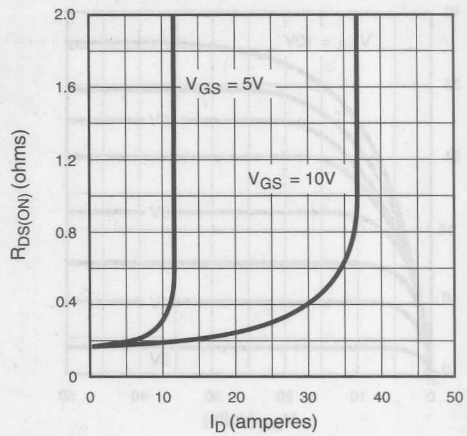


Typical Performance Curves

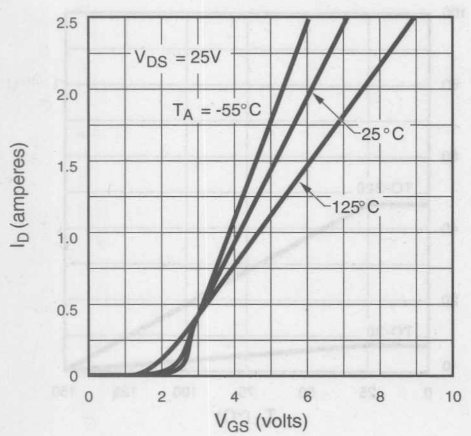
BV_{DSS} Variation with Temperature



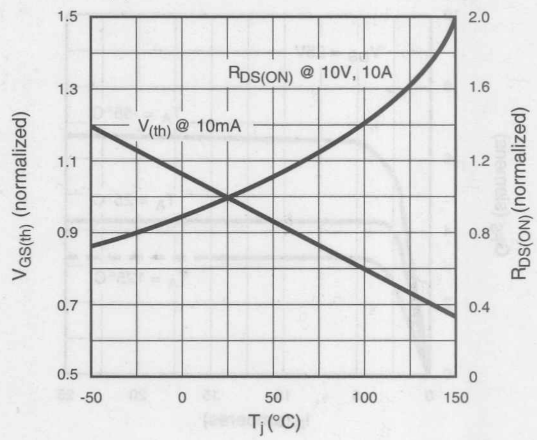
On-Resistance vs. Drain Current



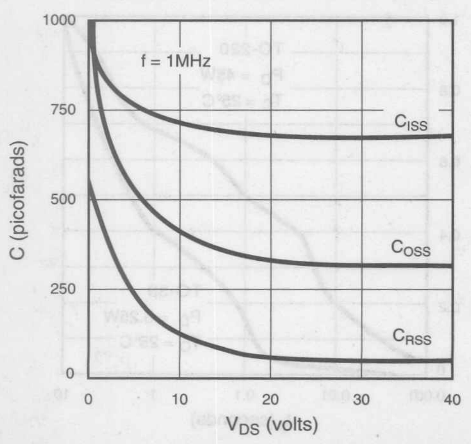
Transfer Characteristics



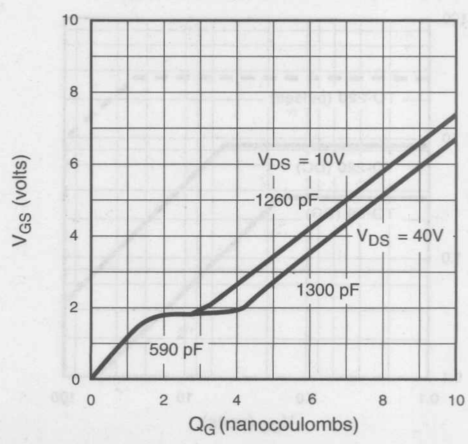
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
120V	6Ω	1.0A	VN1206B	VN1206L	VN1206D
120V	10Ω	1.0A	—	VN1210L	—

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

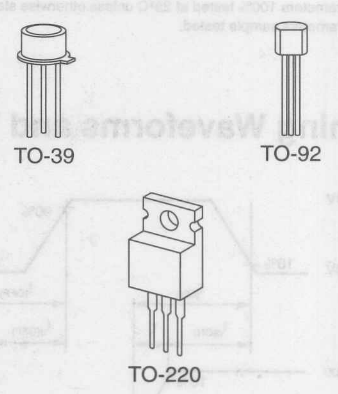
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	0.59A	2.5A	5W	170	25
TO-92	0.18A	2.0A	0.8W	156	21.3
TO-220	1.19A	2.5A	20W	80	6.25

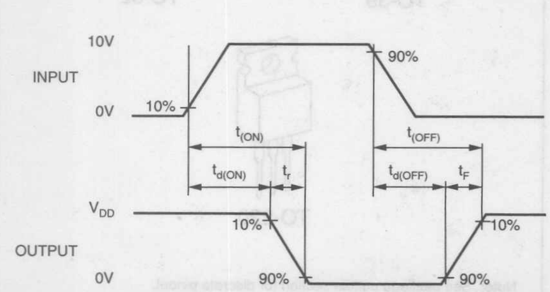
* I_D (continuous) is limited by max rated T_j.

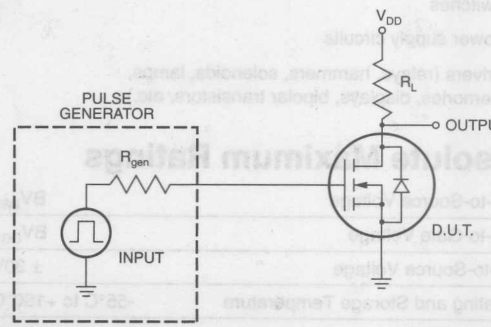
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	120			V	$V_{GS} = 0$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0$, V_{DS} = Max Rating
				500	µA	$V_{GS} = 0$, V_{DS} = Max Rating, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1.0			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance — ALL			10	Ω	$V_{GS} = 2.5V$, $I_D = 0.1A$
	VN1206			6	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
	VN1210			10	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance	300			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			125	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance			20	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
t_r	Rise Time			8	ns	$V_{DD} = 60V$, $I_D = 0.4A$, $R_{GEN} = 25\Omega$
$t_{d(ON)}$	Turn-ON Delay Time			8	ns	$V_{DD} = 60V$, $I_D = 0.4A$, $R_{GEN} = 25\Omega$
t_f	Fall Time			12	ns	$V_{DD} = 60V$, $I_D = 0.4A$, $R_{GEN} = 25\Omega$
$t_{d(OFF)}$	Turn-OFF Delay Time			18	ns	$V_{DD} = 60V$, $I_D = 0.4A$, $R_{GEN} = 25\Omega$
V_{SD}	Diode Forward Voltage Drop — VN1210		1.2		V	$I_{SD} = 0.12A$, $V_{GS} = 0$
	VN1206		1.2		V	$I_{SD} = 0.25A$, $V_{GS} = 0$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
40V	8Ω	0.5A	VN1304N2	VN1304N3
60V	8Ω	0.5A	VN1306N2	VN1306N3
100V	8Ω	0.5A	VN1310N2	VN1310N3

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

TO-39 TO-92

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	0.4A	1.4A	3.0W	125	41.5	0.4A	1.4A
TO-92	0.25A	1.3A	1.0W	170	125	0.25A	1.3A

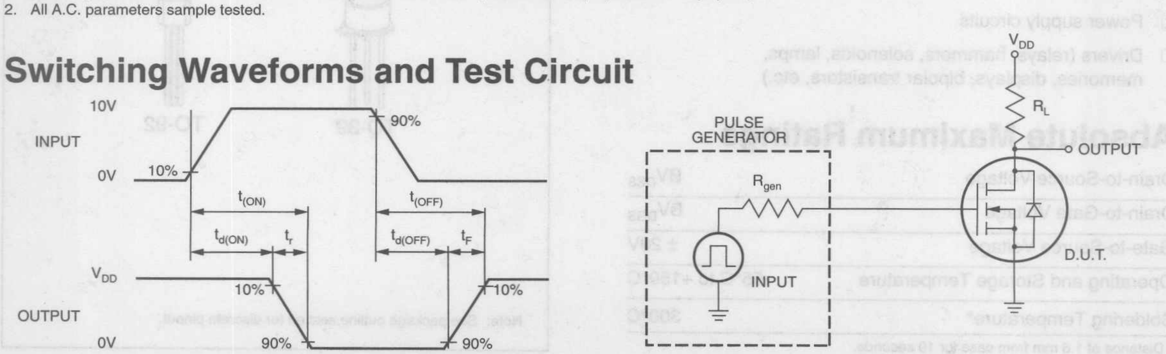
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1310	100			V	$V_{GS} = 0V$, $I_D = 1mA$
		VN1306	60				
		VN1304	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.9	-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					100	µA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.25	0.6		A	$V_{GS} = 5V$, $V_{DS} = 25V$
			0.50	1.4			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	15	Ω	$V_{GS} = 5V$, $I_D = 50mA$
				5	8		$V_{GS} = 10V$, $I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	2	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		120			℧	$V_{DS} = 25V$, $I_D = 500mA$
C_{ISS}	Input Capacitance			27	35	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			13	15		
C_{RSS}	Reverse Transfer Capacitance			3	5		
$t_{d(ON)}$	Turn-ON Delay Time			2	5	ns	$V_{DD} = 25V$ $I_D = 250mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time			2	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			2	6		
t_f	Fall Time			2	5		
V_{SD}	Diode Forward Voltage Drop			1.0	1.3	V	$V_{GS} = 0V$, $I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			350		ns	$V_{GS} = 0V$, $I_{SD} = 1.0A$

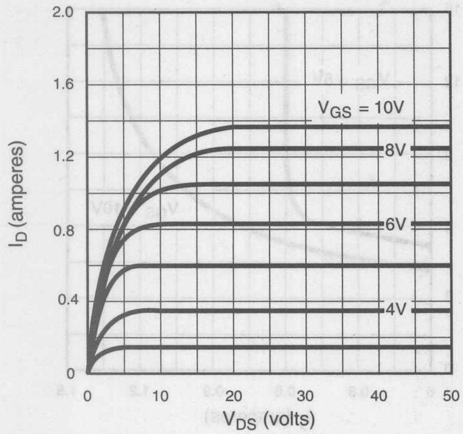
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

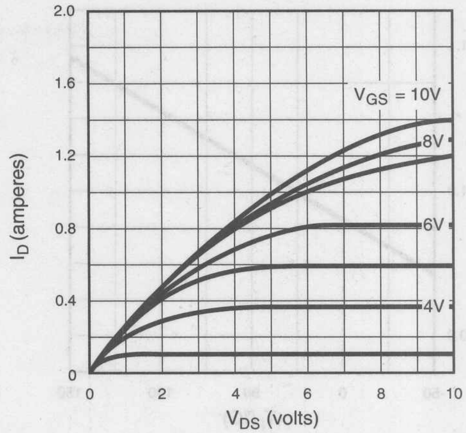


Typical Performance Curves

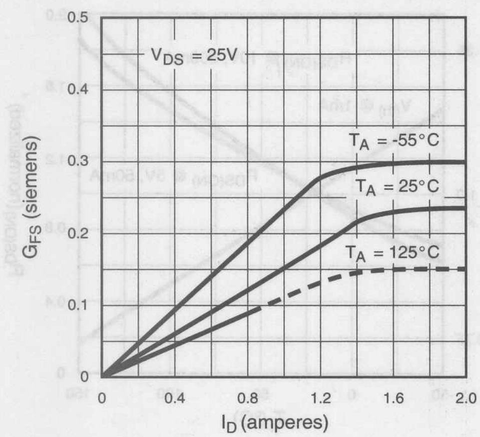
Output Characteristics



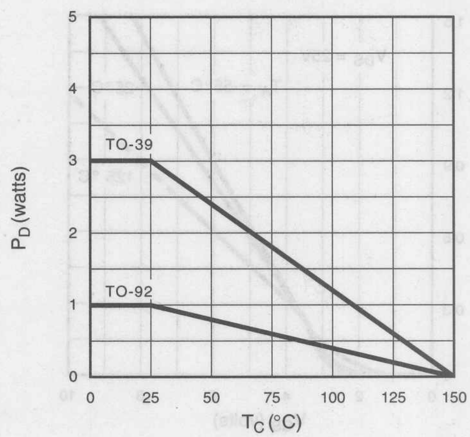
Saturation Characteristics



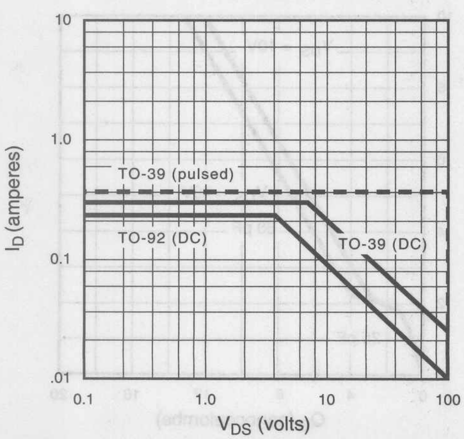
Transconductance vs. Drain Current



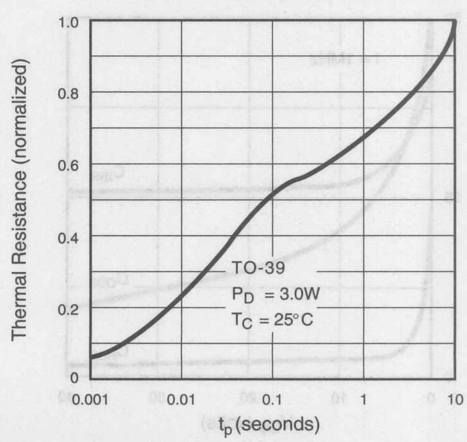
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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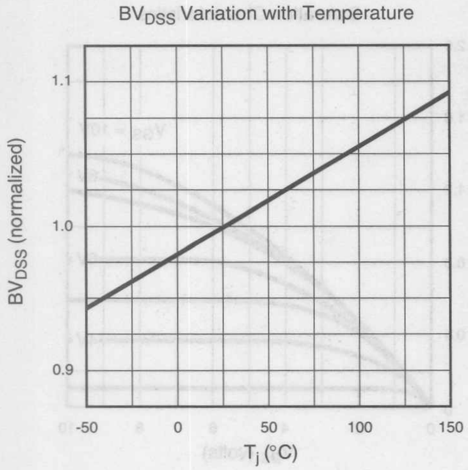
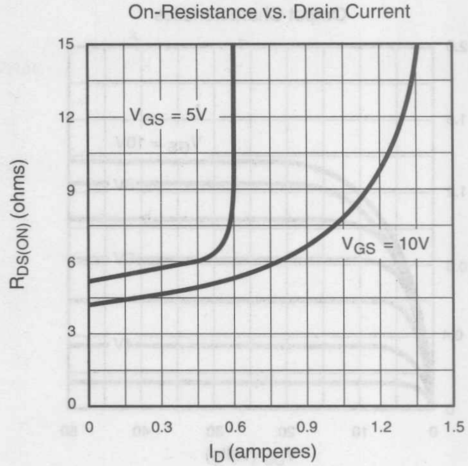
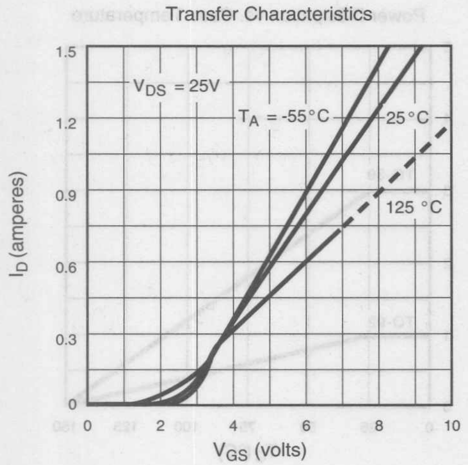
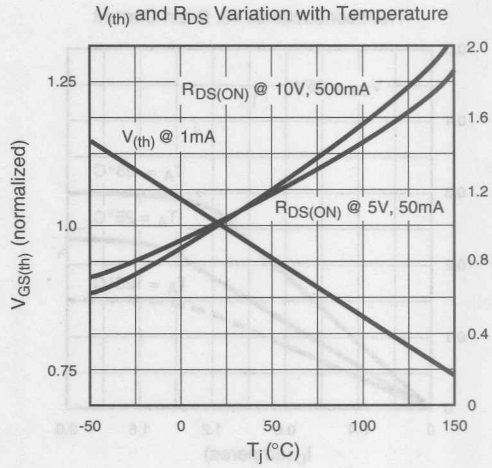
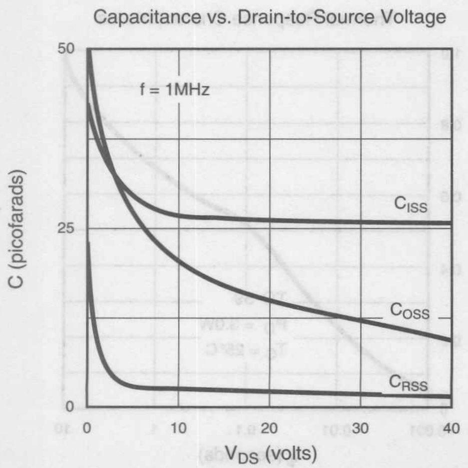
Typical Performance Curves

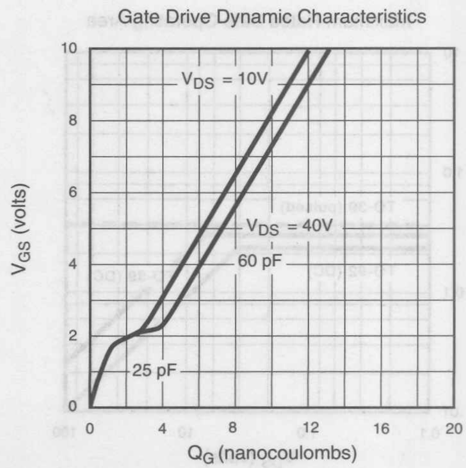












N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
170V	6Ω	1.0A	VN1706B	VN1706L	VN1706D
170V	10Ω	1.0A	—	VN1710L	—

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

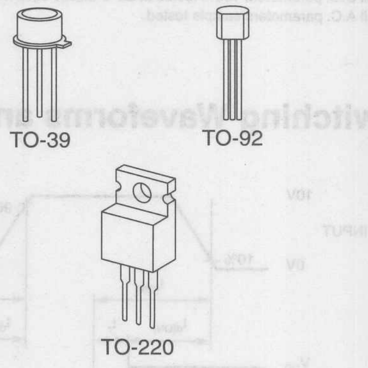
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	0.63A	3.0A	6.25W	170	20
TO-92	0.22A	2.3A	0.8W	156	21.3
TO-220	1.12A	3.0A	20W	80	6.25

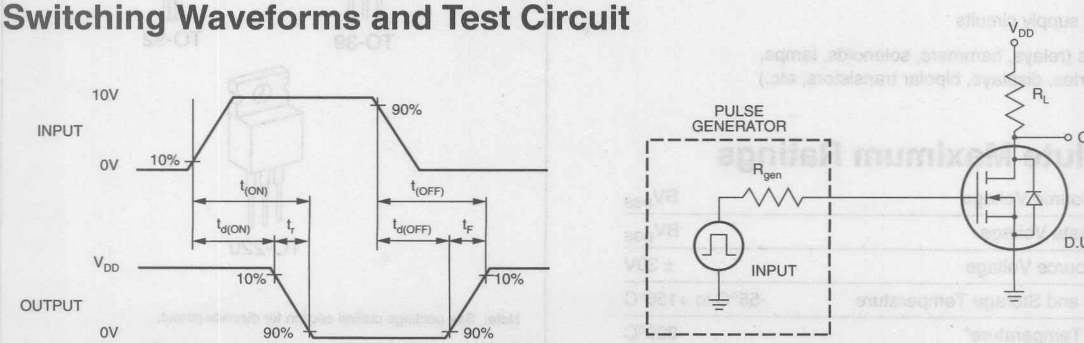
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage		170			V	$V_{GS} = 0V$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	$V_{GS} = 0V$, $V_{DS} = 120V$
					500		$V_{GS} = 0V$, $V_{DS} = 120V$, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		1.0			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	ALL			10	Ω	$V_{GS} = 2.5V$, $I_D = 0.1A$
		VN1710			10	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
		VN1706			6	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance		300			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance				125	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				50	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance				20	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
t_r	Rise Time				8	ns	$V_{DD} = 60V$, $I_D = 0.1A$, $R_{GEN} = 25\Omega$
$t_{d(ON)}$	Turn-ON Delay Time				8	ns	$V_{DD} = 60V$, $I_D = 0.1A$, $R_{GEN} = 25\Omega$
t_f	Fall Time				9	ns	$V_{DD} = 60V$, $I_D = 0.1A$, $R_{GEN} = 25\Omega$
$t_{d(OFF)}$	Turn-OFF Delay Time				13	ns	$V_{DD} = 60V$, $I_D = 0.1A$, $R_{GEN} = 25\Omega$
V_{SD}	Diode Forward Voltage Drop	VN1710		1.2		V	$I_{SD} = 0.19A$, $V_{GS} = 0V$
		VN1706		1.2		V	$I_{SD} = 1.4A$, $V_{GS} = 0V$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package TO-92
200V	10Ω	2.0V	VN2010L

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)
- ☐ Telecom switching

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

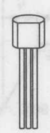
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	250mA	1.0A	1W	170	125	250mA	1.0A

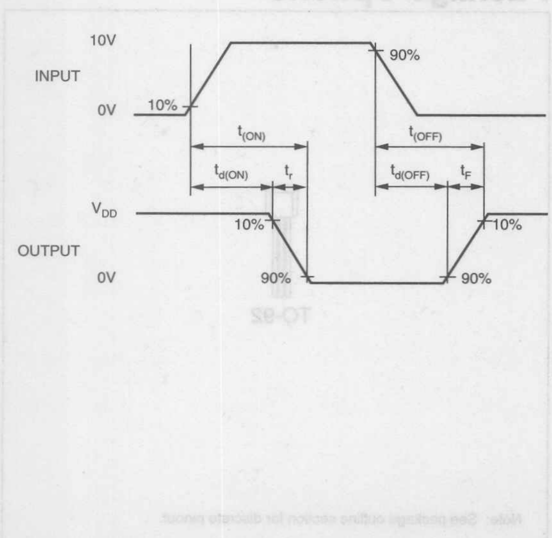
* I_D (continuous) is limited by max rated T_j.

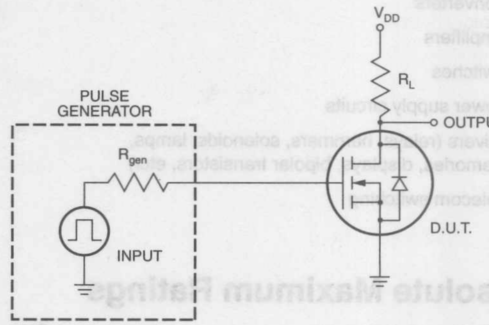
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200			V	$V_{GS} = 0V$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			10	nA	$V_{GS} = \pm 25V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			1.0		$V_{GS} = 0V$, $V_{DS} = 160V$
				100	µA	$V_{GS} = 0V$, $V_{DS} = 160V$, $T_A = 125°C$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10	Ω	$V_{GS} = 4.5V$, $I_D = 50mA$
$I_{D(ON)}$	ON-State Drain Current	100			mA	$V_{GS} = 10V$, $V_{DS} = 10V$
G_{FS}	Forward Transconductance	125			m℧	$V_{DS} = 15V$, $I_D = 0.1A$
C_{ISS}	Input Capacitance			60	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30		
C_{RSS}	Reverse Transfer Capacitance			15		
$t_{(ON)}$	Turn-ON Time			20	ns	$V_{DD} = 25V$, $I_D = 0.1A$, $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS} = 0V$, $I_{SD} = 250mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package		
		TO-92	20 Terminal Ceramic LCC	Die[†]
60V	4Ω	VN2106N3	VN2106NF	VN2106ND
100V	4Ω	VN2110N3	VN2110NF	VN2110ND

[†]MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

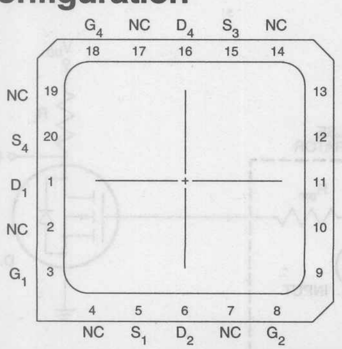
Features

- ☐ Commercial and Military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Pin Configuration



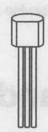
20-pin Ceramic LCC

Advanced DMOS Technology

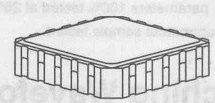
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92



Type "C" Leadless
20 Terminal
Ceramic Chip Carrier

Note: See package outline section for discrete pinout.

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation* @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}†	I_{DRM}
TO-92	0.25A	1.0A	1.0W	170	125	0.25A	1.0A
20 Terminal LCC	0.46A	2.0A	1.25W	170	100	0.46A	2.0A

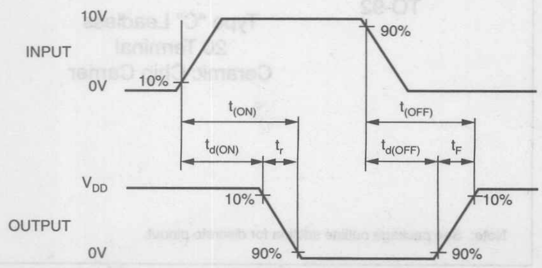
† I_D (continuous) is limited by max rated T_j.
* Total for package.

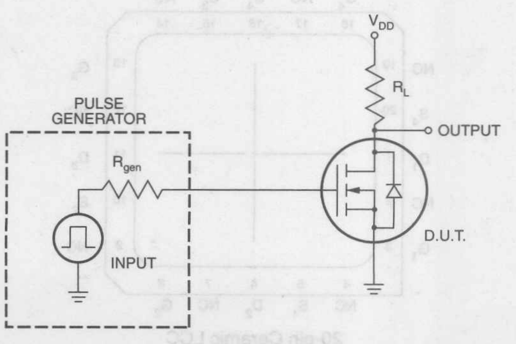
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2110	100			V	$I_D = 1mA, V_{GS} = 0V$
		VN2106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$I_D = 1mA, V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage			0.1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0V, V_{DS}$ = Max Rating
					100		$V_{GS} = 0V, V_{DS}$ = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.15	1.0		A	$V_{GS} = 5V, V_{DS} = 25V$
			1.0	2.50			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.50	6	Ω	$V_{GS} = 5V, I_D = 75mA$
				2	4		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1.0	%/°C	$I_D = 500mA, V_{GS} = 10V$
G_{FS}	Forward Transconductance		150	400		m℧	$V_{DS} = 25V, I_D = 0.5A$
C_{ISS}	Input Capacitance				50	pF	$V_{GS} = 0V, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance				25		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = 25V$ $I_D = 1.0A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$I_{SD} = 1.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			400		ns	$I_{SD} = 1.0A, V_{GS} = 0V$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

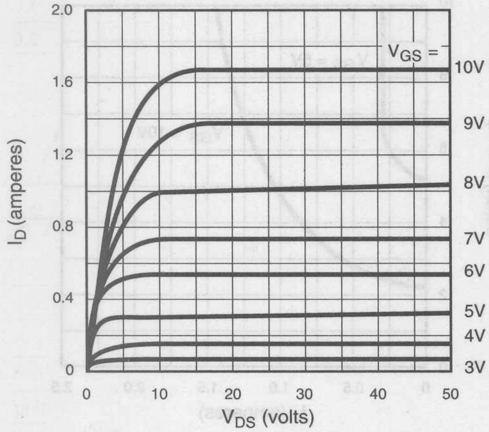
Switching Waveforms and Test Circuit



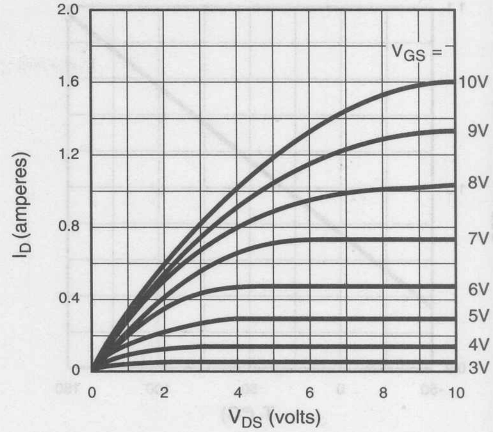


Typical Performance Curves

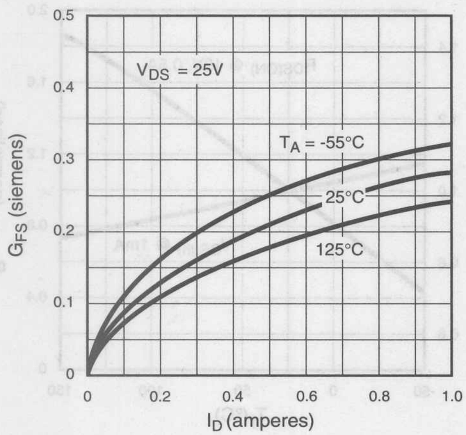
Output Characteristics



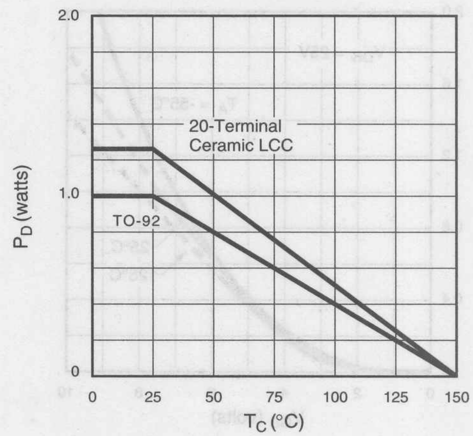
Saturation Characteristics



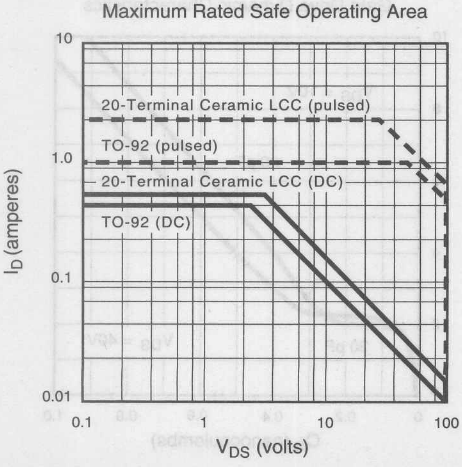
Transconductance vs. Drain Current



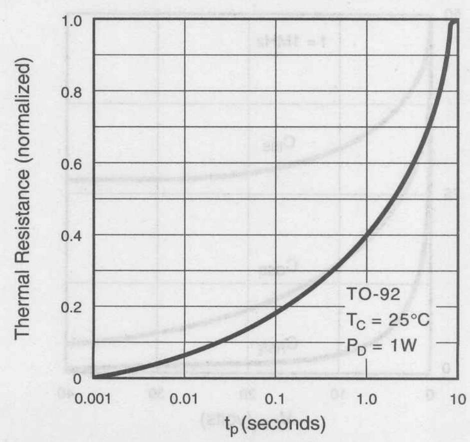
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

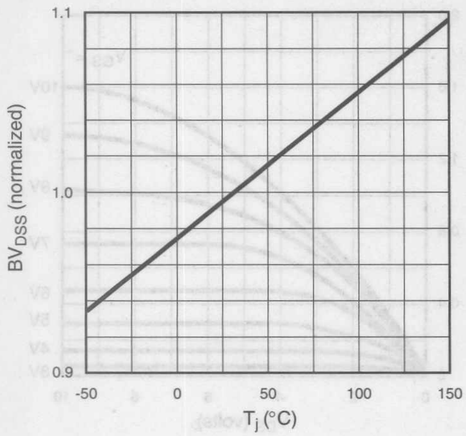


Thermal Response Characteristics

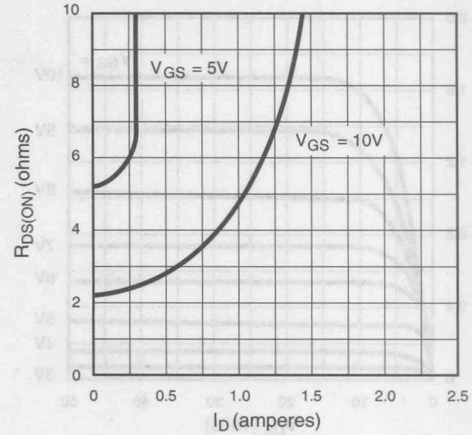


Typical Performance Curves

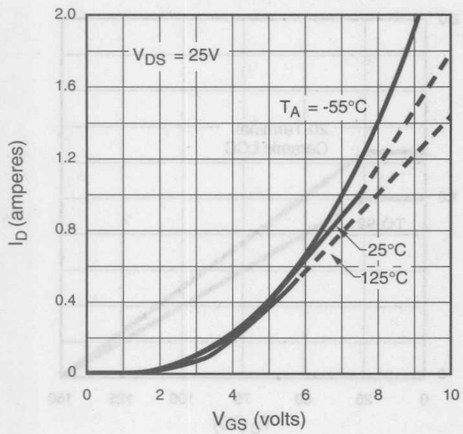
BV$_{DSS}$ Variation with Temperature



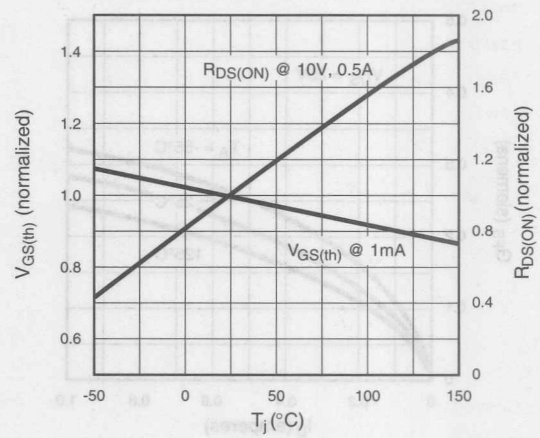
On-Resistance vs. Drain Current



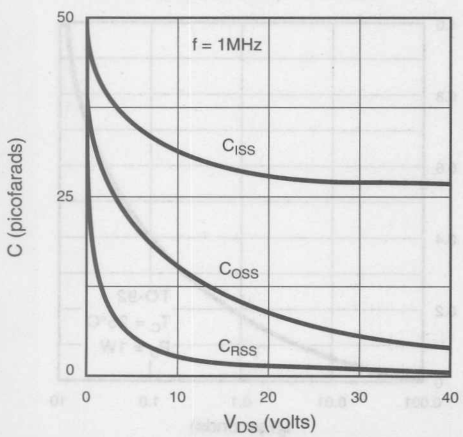
Transfer Characteristics



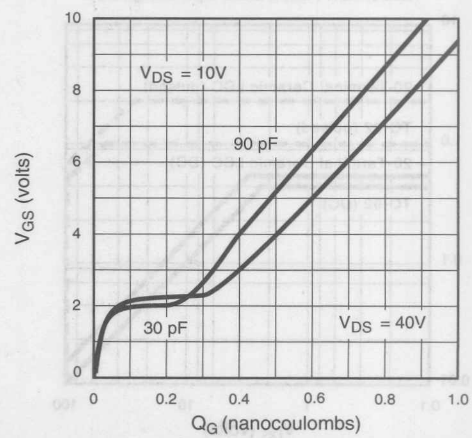
$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92	Dice†
60V	0.35Ω	8A	VN2206N3	VN2206ND
100V	0.35Ω	8A	VN2210N3	VN2210ND

† MIL visual screening available

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

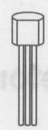
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	1.2A	8.0A	1.0W	170	125	1.2A	8.0A

* I_D (continuous) is limited by max rated T_j.

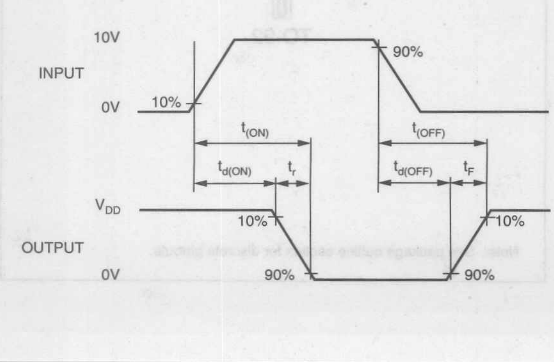
Electrical Characteristics (@ 25°C unless otherwise specified)

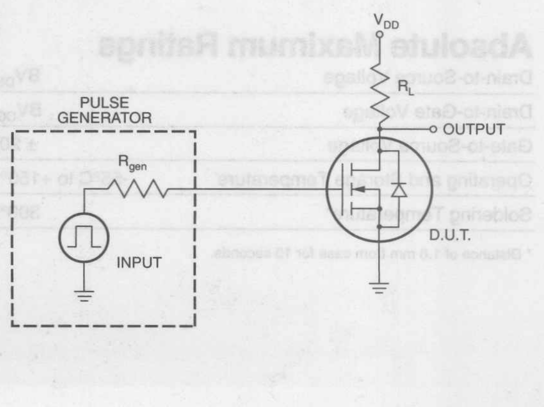
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2206	60			V	$V_{GS} = 0V, I_D = 10mA$
		VN2210	100				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.3	-5.5	mV/°C	$V_{GS} = V_{DS}, I_D = 10mA$
I_{GSS}	Gate Body Leakage			1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				50	µA	$V_{GS} = 0V, V_{DS} =$ Max Rating
					10	mA	$V_{GS} = 0V, V_{DS} = 0.8$ Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		3	4.5		A	$V_{GS} = 5V, V_{DS} = 25V$
			8	17			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.4	0.5	Ω	$V_{GS} = 5V, I_D = 1A$
				0.27	0.35		$V_{GS} = 10V, I_D = 4A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	$V_{GS} = 10V, I_D = 4A$
G_{FS}	Forward Transconductance		1.5	2.0		℧	$V_{DS} = 25V, I_D = 2A$
C_{ISS}	Input Capacitance			300	500	pF	$V_{GS} = 0V, V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			125	200		
C_{RSS}	Reverse Transfer Capacitance			50	65		
$t_{d(ON)}$	Turn-ON Delay Time			10	15	ns	$V_{DD} = 25V$ $I_D = 2A$ $R_{GEN} = 10\Omega$
t_r	Rise Time			10	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			30	50		
t_f	Fall Time			30	50		
V_{SD}	Diode Forward Voltage Drop			1.0	1.6	V	$V_{GS} = 0V, I_{SD} = 4A$
t_{rr}	Reverse Recovery Time			500		ns	$V_{GS} = 0V, I_{SD} = 1A$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

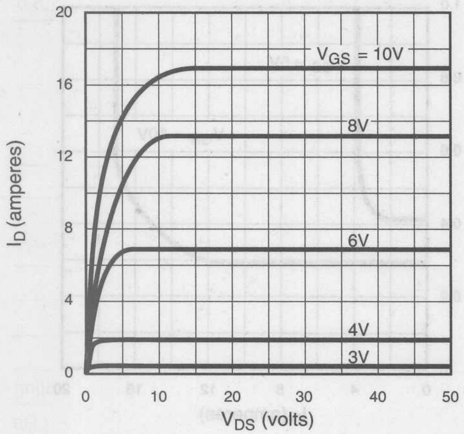
Switching Waveforms and Test Circuit



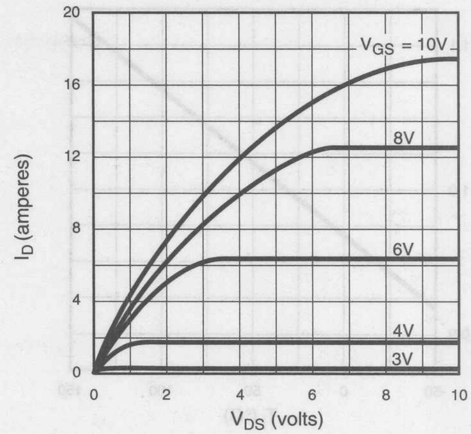


Typical Performance Curves

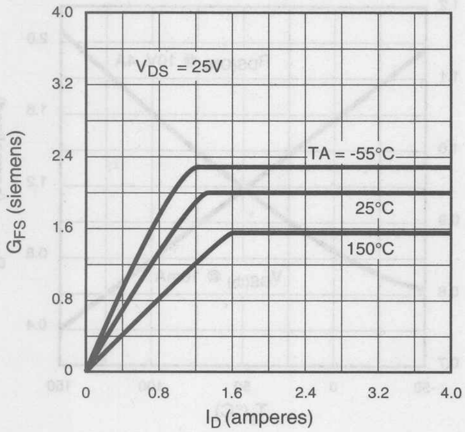
Output Characteristics



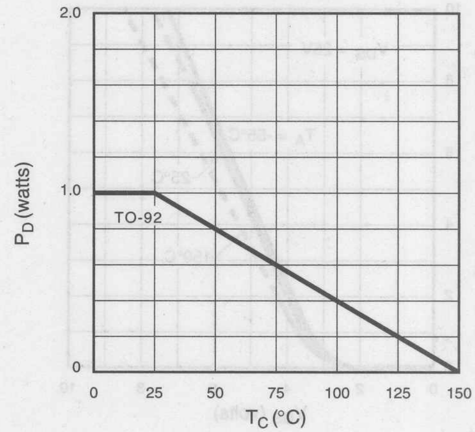
Saturation Characteristics



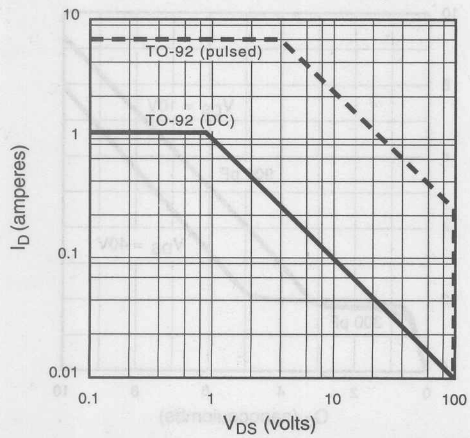
Transconductance vs. Drain Current



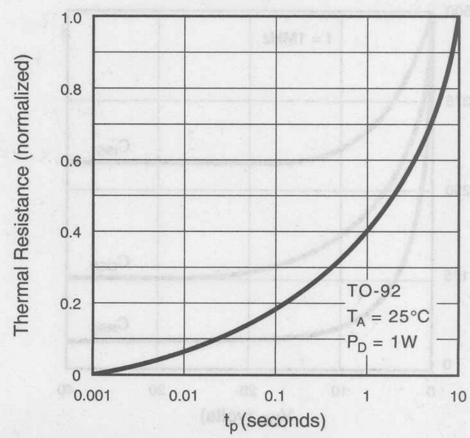
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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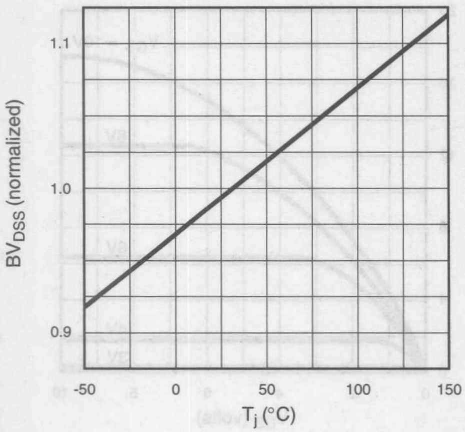
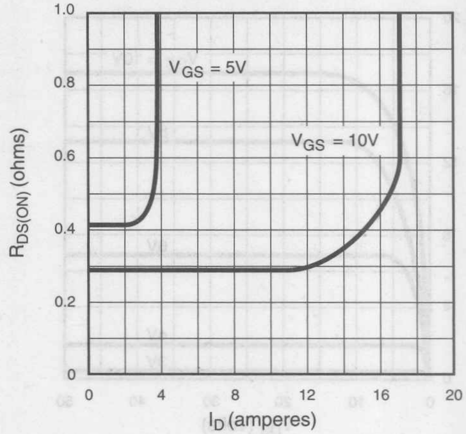
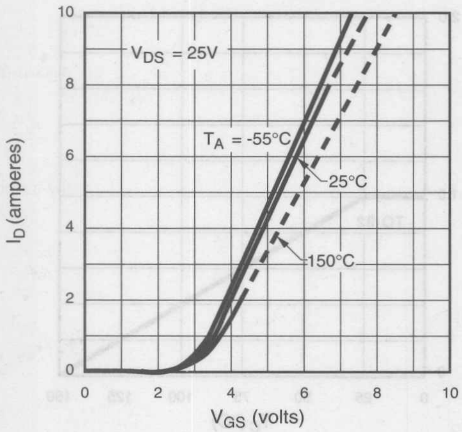
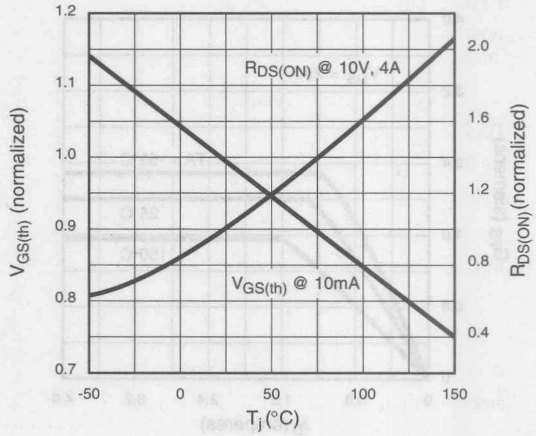
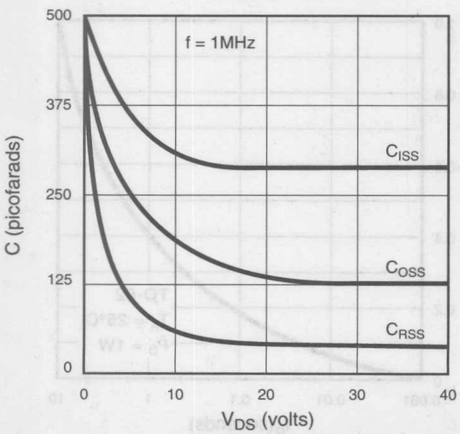
Typical Performance Curves

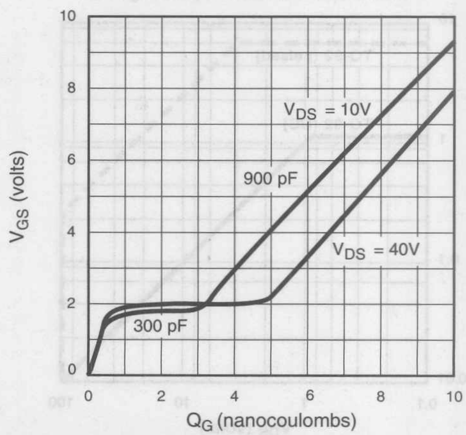












Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	Dice†
200V	1.25Ω	5.0A	VN2220N2	VN2220N3	VN2220ND
240V	1.25Ω	5.0A	VN2224N2	VN2224N3	VN2224ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

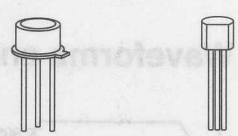
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	1.5A	7.0A	6.0W	125	21	1.5A	7.0A
TO-92	0.9A	5.0A	1.0W	170	125	0.9A	5.0A

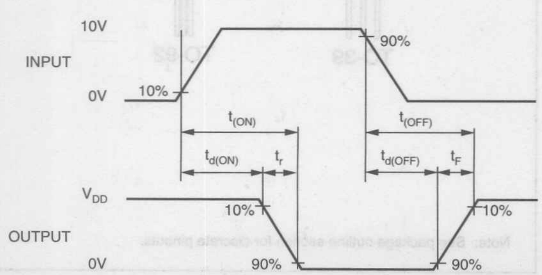
* I_D (continuous) is limited by max rated T_j.

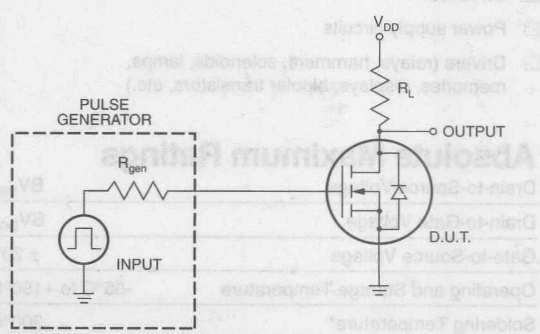
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2224	240			V	$V_{GS} = 0V$, $I_D = 5mA$
		VN2220	200				
$V_{GS(th)}$	Gate Threshold Voltage		1.0		3	V	$V_{GS} = V_{DS}$, $I_D = 5mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.7	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 5mA$
I_{GSS}	Gate Body Leakage			1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				50	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					5	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		2			A	$V_{GS} = 5V$, $V_{DS} = 25V$
			5	10			$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.0	1.5	Ω	$V_{GS} = 5V$, $I_D = 2A$
				0.9	1.25		$V_{GS} = 10V$, $I_D = 2A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	1.4	%/°C	$V_{GS} = 10V$, $I_D = 2A$
G_{FS}	Forward Transconductance		1.0	2.2		℧	$V_{DS} = 25V$, $I_D = 2A$
C_{ISS}	Input Capacitance			300	350	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			85	150		
C_{RSS}	Reverse Transfer Capacitance			20	35		
$t_{d(ON)}$	Turn-ON Delay Time			6	15	ns	$V_{DD} = 25V$ $I_D = 2A$ $R_{GEN} = 10Ω$
t_r	Rise Time			16	25		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	90		
t_f	Fall Time			30	60		
V_{SD}	Diode Forward Voltage Drop			0.8	1.0	V	$V_{GS} = 0V$, $I_{SD} = 100mA$
t_{rr}	Reverse Recovery Time			500		ns	$V_{GS} = 0V$, $I_{SD} = 1A$

Notes:
1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2.All A.C. parameters sample tested.

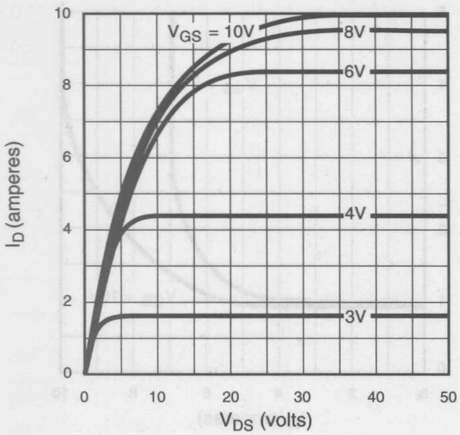
Switching Waveforms and Test Circuit



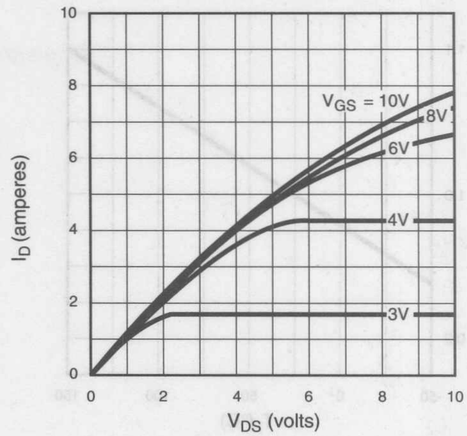


Typical Performance Curves

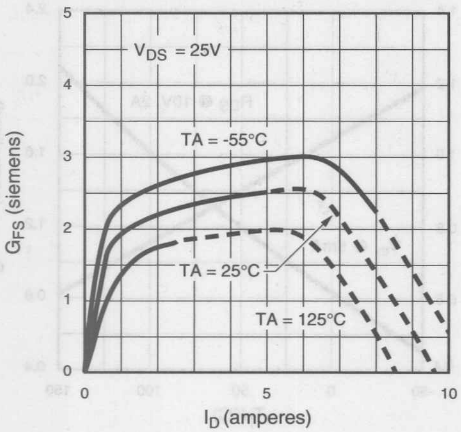
Output Characteristics



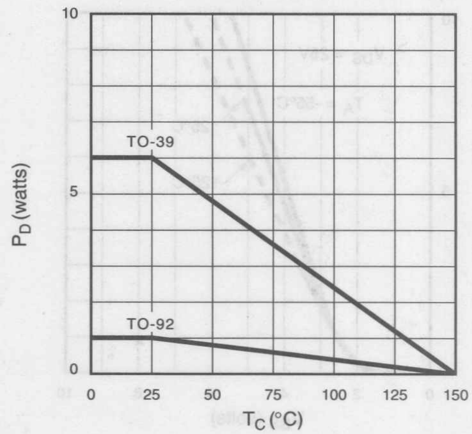
Saturation Characteristics



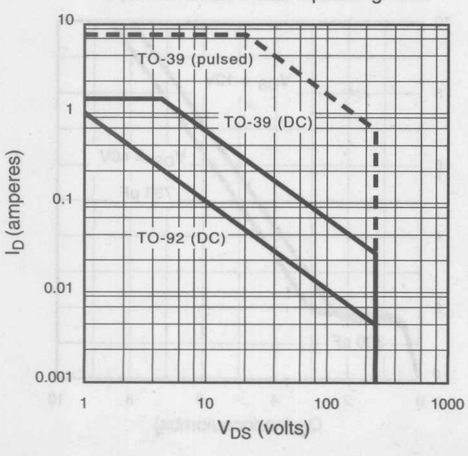
Transconductance vs. Drain Current



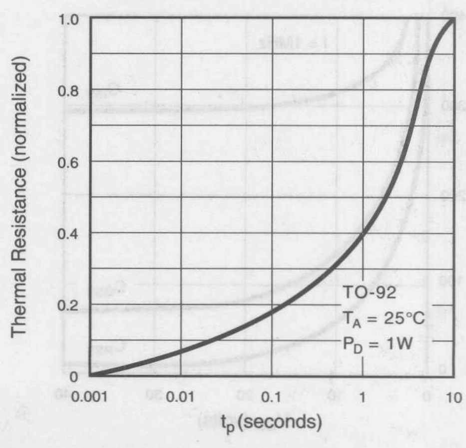
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



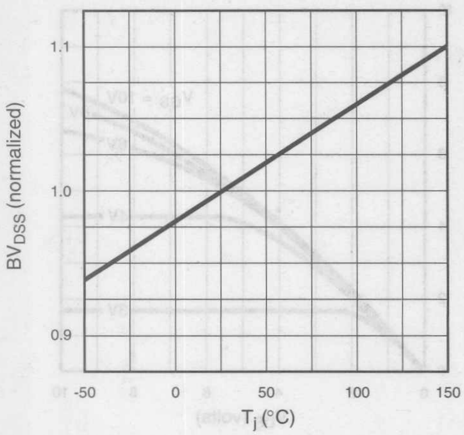
Thermal Response Characteristics



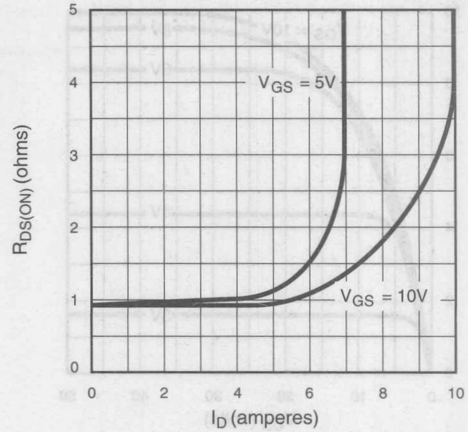
8

Typical Performance Curves

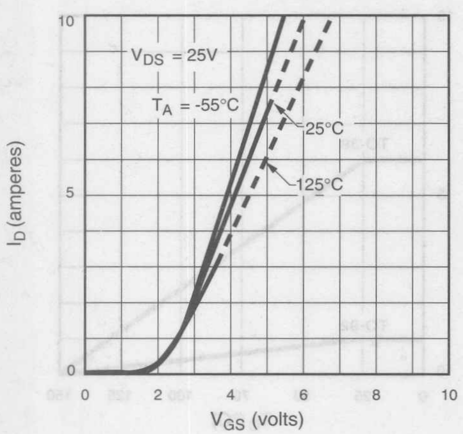
BV_{DSS} Variation with Temperature



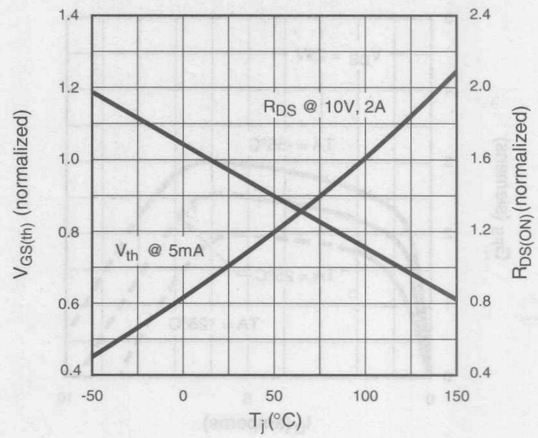
On-Resistance vs. Drain Current



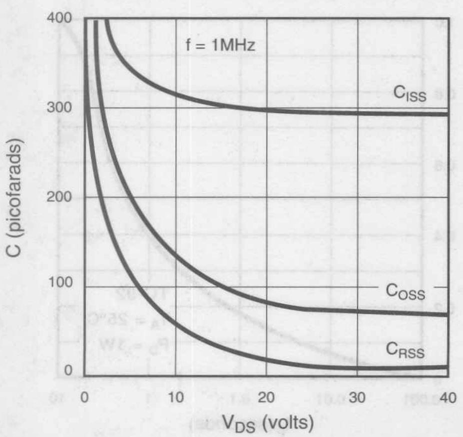
Transfer Characteristics



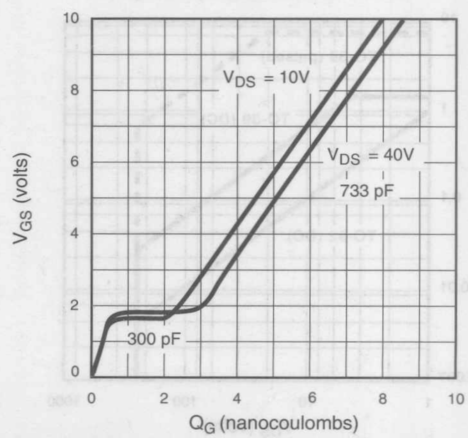
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-92
60V	7.5Ω	0.75A	VN2222LL

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

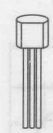
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	0.23A	1.0A	0.8W	156	51

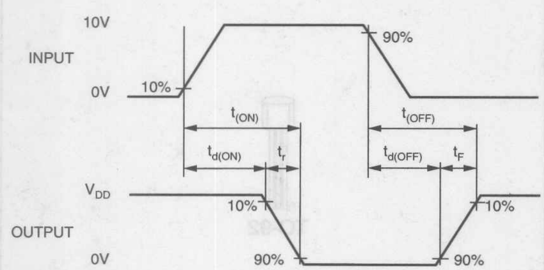
* I_D (continuous) is limited by max rated T_j.

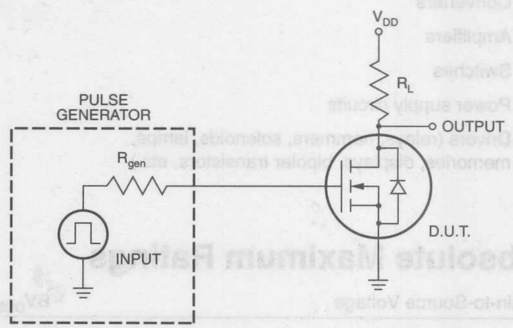
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.6		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10		$V_{GS} = 0V$, V_{DS} = Max Rating
				500	µA	$V_{GS} = 0V$, $V_{DS} = 48V$ $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	0.75			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	$V_{GS} = 5V$, $I_D = 0.2A$
				7.5	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
G_{FS}	Forward Transconductance	100			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			60		
C_{OSS}	Common Source Output Capacitance			25	pF	$V_{GS} = 0V$, $V_{DS} = 25$ f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance			8		
$t_{(ON)}$	Turn-ON Time			10		
$t_{(OFF)}$	Turn-OFF Time			10	ns	$V_{DD} = 15V$, $I_D = 0.6A$ $R_{GEN} = 25\Omega$
V_{SD}	Diode Forward Voltage Drop		0.85		V	$V_{GS} = 0V$, $I_{SD} = 0.2A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

VN2406
VN2410

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
240V	6Ω	1.0A	VN2406B	VN2406L	VN2406D
240V	10Ω	1.0A	—	VN2410L	—

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

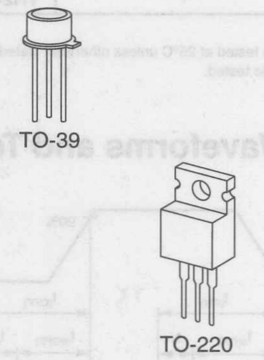
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

8

Thermal Characteristics

Package	I_D (continuous)* @ $T_C = 25°C$	I_D (pulsed)* °C/W	Power Dissipation °C/W	θ_{ja}	θ_{jc}
TO-39	0.63A	3.0A	6.25W	170	20
TO-92	0.17A	1.7A	0.8W	156	21.3
TO-220	1.12A	3.0A	20W	80	6.25

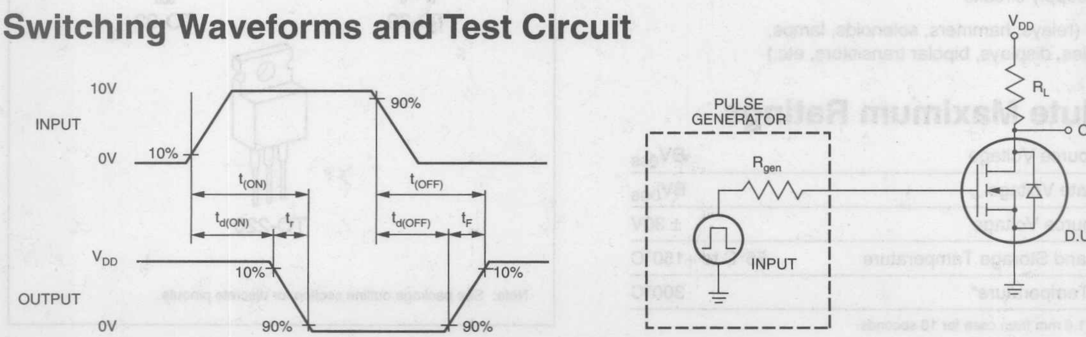
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	240			V	$V_{GS} = 0$, $I_D = 0.1mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2	V	$V_{GS} = V_{DS}$, $I_D = 10mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0$, $V_{DS} = 120V$
				500		$V_{GS} = 0$, $V_{DS} = 120V$, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1.0			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance — All			10	Ω	$V_{GS} = 2.5V$, $I_D = 0.1A$
	VN2410			10		$V_{GS} = 10V$, $I_D = 0.5A$
	VN2406			6		$V_{GS} = 10V$, $I_D = 0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		1.0	1.4	%/°C	$V_{GS} = 10V$, $I_D = 5A$
G_{FS}	Forward Transconductance	300			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			125	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50		
C_{RSS}	Reverse Transfer Capacitance			20		
$t_{d(ON)}$	Turn-ON Delay Time			8	ns	$V_{DD} = 60V$, $I_D = 0.4A$, $R_{GEN} = 25Ω$
t_r	Rise Time			8		
$t_{d(OFF)}$	Turn-OFF Delay Time			18		
t_f	Fall Time			12		
V_{SD}	Diode Forward Voltage Drop — VN2410		1.2		V	$V_{GS} = 0$, $I_{SD} = 0.19A$
	VN2406		1.2		V	$V_{GS} = 0$, $I_{SD} = 0.8A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92
350V	15Ω	1.8V	0.15A	—	VN3515L
400V	12Ω	1.8V	0.15A	VN4012B	VN4012L

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Telecom Switching
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

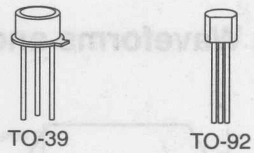
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

8

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
VN3515L	150mA	600mA	1W	156	125	150mA	600mA
VN4012B	420mA	1.3A	5W	125	—	420mA	1.3A
VN4012L	160mA	650mA	1W	156	125	160mA	650mA

* I_D (continuous) is limited by max rated T_j.

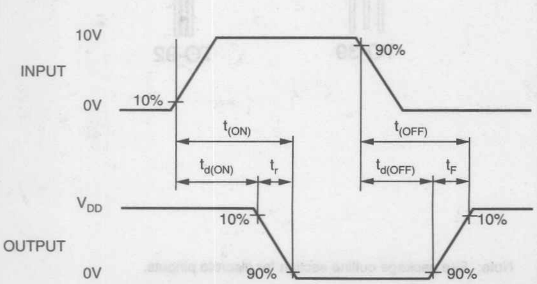
Electrical Characteristics (@ 25°C unless otherwise specified)

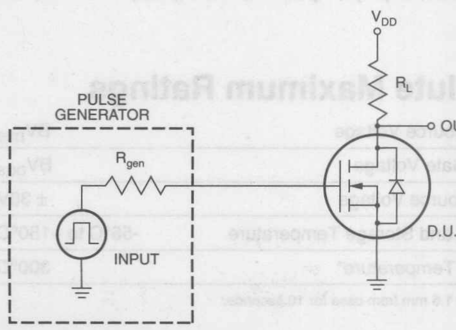
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN3515	350			V	$V_{GS} = 0, I_D = 100\mu A$
		VN4012	400				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.8	V	$V_{GS} = V_{DS}, I_D = 1mA$
I_{GSS}	Gate Body Leakage				10	nA	$V_{GS} = \pm 20V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0, V_{DS}$ = Max Rating
					100		$V_{GS} = 0, V_{DS}$ = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.15	0.3		A	$V_{DS} = 10V, V_{GS} = 4.5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	VN3515		9.5	15	Ω	$V_{GS} = 4.5V, I_D = 100mA$
				17	35		$V_{GS} = 4.5V, I_D = 100mA, TA = 125°C$
		VN4012		9.5	12		$V_{GS} = 4.5V, I_D = 100mA$
				17	30		$V_{GS} = 4.5V, I_D = 100mA, TA = 125°C$
G_{FS}	Forward Transconductance		125	350		m℧	$V_{DS} = 15V, I_D = 100mA$
C_{ISS}	Input Capacitance				90	pF	$V_{DS} = 25V, V_{GS} = 0V$ f = 1MHz
C_{OSS}	Common Source Output Capacitance				20		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	$V_{DD} = 25V$ $I_D = 100mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time				20		
$t_{d(OFF)}$	Turn-OFF Delay Time				65		
t_f	Fall Time				65		
V_{SD}	Diode Forward Voltage Drop				1.2	V	$V_{GS} = 0, I_{SD} = 160mA$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
3. See TN06D data sheet for characteristic curves.

Switching Waveforms and Test Circuit





Chapter 9 – DMOS P-Channel Discretes

Supertex inc.

VP01A

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package						
			TO-39	TO-52	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
-40V	8Ω	-0.5A	VP0104N2	VP0104N9	VP0104N3	VP0104N5	VP0104N6	VP0104N7	VP0104ND
-60V	8Ω	-0.5A	VP0106N2	VP0106N9	VP0106N3	VP0106N5	VP0106N6	VP0106N7	VP0106ND
-90V	8Ω	-0.5A	VP0109N2	VP0109N9	VP0109N3	VP0109N5	—	—	VP0109ND

* 14 pin side brazed ceramic DIP
† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

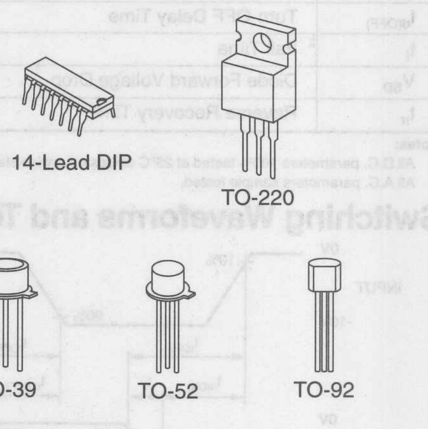
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See package outline section for discrete pinouts.
Note 2: See array section for quad pinouts.

9

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed) @ $T_C = 25°C$	Power Dissipation °C/W	θ_{ja} °C/W	θ_{jc}	I_{DR}*	I_{DRM}
TO-39	-0.45A	-1.0A	3.5W	125	35	-0.5A	-1.0A
TO-52	-0.25A	-1.0A	1.0W	170	125	-0.25A	-1.0A
TO-92	-0.25A	-0.8A	1.0W	170	125	-0.25A	-0.8A
TO-220	-1.0A	-1.2A	15.0W	70	8.3	-1.0A	-1.2A
Plastic DIP	Refer to Arrays & Special Functions Section.						
Ceramic DIP							

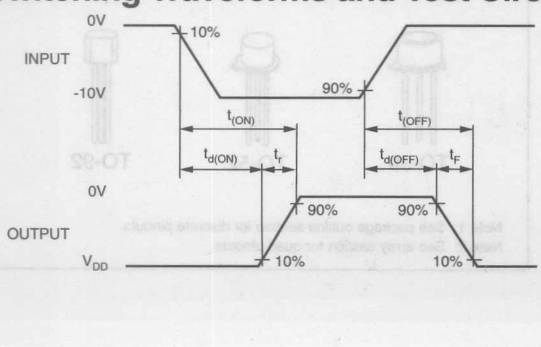
* I_D (continuous) is limited by max rated T_j.

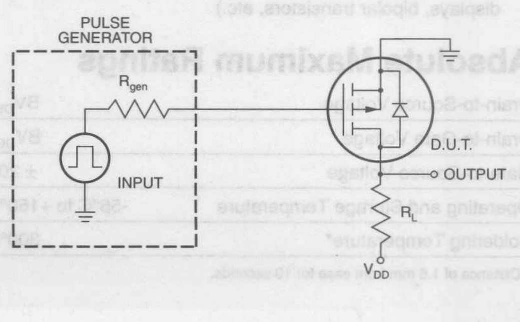
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0109	-90			V	$I_D = -1.0mA$, $V_{GS} = 0V$
		VP0106	-60				
		VP0104	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			5.8	6.5	mV/°C	$I_D = -1.0mA$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.15	-0.25		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-0.50	-1.2			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			11	15	Ω	$V_{GS} = -5V$, $I_D = -0.1A$
				6	8		$V_{GS} = -10V$, $I_D = -0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	$I_D = -0.5A$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		150	190		m℧	$V_{DS} = -25V$, $I_D = -0.5A$
C_{ISS}	Input Capacitance			45	60	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	$V_{DD} = -25V$ $I_D = -0.5A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	7		
t_f	Fall Time			4	10		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	$I_{SD} = -1.0A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			400		ns	$I_{SD} = -1.0A$, $V_{GS} = 0V$

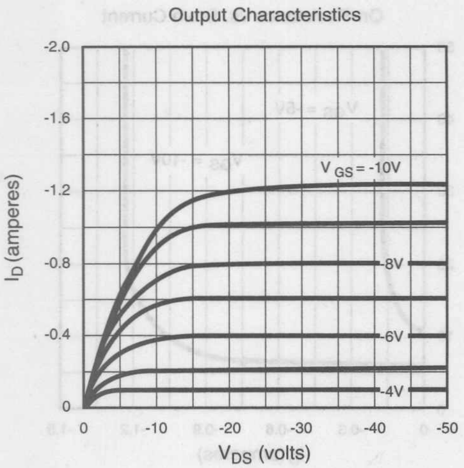
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

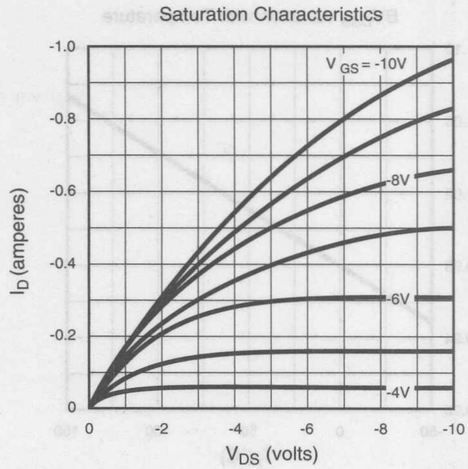
Switching Waveforms and Test Circuit

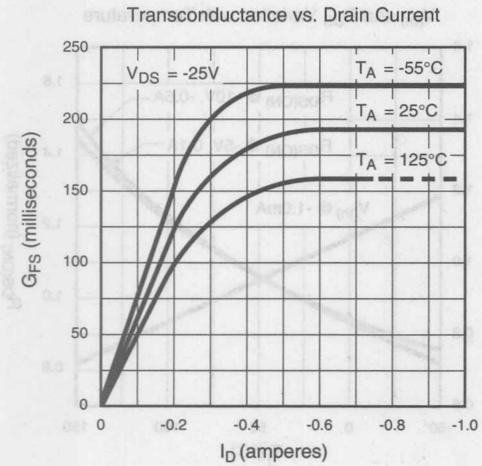


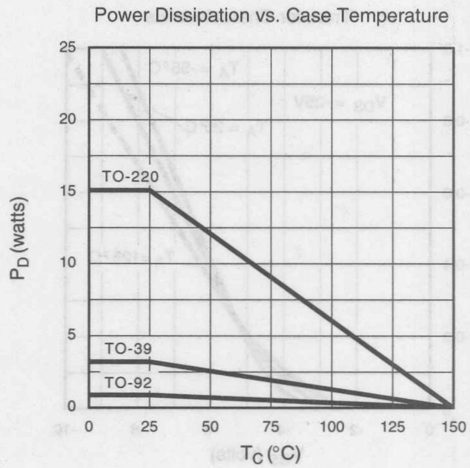


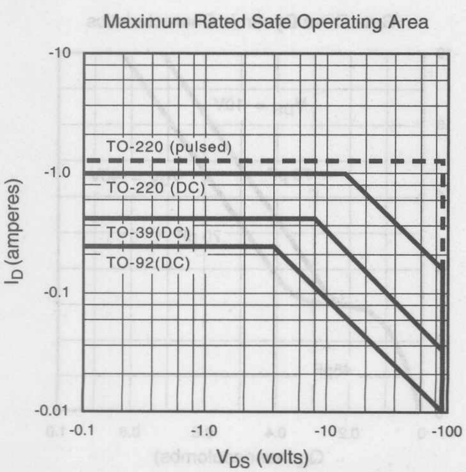
Typical Performance Curves

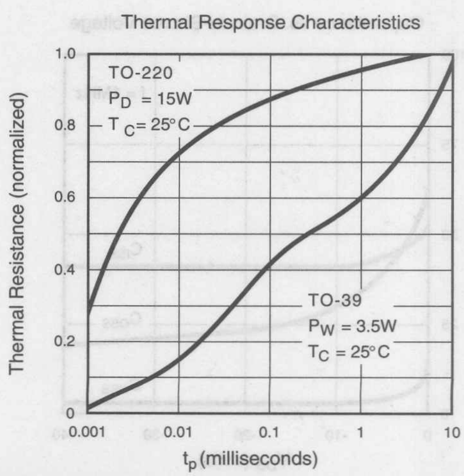






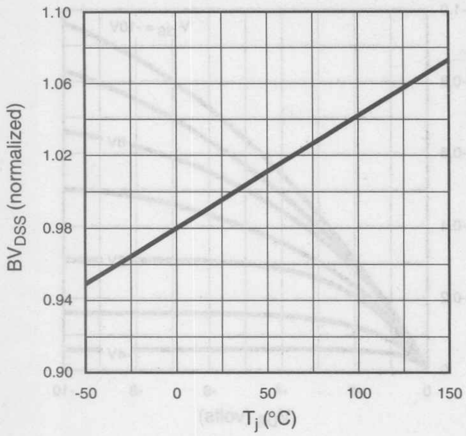




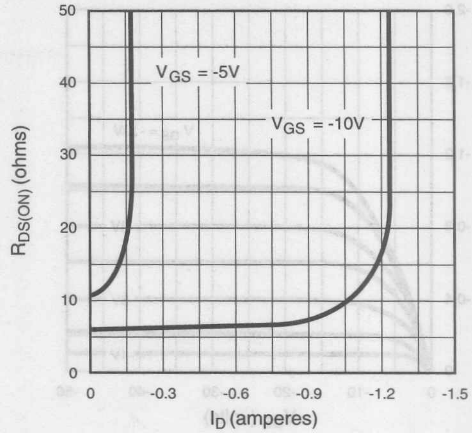


Typical Performance Curves

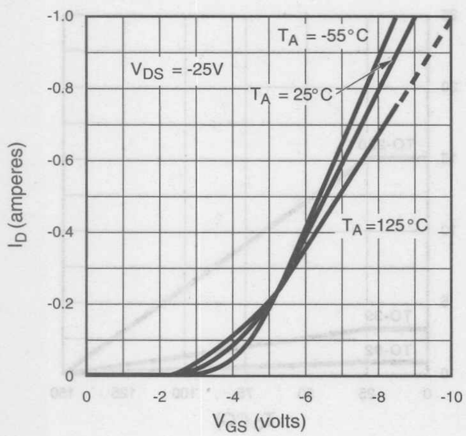
BV_{DSS} Variation with Temperature



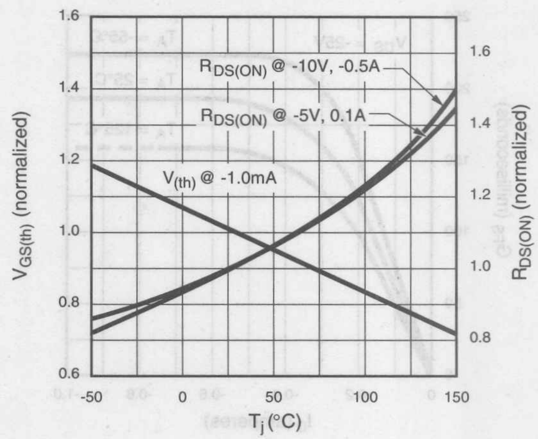
On-Resistance vs. Drain Current



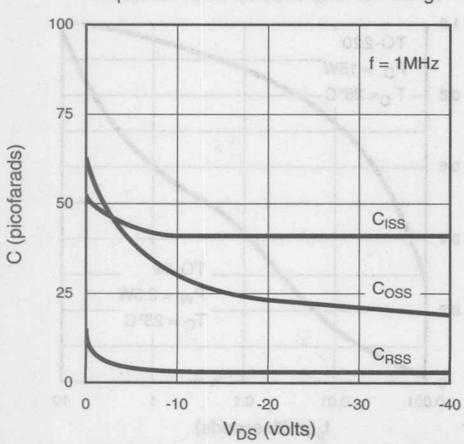
Transfer Characteristics



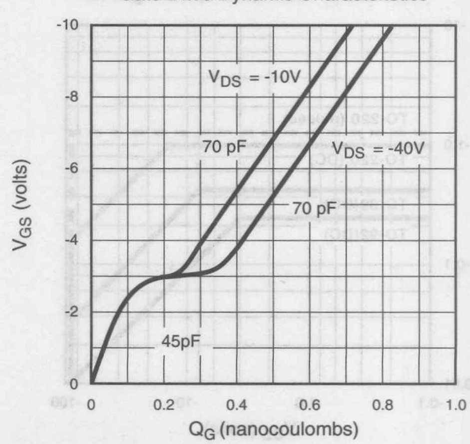
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	DICE†
-160V	25Ω	-100mA	VP0116N2	VP0116N3	VP0116N5	VP0116ND
-200V	25Ω	-100mA	VP0120N2	VP0120N3	VP0120N5	VP0120ND

†MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

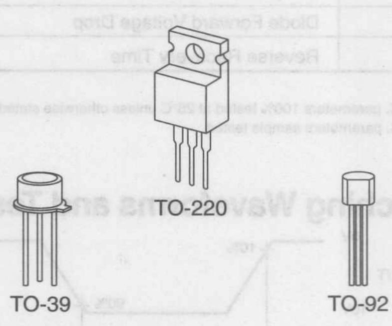
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.2A	-0.65A	3.5W	125	35	-0.2A	-0.65A
TO-92	-0.1A	-0.35A	1.0W	170	125	-0.1A	-0.35A
TO-220	-0.425A	-1.0A	15.0W	70	8.3	-0.425A	-1.0A

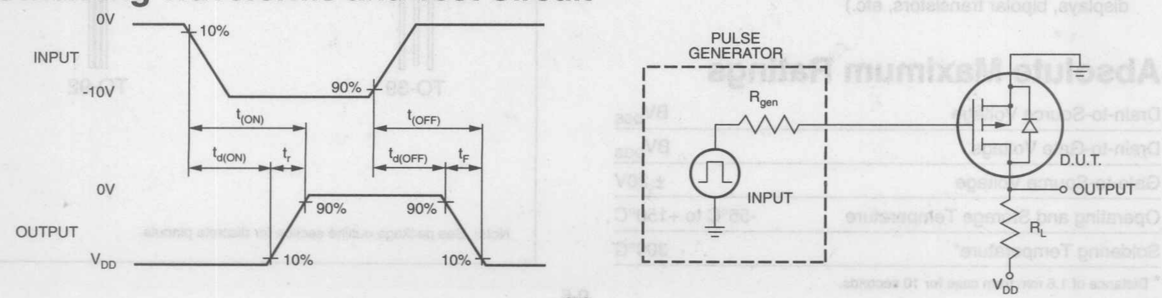
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

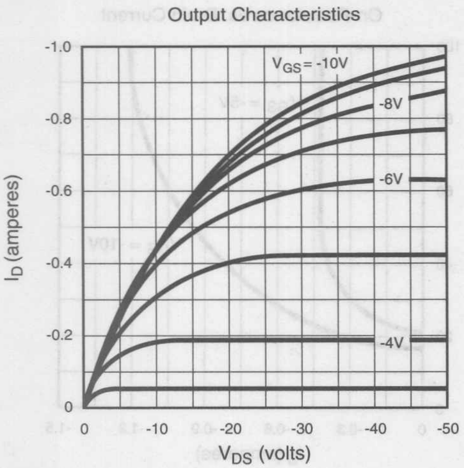
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0120	-200			V	$I_D = -1.0mA$, $V_{GS} = 0V$
		VP0116	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			6.0		mV/°C	$I_D = -1.0mA$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-100	-400		mA	$V_{GS} = -5V$, $V_{DS} = -25V$
			-350	-750			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			25	40	Ω	$V_{GS} = -5V$, $I_D = -50mA$
				15	25		$V_{GS} = -10V$, $I_D = -100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6		%/°C	$I_D = -100mA$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		50	70		m℧	$V_{DS} = -25V$, $I_D = -100mA$
C_{ISS}	Input Capacitance			50	60	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			10	30		
C_{RSS}	Reverse Transfer Capacitance			5	10		
$t_{d(ON)}$	Turn-ON Delay Time			4	10	ns	$V_{DD} = -25V$ $I_D = -350mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time			4	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			4	10		
t_f	Fall Time			4	11		
V_{SD}	Diode Forward Voltage Drop			-1.0		V	$I_{SD} = -0.5A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			500		ns	$I_{SD} = -0.5A$, $V_{GS} = 0V$

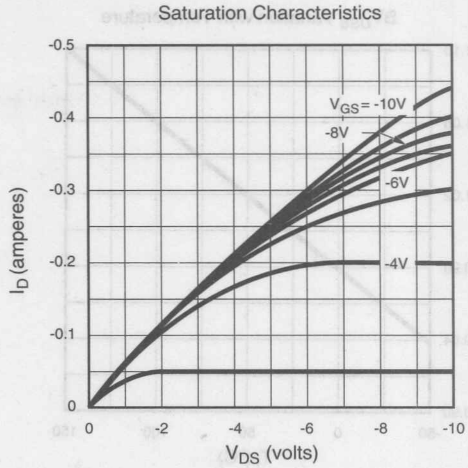
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

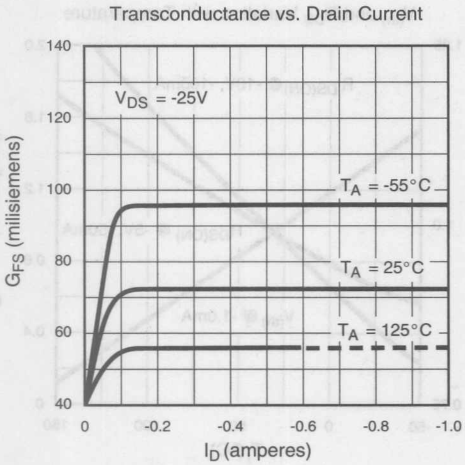
Switching Waveforms and Test Circuit

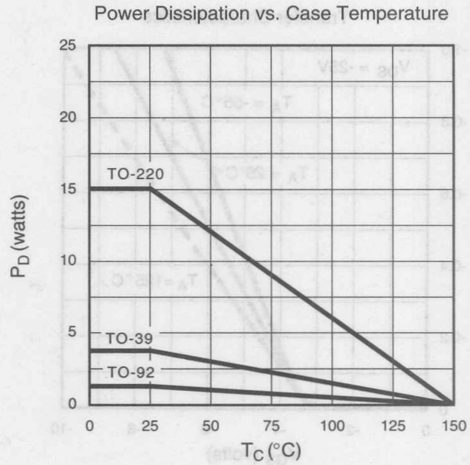


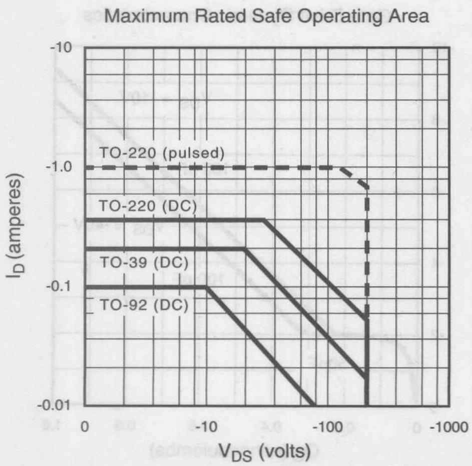
Typical Performance Curves

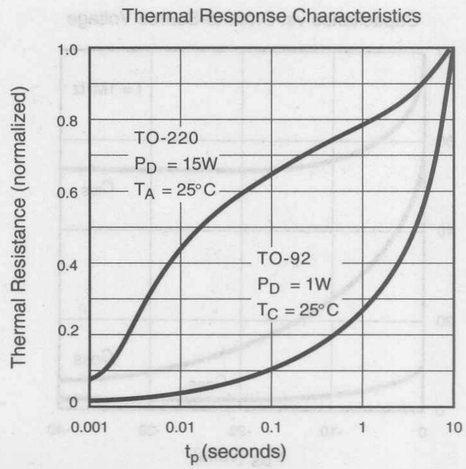






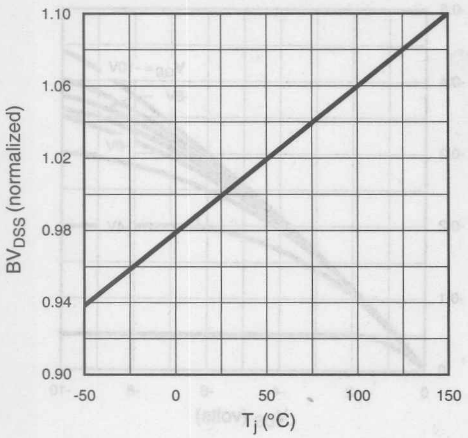




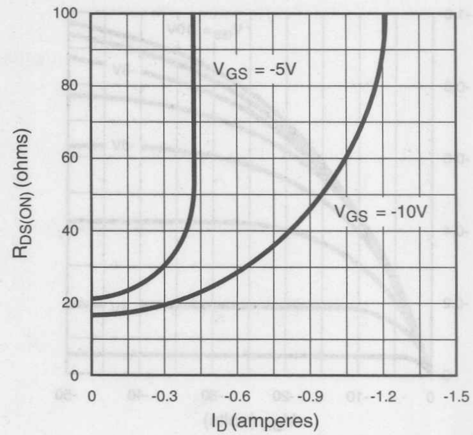


Typical Performance Curves

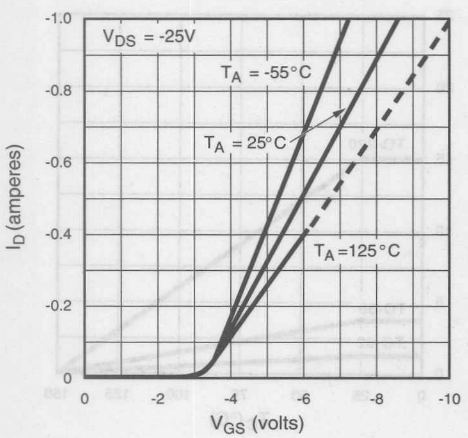
BV$_{DSS}$ Variation with Temperature



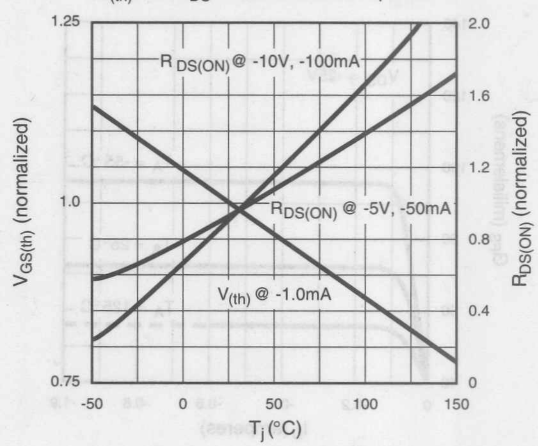
On-Resistance vs. Drain Current



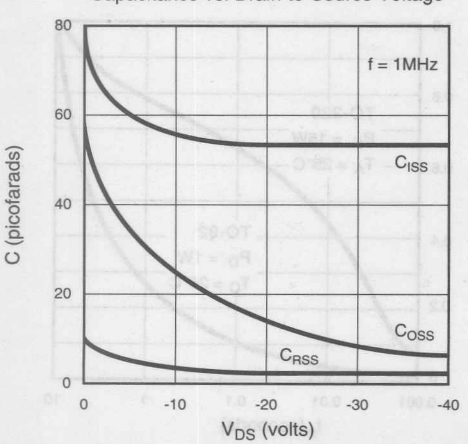
Transfer Characteristics



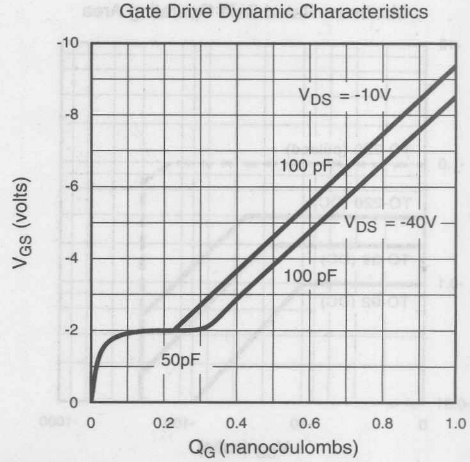
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE†
-350V	6Ω	-1.5A	VP0335N1	VP0335N2	VP0335N5	VP0335ND
-400V	6Ω	-1.5A	VP0340N1	VP0340N2	VP0340N5	VP0340ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

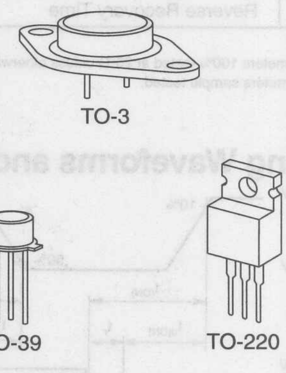
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-3	-2.7A	-5.0A	100W	1.25	300	-2.7A	-5.0A
TO-39	-0.7A	-5.0A	6W	20.8	125	-0.7A	-5.0A
TO-220	-1.6A	-5.0A	50W	2.5	40	-1.6A	-5.0A

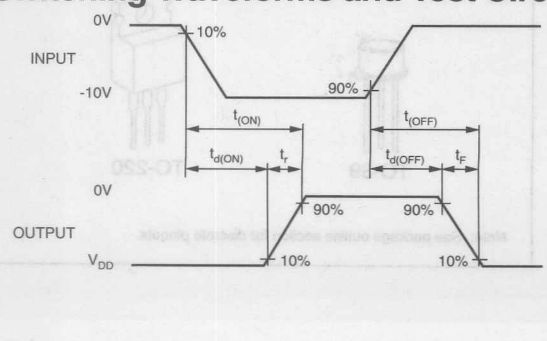
* I_D (continuous) is limited by max rated T_j.

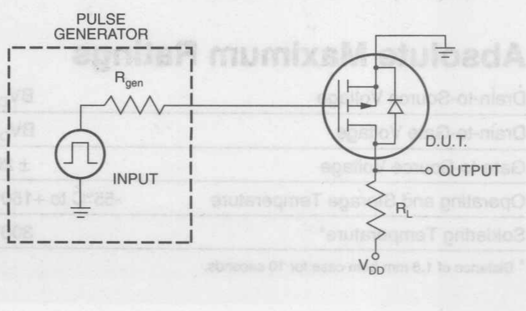
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0340	-400			V	$V_{GS} = 0V$, $I_D = -1.0mA$
		VP0335	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.8	6.0	mV/°C	$I_D = -1.0mA$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-200	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-2.0	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			-1.0		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-1.5	-3.5			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6		Ω	$V_{GS} = -5V$, $I_D = -50mA$
				4.5	6		$V_{GS} = -10V$, $I_D = -100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.2	%/°C	$I_D = -100mA$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		0.5	0.8		℧	$V_{DS} = -25V$, $I_D = -100mA$
C_{ISS}	Input Capacitance			550	700	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			90	120		
C_{RSS}	Reverse Transfer Capacitance			20	50		
$t_{d(ON)}$	Turn-ON Delay Time			25	40	ns	$V_{DD} = -25V$ $I_D = -1A$ $R_{GEN} = 10\Omega$
t_r	Rise Time			25	40		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	110		
t_f	Fall Time			20	40		
V_{SD}	Diode Forward Voltage Drop			-1.0	-1.3	V	$I_{SD} = -0.5A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			500		ns	$I_{SD} = -0.5A$, $V_{GS} = 0V$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

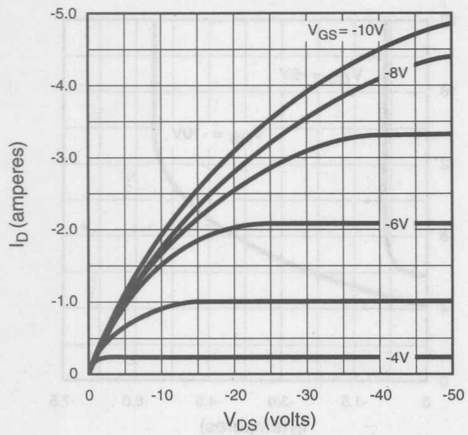
Switching Waveforms and Test Circuit



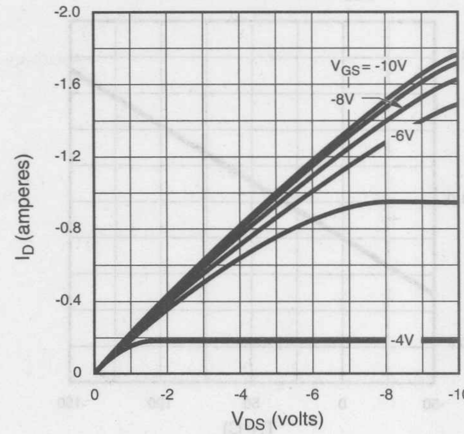


Typical Performance Curves

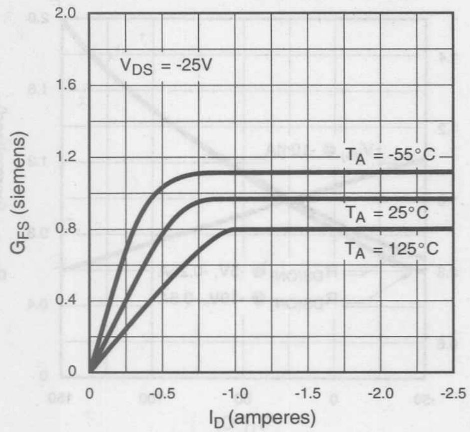
Output Characteristics



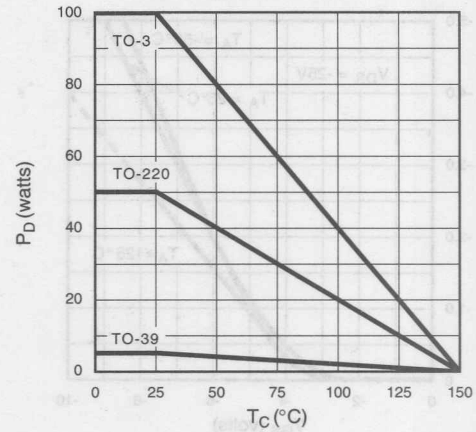
Saturation Characteristics



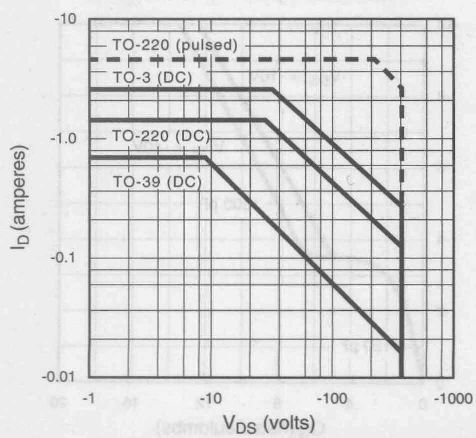
Transconductance vs. Drain Current



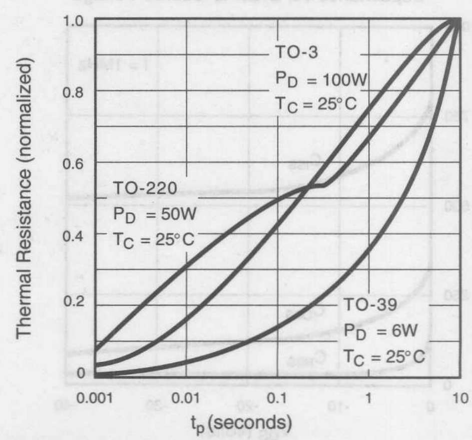
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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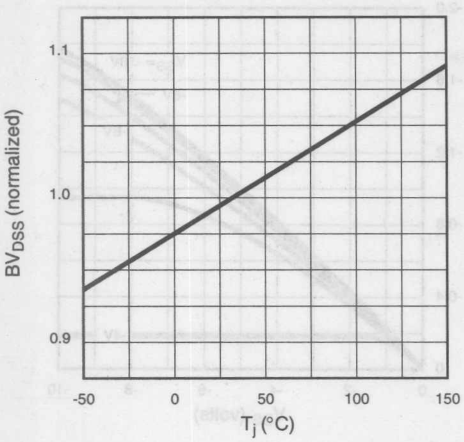
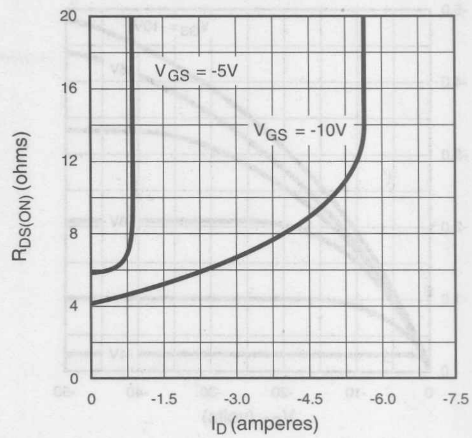
Typical Performance Curves

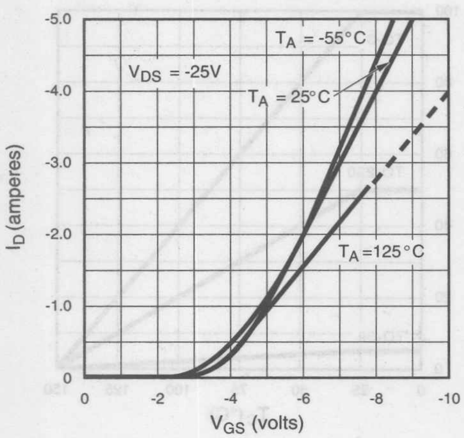
BV_{DSS} Variation with Temperature



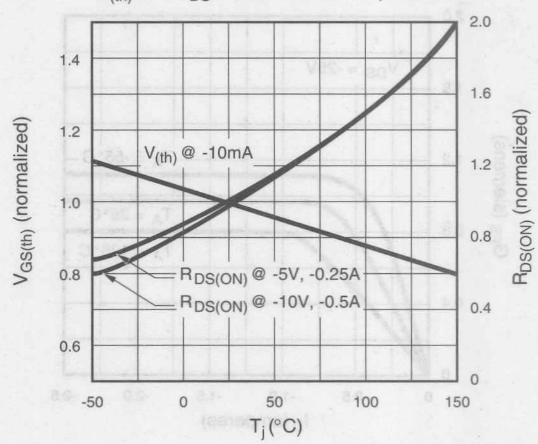
On-Resistance vs. Drain Current



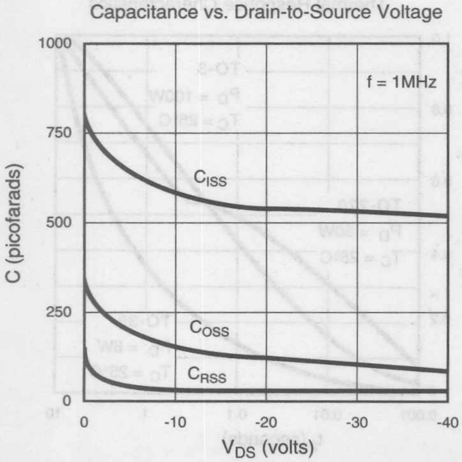
Transfer Characteristics



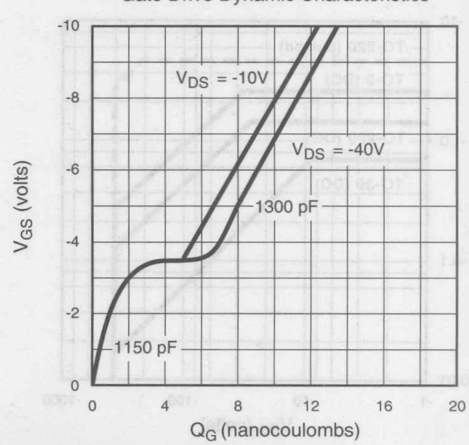
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE†
-450V	7.5Ω	-1A	VP0345N1	VP0345N2	VP0345N5	VP0345ND
-500V	7.5Ω	-1A	VP0350N1	VP0350N2	VP0350N5	VP0350ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

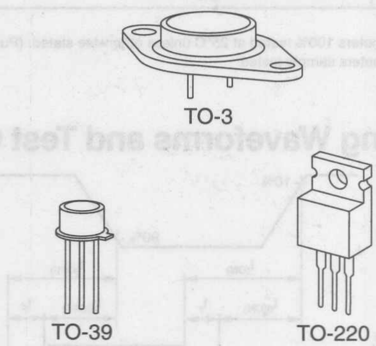
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-3	-1.5A	-3.0A	100W	1.25	30	-1.5A	-3.0A
TO-39	-0.4A	-3.0A	6W	20.8	125	-0.4A	-3.0A
TO-220	-1.0A	-3.0A	50W	2.5	40	-1.0A	-3.0A

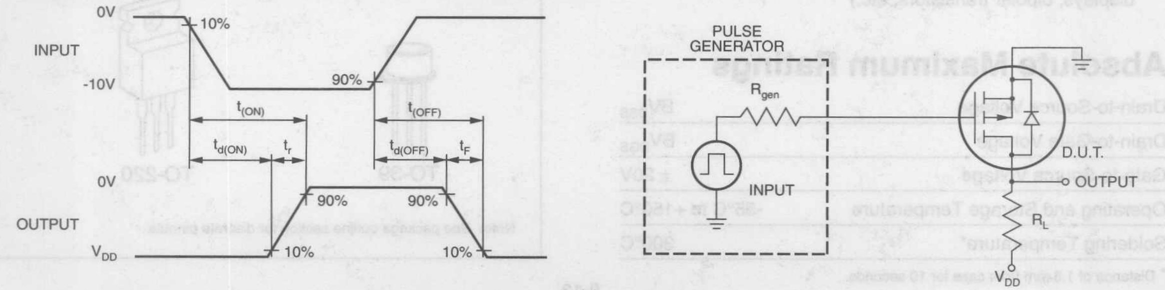
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0350	-500			V	V_{GS} = 0, I_D = -10mA
		VP0345	-450				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	$V_{GS} = V_{DS}$, I_D = -10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.8	6.0	mV/°C	$V_{GS} = V_{DS}$, I_D = -10mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				-200	µA	V_{GS} = 0V, V_{DS} = Max Rating
					-2	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-1.5		A	V_{GS} = -5V, V_{DS} = -25V
			-1.0	-3.0			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6.0		Ω	V_{GS} = -5V, I_D = -0.25A
				5.5	7.5		V_{GS} = -10V, I_D = -0.25A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.2	%/°C	V_{GS} = -10V, I_D = -0.25A
G_{FS}	Forward Transconductance		0.25	0.45		℧	V_{DS} = -25V, I_D = -0.5A
C_{ISS}	Input Capacitance			720	800	pF	V_{GS} = 0V, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			110	130		
C_{RSS}	Reverse Transfer Capacitance			20	50		
$t_{d(ON)}$	Turn-ON Delay Time			11	30	ns	V_{DD} = -25V I_D = -1A R_{GEN} = 10Ω
t_r	Rise Time			11	30		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	100		
t_f	Fall Time			22	30		
V_{SD}	Diode Forward Voltage Drop			-1.0	-1.3	V	V_{GS} = 0V, I_{SD} = -0.25A
t_{rr}	Reverse Recovery Time			550		ns	V_{GS} = 0V, I_{SD} = -0.25A

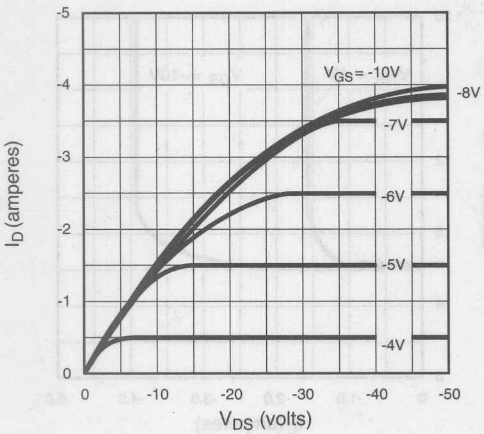
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

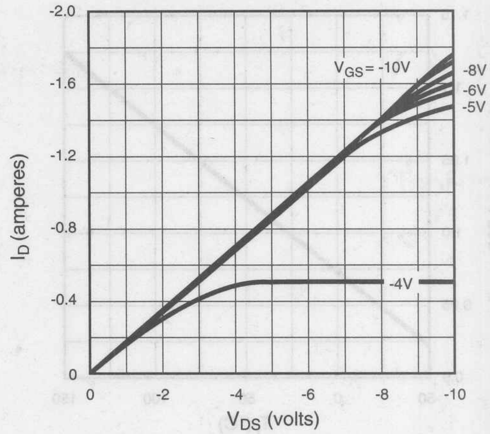


Typical Performance Curves

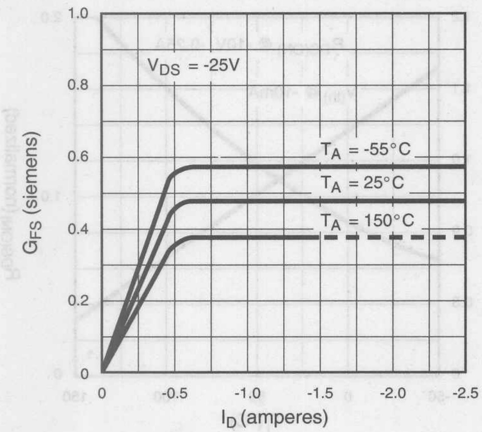
Output Characteristics



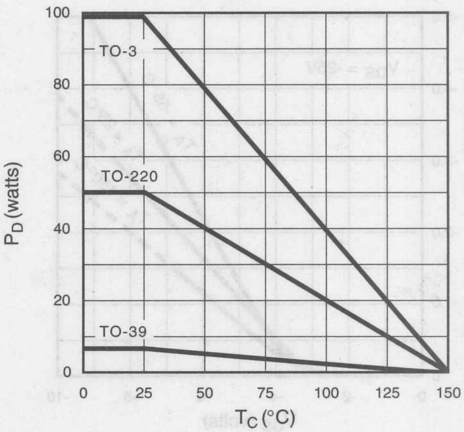
Saturation Characteristics



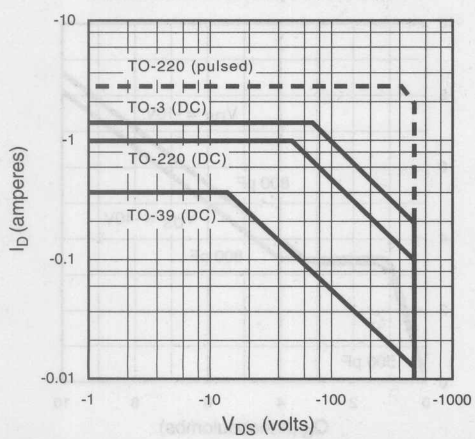
Transconductance vs. Drain Current



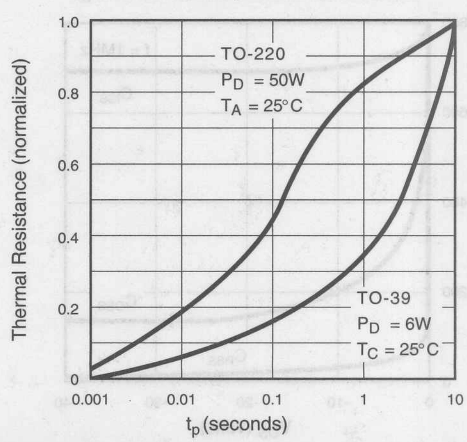
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

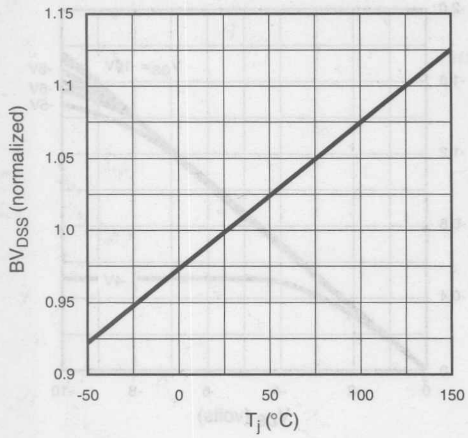


Thermal Response Characteristics

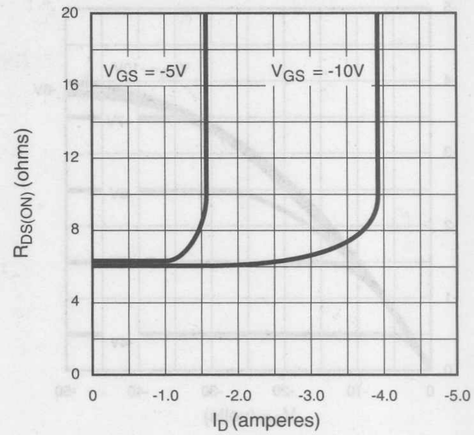


Typical Performance Curves

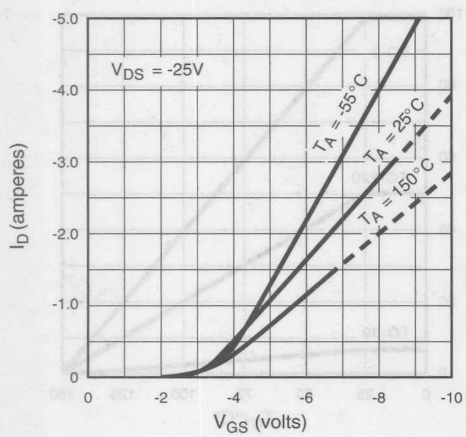
BV$_{DSS}$ Variation with Temperature



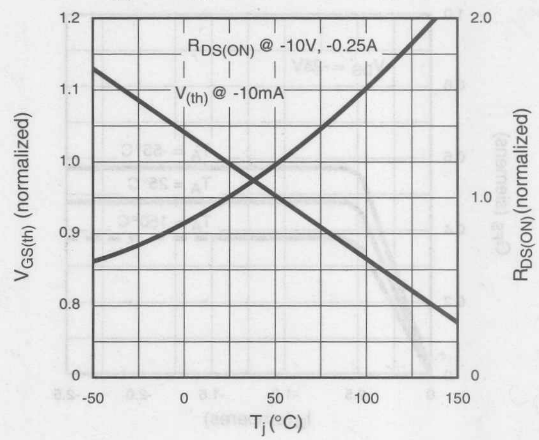
On-Resistance vs. Drain Current



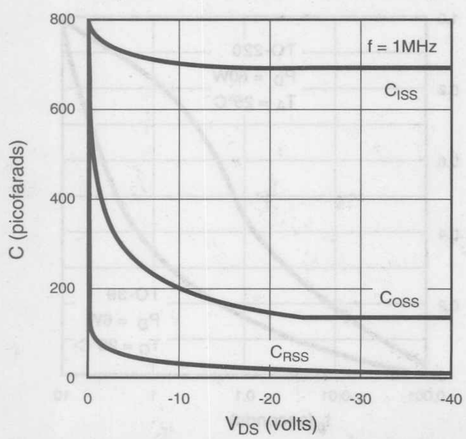
Transfer Characteristics



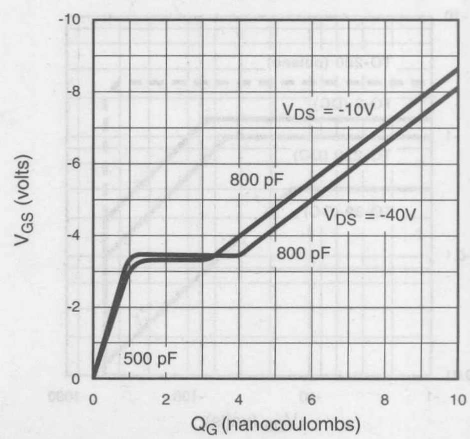
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92
-30V	2.5Ω	-1.5A	VP0300B	VP0300L

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

TO-39 TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	-1.25A	-3.0A	6.25W	125	20
TO-92	-0.32A	-0.87A	1.0W	170	41

* I_D (continuous) is limited by max rated T_j.

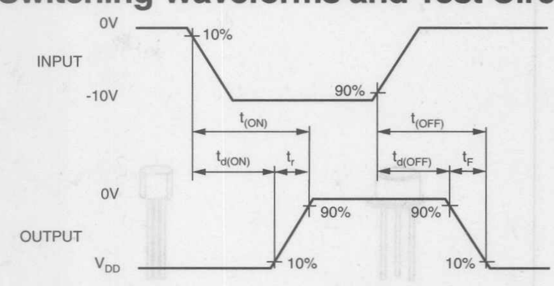
Electrical Characteristics (@ 25°C unless otherwise specified)

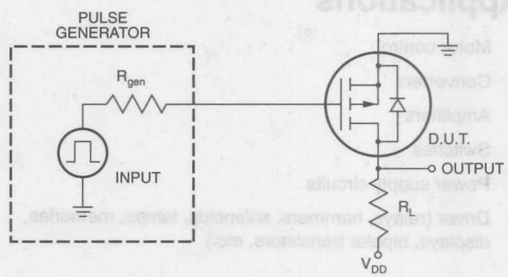
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30			V	V_{GS}= 0V, I_D =-10µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-1.8	-4.5	V	$V_{GS} = V_{DS}$, I_D = -1mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±30V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-10		V_{GS} = 0V, V_{DS} = -25V
				-500	µA	V_{GS} = 0V, V_{DS} = -25V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-1.5	-1.7		A	V_{GS} = -12V, V_{DS} = -10V
$R_{DS(ON)}$	Static Drain-to-SourceON-State Resistance			2.5	Ω	V_{GS} = -12V, I_D = -1A
G_{FS}	Forward Transconductance	200			m℧	V_{DS} = -10V, I_D = -0.5A
C_{ISS}	Input Capacitance			150	pF	V_{GS} = 0V, V_{DS} = -15V f = 1MHz
C_{OSS}	Common Source Output Capacitance			120		
C_{RSS}	Reverse Transfer Capacitance			60		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = -25V, I_D = -1A R_{GEN} = 25Ω
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		-1.2		V	V_{GS} = 0V, I_{SD} = -1.5A

Notes

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE†
-350V	75Ω	-200mA	VP0535N2	VP0535N3	VP0535ND
-400V	75Ω	-200mA	VP0540N2	VP0540N3	VP0540ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
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- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

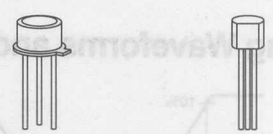
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39 TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.2A	-0.5A	3.5W	35	125	-0.2A	-0.5A
TO-92	-0.1A	-0.5A	1.0W	125	170	-0.1A	-0.5A

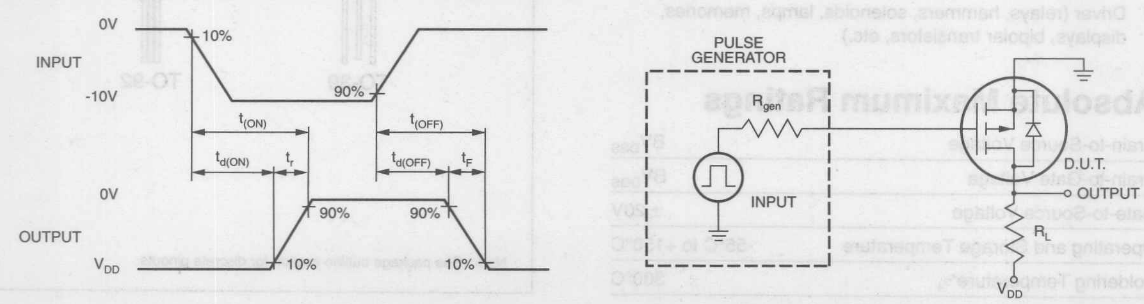
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0540	-400			V	$V_{GS} = 0V$, $I_D = -1mA$
		VP0535	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			3.5	6.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-500		$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			-80		mA	$V_{GS} = -5V$, $V_{DS} = -25V$
			-200	-350			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			60		Ω	$V_{GS} = -5V$, $I_D = -10mA$
				45	75		$V_{GS} = -10V$, $I_D = -50mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	1.5	%/°C	$V_{GS} = -10V$, $I_D = -50mA$
G_{FS}	Forward Transconductance		50	70		m℧	$V_{DS} = -25V$, $I_D = -50mA$
C_{ISS}	Input Capacitance			40	60	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			11	20		
C_{RSS}	Reverse Transfer Capacitance			3	5		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$ $I_D = -200mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				15		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop			-0.8	-1.5	V	$V_{GS} = 0V$, $I_{SD} = -0.1A$
t_{rr}	Reverse Recovery Time			200		ns	$V_{GS} = 0V$, $I_{SD} = -0.1A$

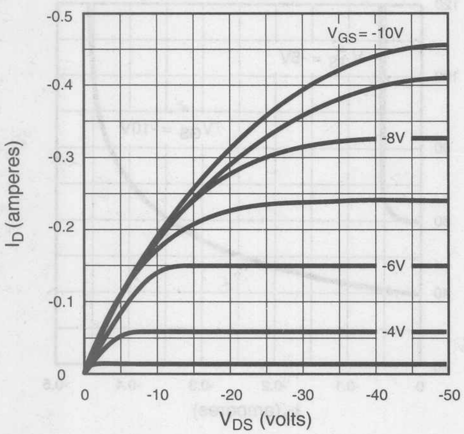
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

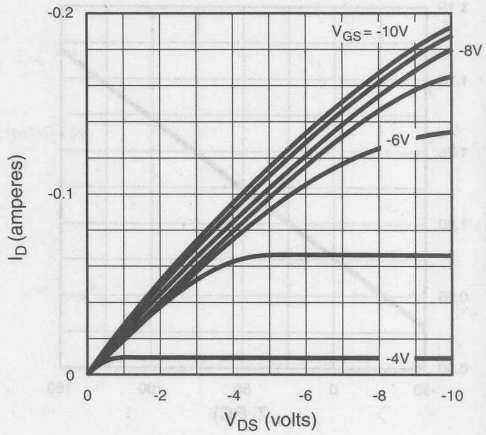


Typical Performance Curves

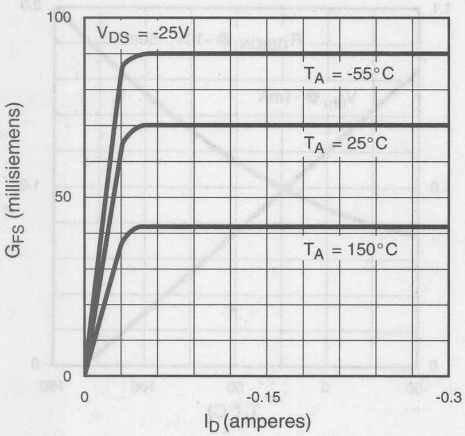
Output Characteristics



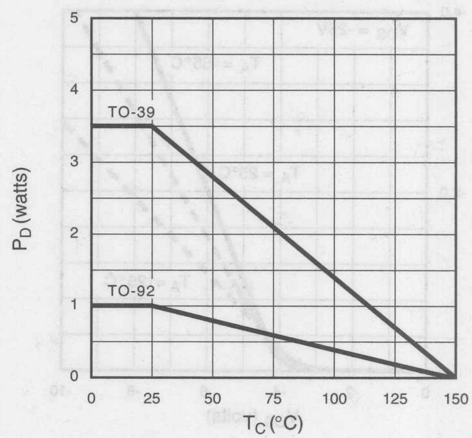
Saturation Characteristics



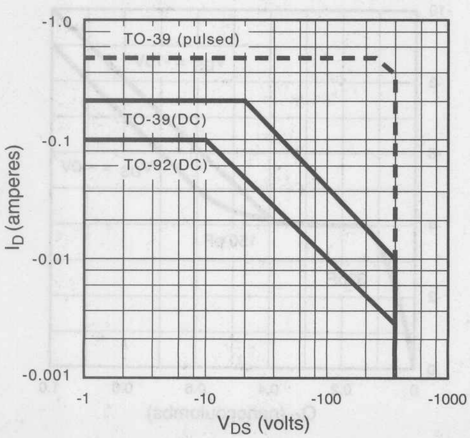
Transconductance vs. Drain Current



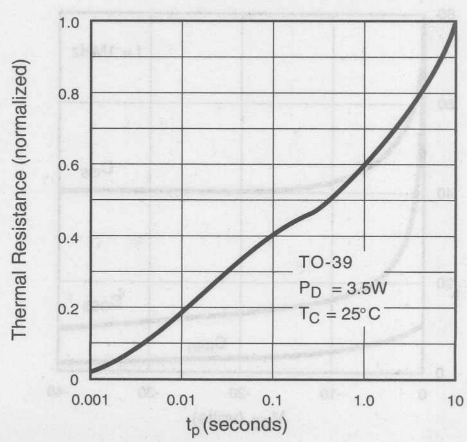
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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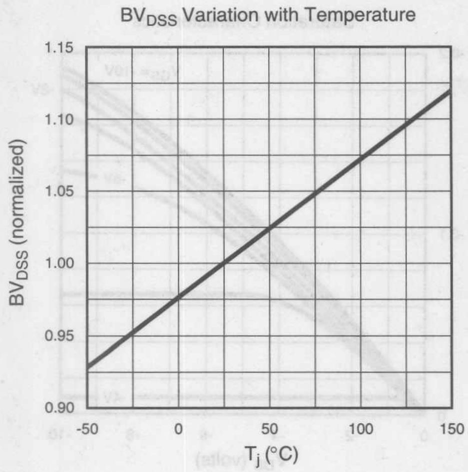
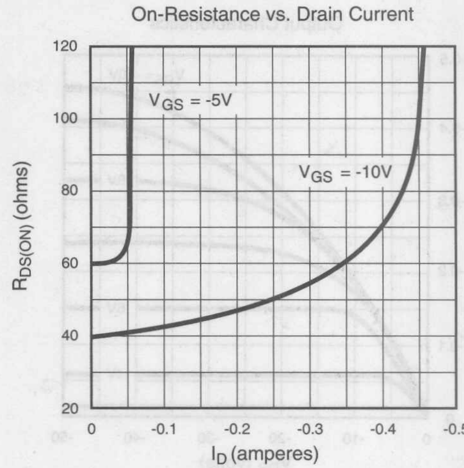
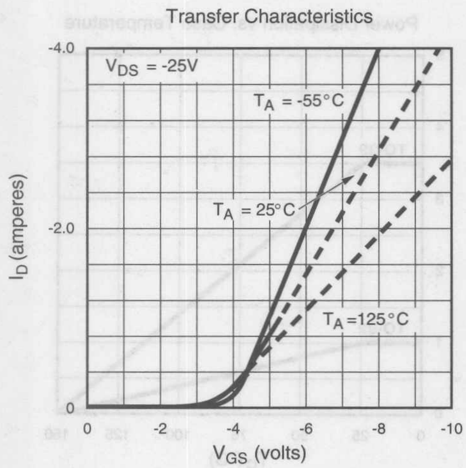
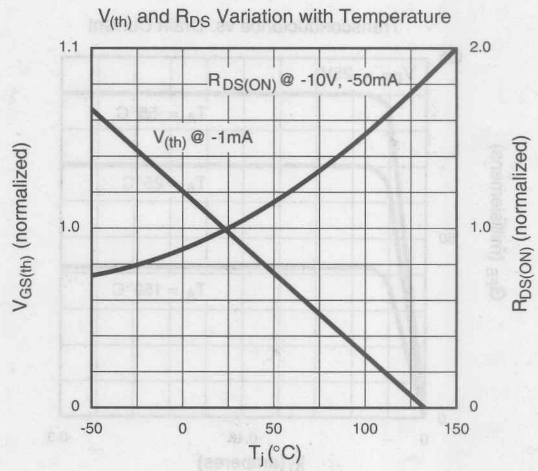
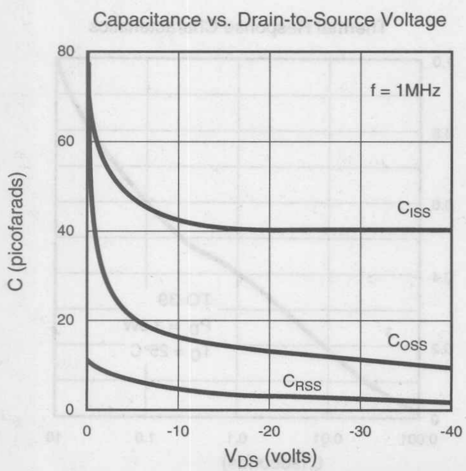
Typical Performance Curves

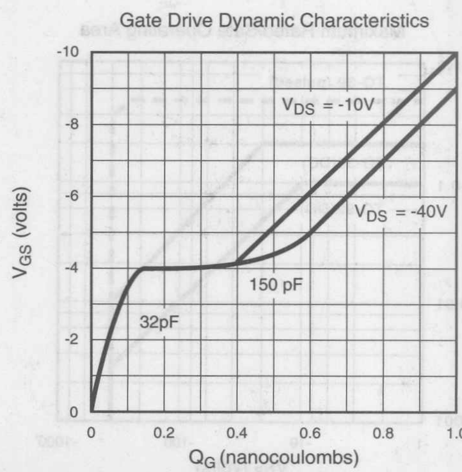












Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE†
-450V	125Ω	-100mA	VP0545N2	VP0545N3	VP0545ND
-500V	125Ω	-100mA	VP0550N2	VP0550N3	VP0550ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

TO-39 TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-125mA	-0.25A	3.5W	35	125	-125mA	-0.25A
TO-92	-70mA	-0.25A	1W	125	170	-70mA	-0.25A

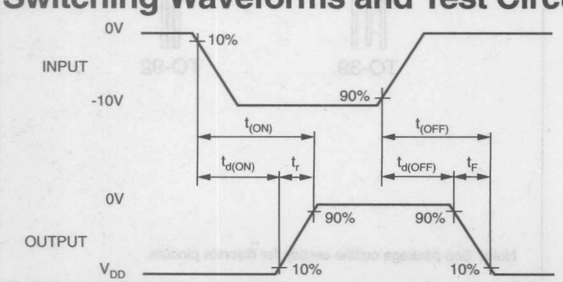
* I_D (continuous) is limited by max rated T_j.

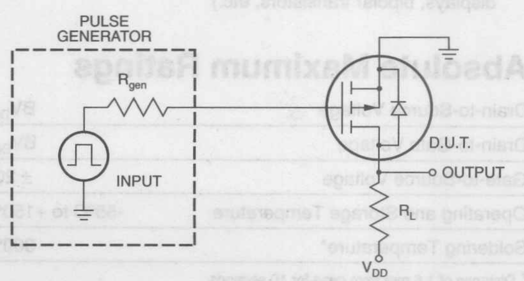
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0550	-500			V	$V_{GS} = 0V$, $I_D = -1mA$
		VP0545	-450				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			3.5	6	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-1000		$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			-90		mA	$V_{GS} = -5V$, $V_{DS} = -25V$
			-100	-240			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			85		Ω	$V_{GS} = -5V$, $I_D = -5mA$
				80	125		$V_{GS} = -10V$, $I_D = -10mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85		%/°C	$V_{GS} = -10V$, $I_D = -10mA$
G_{FS}	Forward Transconductance		25	40		m℧	$V_{DS} = -25V$, $I_D = -10mA$
C_{ISS}	Input Capacitance			40	60	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			10	20		
C_{RSS}	Reverse Transfer Capacitance			3	10		
$t_{d(ON)}$	Turn-ON Delay Time			5	10	ns	$V_{DD} = -25V$ $I_D = -100mA$ $R_{GEN} = 25Ω$
t_r	Rise Time			8	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			8	15		
t_f	Fall Time			5	16		
V_{SD}	Diode Forward Voltage Drop			-0.8	-1.5	V	$V_{GS} = 0V$, $I_{SD} = -0.1A$
t_{rr}	Reverse Recovery Time			200		ns	$V_{GS} = 0V$, $I_{SD} = -0.1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

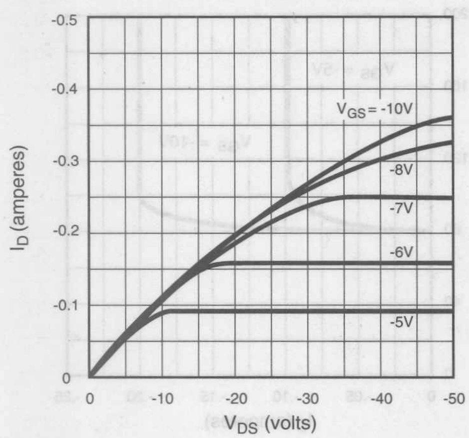
Switching Waveforms and Test Circuit



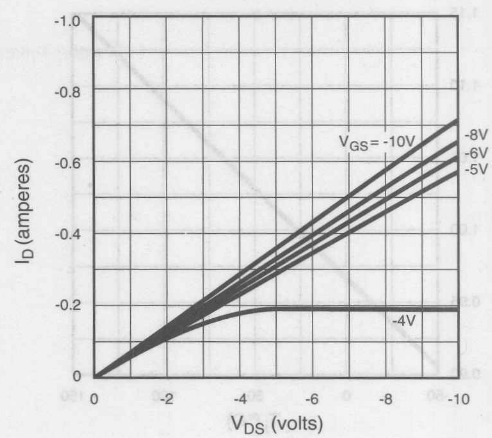


Typical Performance Curves

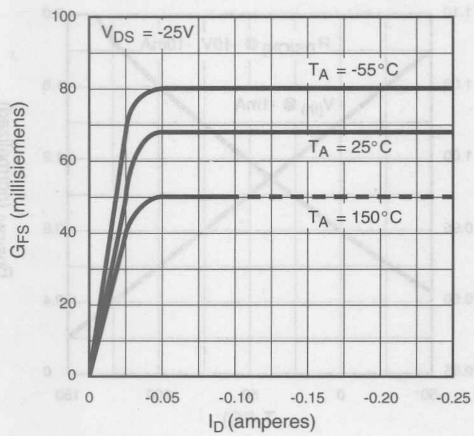
Output Characteristics



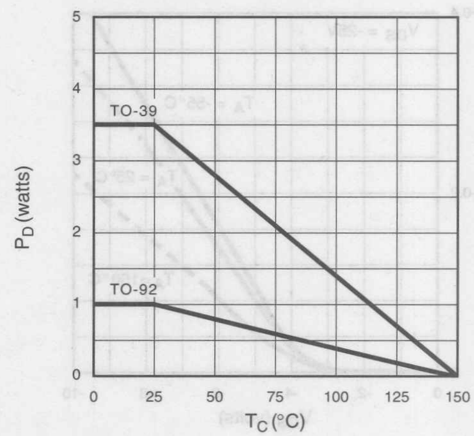
Saturation Characteristics



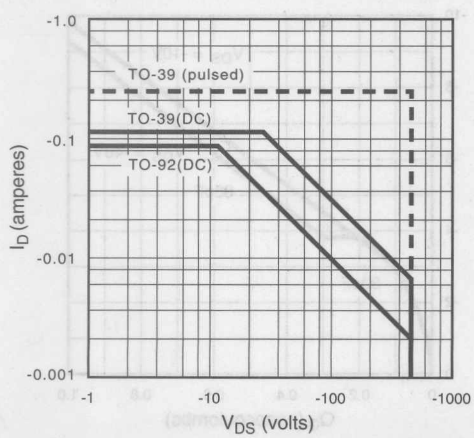
Transconductance vs. Drain Current



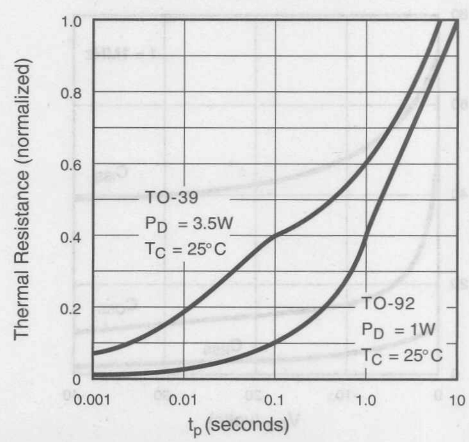
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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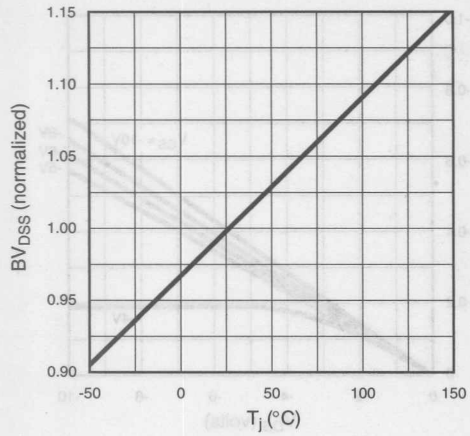
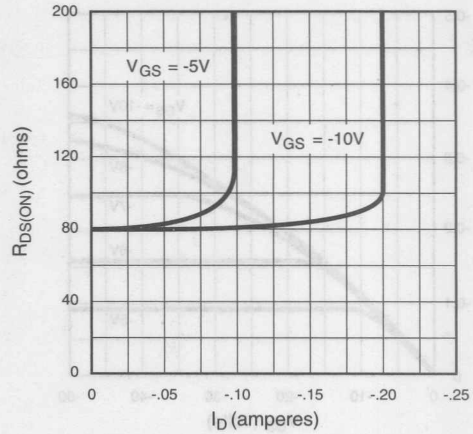
Typical Performance Curves

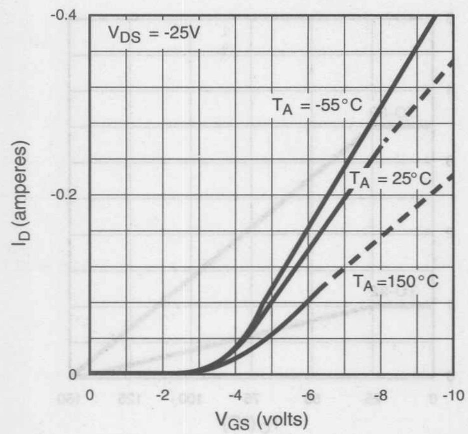
BV$_{DSS}$ Variation with Temperature



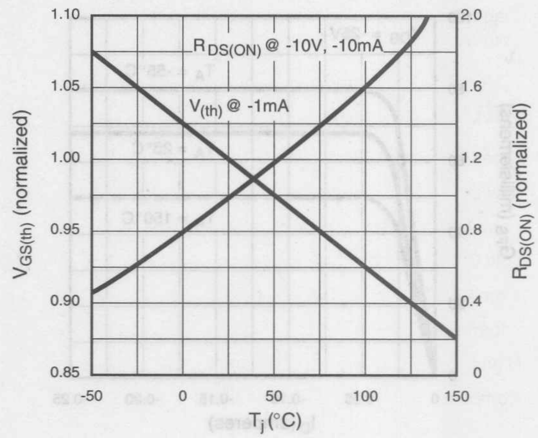
On-Resistance vs. Drain Current



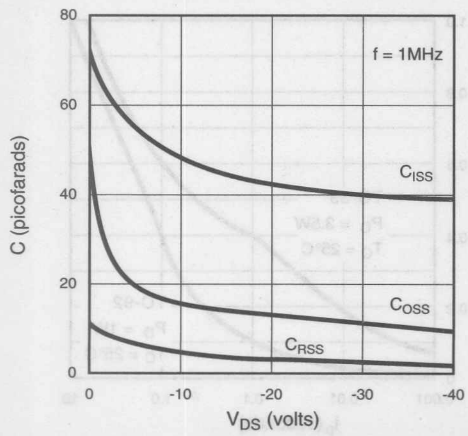
Transfer Characteristics



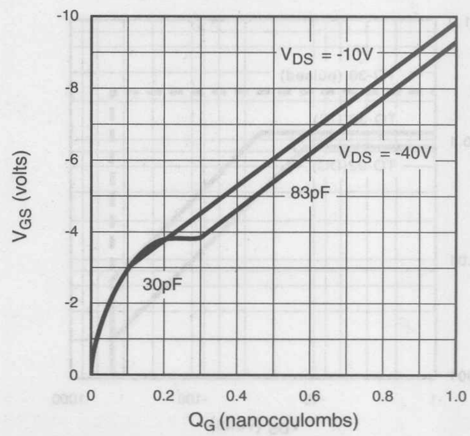
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92	TO-220	DICE†
-350V	25Ω	-0.4A	VP0635N2	VP0635N3	VP0635N5	VP0635ND
-400V	25Ω	-0.4A	VP0640N2	VP0640N3	VP0640N5	VP0640ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

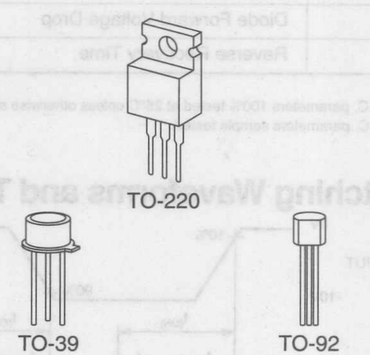
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.30A	-0.6A	1W	125	170	-0.30A	-0.6A
TO-39	-0.40A	-0.75A	6W	21	125	-0.40A	-0.75A
TO-220	-0.40A	-0.75A	28W	2.7	70	-0.40A	-0.75A

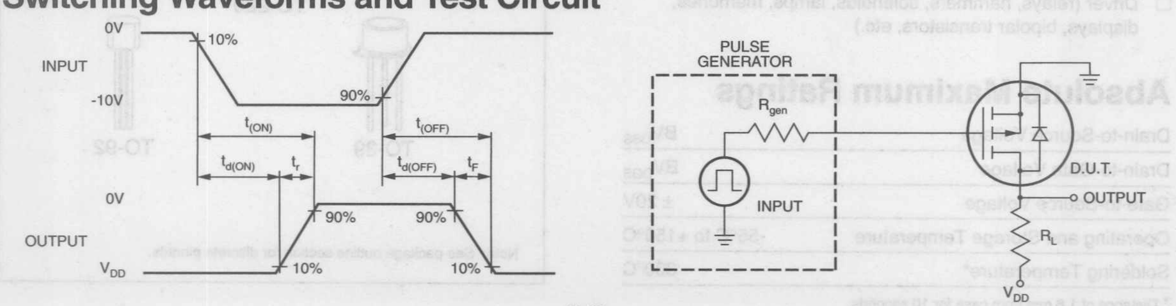
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

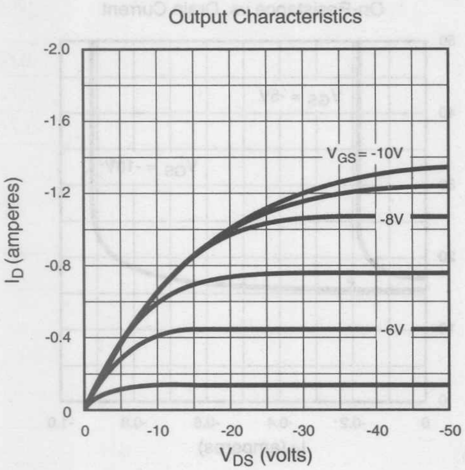
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0640	-400			V	$V_{GS} = 0V$, $I_D = -2mA$
		VP0635	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-2		-4	V	$V_{GS} = V_{DS}$, $I_D = -2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				4.8	mV/°C	$V_{GS} = V_{DS}$, $I_D = -2mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating, $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			-0.2		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-0.4	-1.1			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20		Ω	$V_{GS} = -5V$, $I_D = -100mA$
				19	25		$V_{GS} = -10V$, $I_D = -100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = -10V$, $I_D = -100mA$
G_{FS}	Forward Transconductance		100			m℧	$V_{DS} = -25V$, $I_D = -100mA$
C_{ISS}	Input Capacitance			105	145	pF	$V_{GS} = 0V$, $V_{DS} = -25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			30	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$, $I_D = -400mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0V$, $I_{SD} = -100mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0V$, $I_{SD} = -100mA$

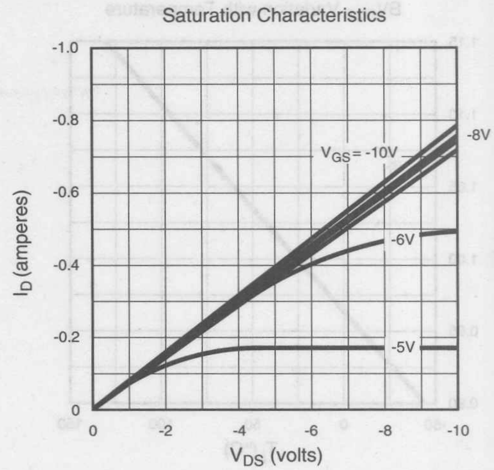
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300mµs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

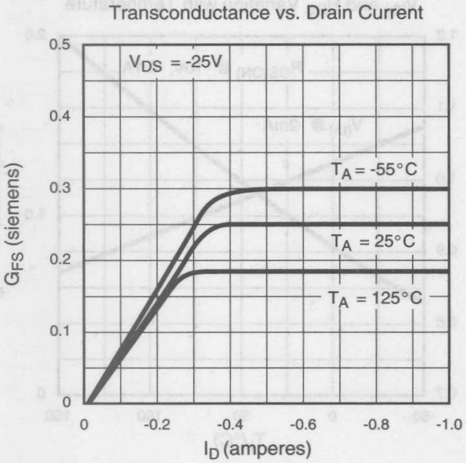
Switching Waveforms and Test Circuit

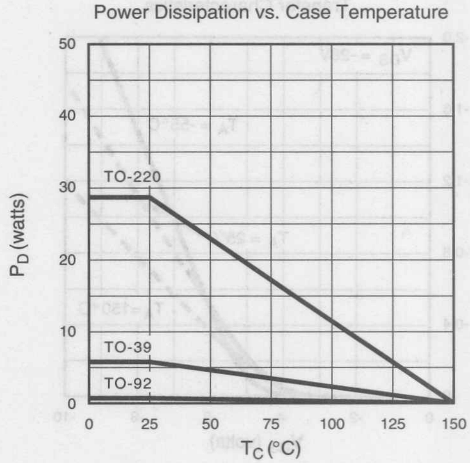


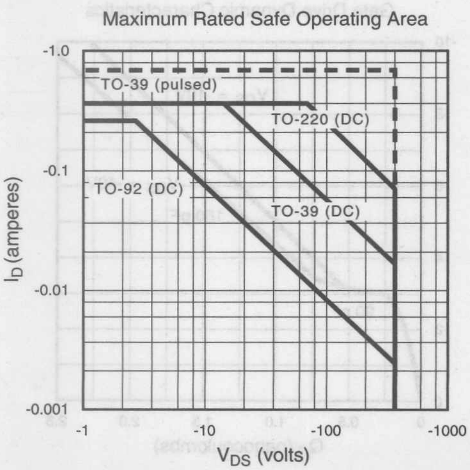
Typical Performance Curves

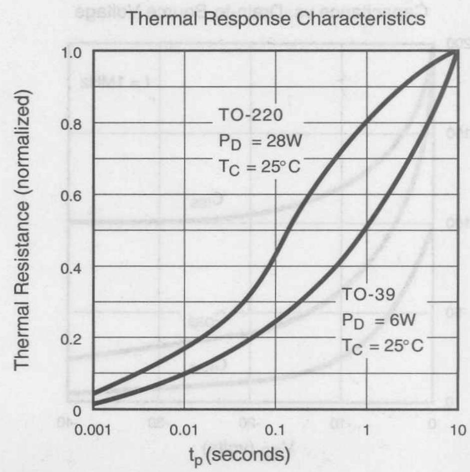




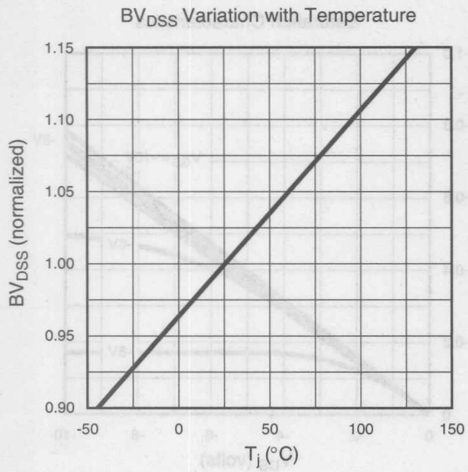


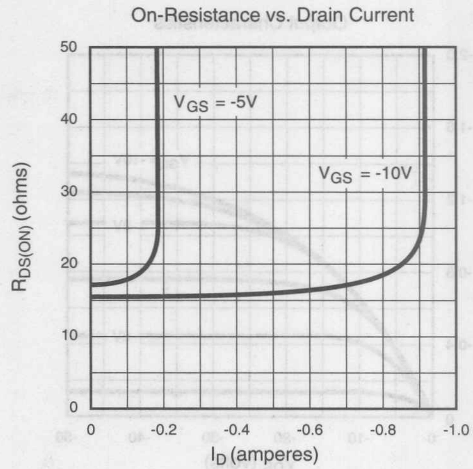


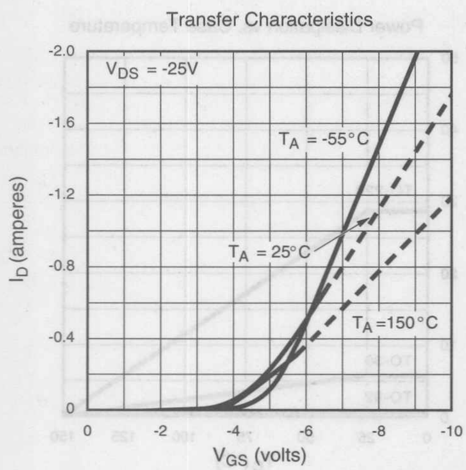


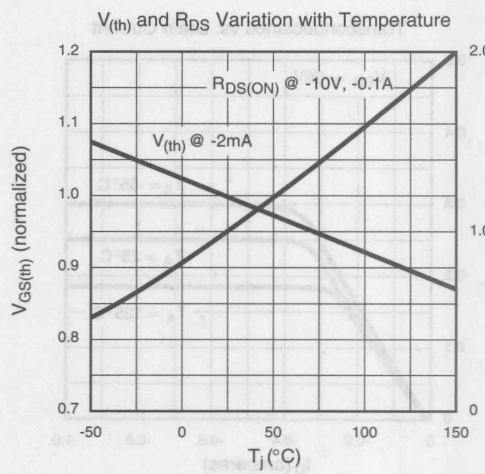


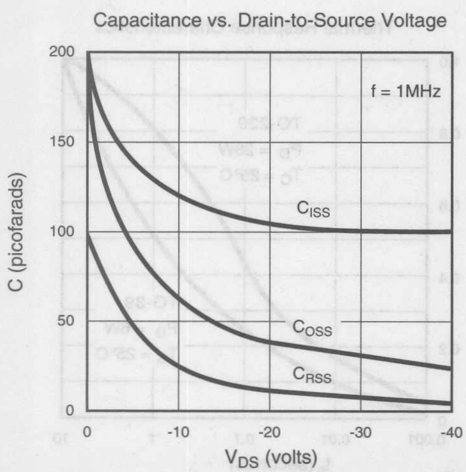
Typical Performance Curves

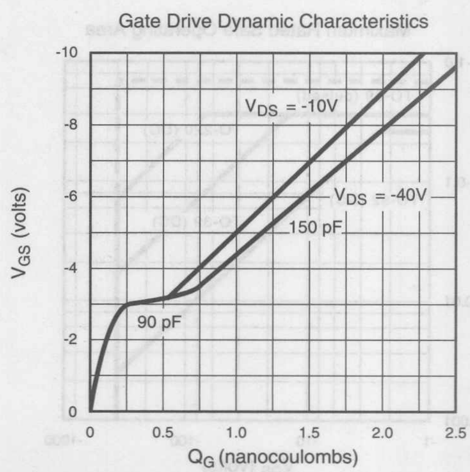












Supertex inc.

VP06E

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-39	TO-92	TO-220	DICE†
-450V	30Ω	-0.2A	VP0645N2	VP0645N3	VP0645N5	VP0645ND
-500V	30Ω	-0.2A	VP0650N2	VP0650N3	VP0650N5	VP0650ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

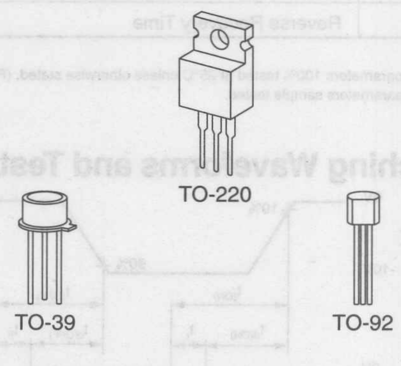
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.1A	-0.3A	1W	125	170	-0.1A	-0.3A
TO-39	-0.25A	-0.5A	6W	21	125	-0.25A	-0.5A
TO-220	-0.25A	-0.5A	45W	2.7	70	-0.25A	-0.5A

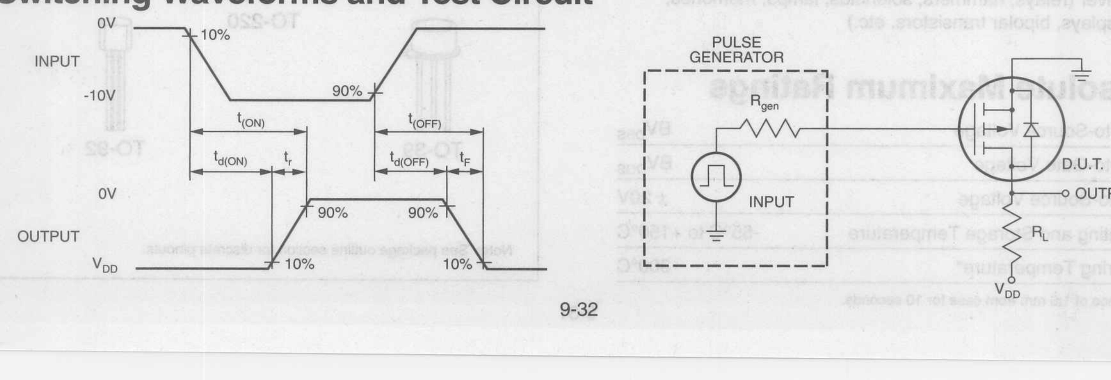
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0650	-500			V	$V_{GS} = 0V$, $I_D = -2mA$
		VP0645	-450				
$V_{GS(th)}$	Gate Threshold Voltage		-2		-4	V	$V_{GS} = V_{DS}$, $I_D = -2mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.8	mV/°C	$V_{GS} = V_{DS}$, $I_D = -2mA$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current			-200		mA	$V_{GS} = -5V$, $V_{DS} = -25V$
			-200	-700			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			27		Ω	$V_{GS} = -5V$, $I_D = -100mA$
				22	30		$V_{GS} = -10V$, $I_D = -100mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	$V_{GS} = -10V$, $I_D = -100mA$
G_{FS}	Forward Transconductance		50	125		m℧	$V_{DS} = -25V$, $I_D = -100mA$
C_{ISS}	Input Capacitance			95	130	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	$V_{DD} = -25V$ $I_D = -200mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	$V_{GS} = 0V$, $I_{SD} = -50mA$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0V$, $I_{SD} = -50mA$

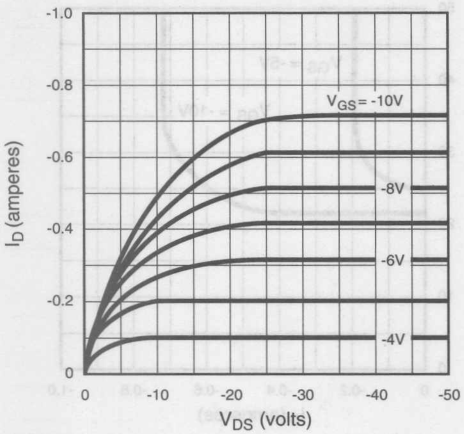
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

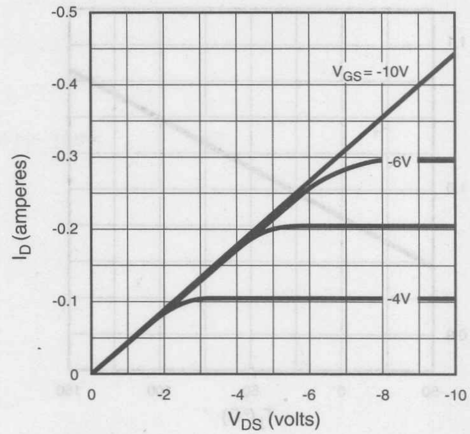


Typical Performance Curves

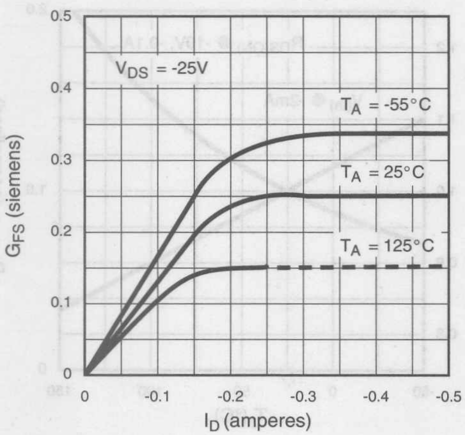
Output Characteristics



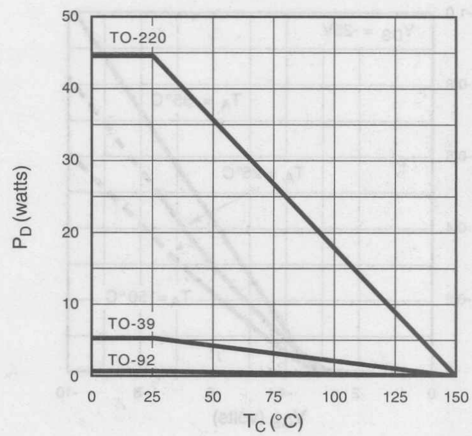
Saturation Characteristics



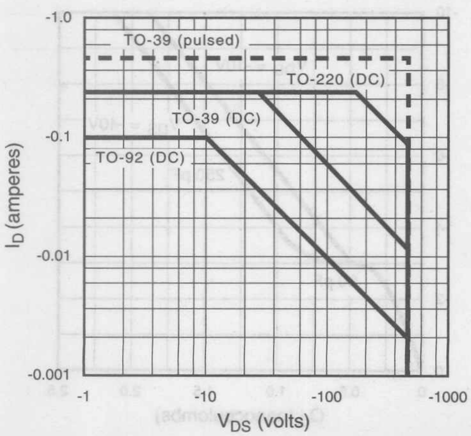
Transconductance vs. Drain Current



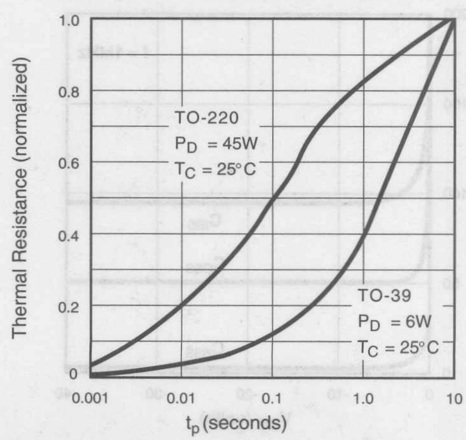
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



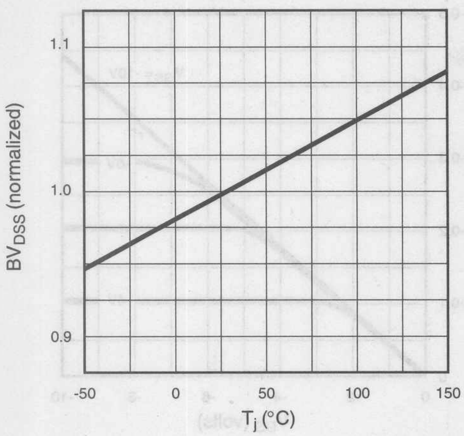
Thermal Response Characteristics



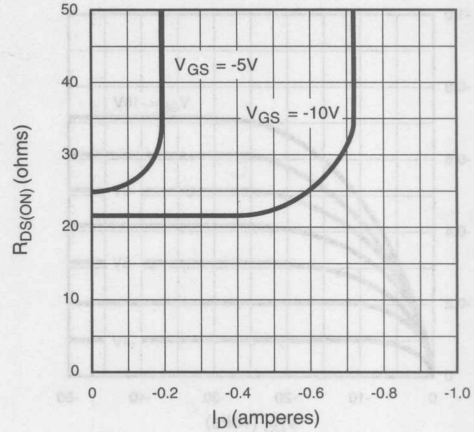
9

Typical Performance Curves

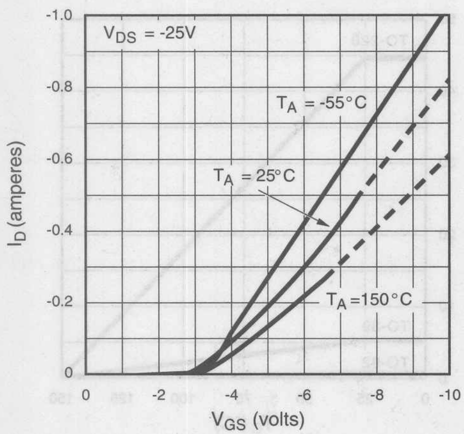
BV$_{DSS}$ Variation with Temperature



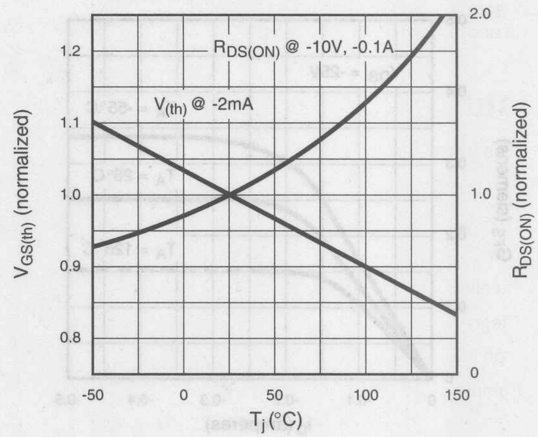
On-Resistance vs. Drain Current



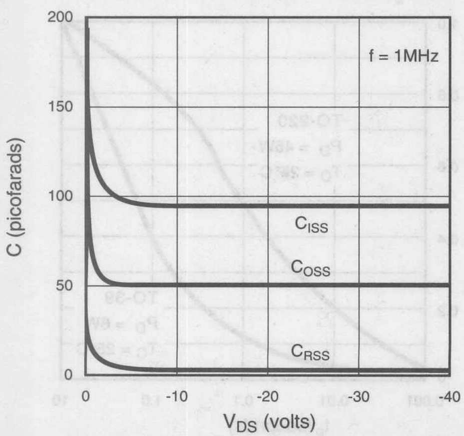
Transfer Characteristics



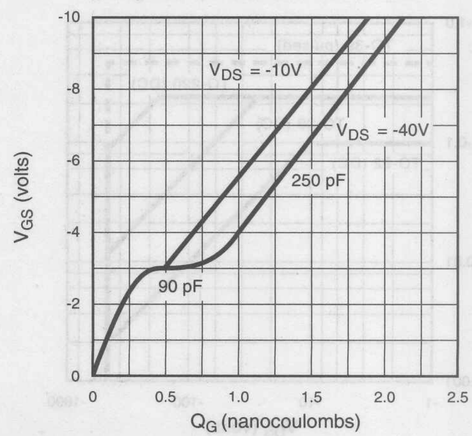
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

VP0808
VP1008

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
-80V	5Ω	-1.1A	VP0808B	VP0808L
-100V	5Ω	-1.1A	VP1008B	VP1008L

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

Note: See package outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation	θ_{ja} °C/W	θ_{jc} °C/W
TO-39	-0.88A	-3A	6.25W	125	20
TO-92	-0.28A	-3A	0.4W	170	125

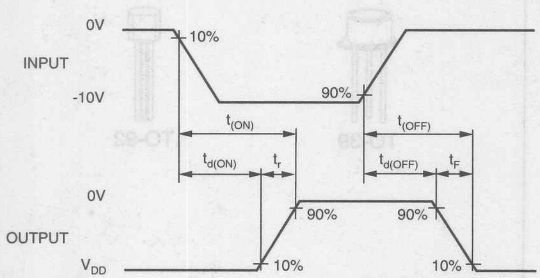
* I_D (continuous) is limited by max rated T_j.

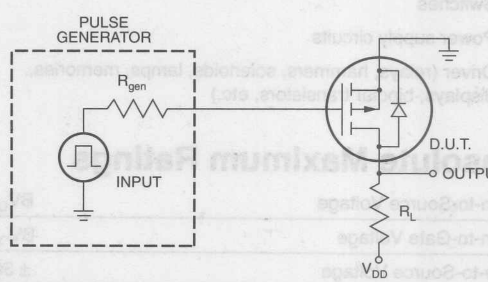
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1008	-100			V	V_{GS}= 0V, I_D = -10μA
		VP8080	-80				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-4.5	V	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = 30V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				-10		V_{GS} = 0V, V_{DS} = Max Rating
					-500	μA	V_{GS} = 0V, V_{DS} = Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-1.1			A	V_{GS} = -10V, V_{DS} = -15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance				5	Ω	V_{GS} = -10V, I_D = -1A
G_{FS}	Forward Transconductance		200			m℧	V_{DS} = -10V, I_D = -0.5A
C_{ISS}	Input Capacitance				150		
C_{OSS}	Common Source Output Capacitance				60	pF	V_{GS} = 0V, V_{DS} = -25V f = 1MHz
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				15		
t_r	Rise Time				40		V_{DD} = -25V, I_D = -0.5A R_{GEN} = 25Ω
$t_{d(OFF)}$	Turn-OFF Time				30	ns	
t_f	Fall Time				30		
V_{SD}	Diode Forward Voltage Drop	VP1008		-1.2		V	V_{GS} = 0V, I_{SD} = -0.21A
		VP0808		-1.2			V_{GS} = 0V, I_{SD} = -0.9A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-220	DICE†
-60V	2Ω	-5A	VP1106N2	VP1106N5	VP1106ND
-100V	2Ω	-5A	VP1110N2	VP1110N5	VP1110ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

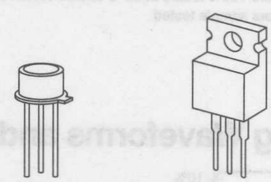
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39 TO-220

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	-1.5A	-7A	6W	125	20.8	-1.5A	-7A
TO-220	-4.0A	-12A	45W	70	2.78	-4A	-12A

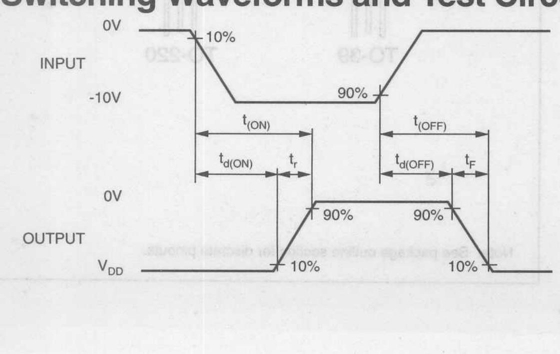
* I_D (continuous) is limited by max rated T_j.

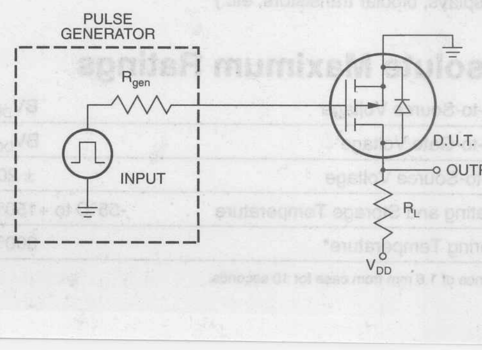
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1110	-100			V	$I_D = -5mA$, $V_{GS} = 0V$
		VP1106	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -5mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.0		mV/°C	$I_D = -5mA$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-50	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-5	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-1.0			A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-5.0				$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.7	5	Ω	$V_{GS} = -5V$, $I_D = -0.5A$
				1.5	2		$V_{GS} = -10V$, $I_D = -2.0A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.7	1.0	%/°C	$I_D = -1.0A$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		0.9	1.3		℧	$V_{DS} = -25V$, $I_D = -2.0A$
C_{ISS}	Input Capacitance			300	350	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			125	150		
C_{RSS}	Reverse Transfer Capacitance			20	35		
$t_{d(ON)}$	Turn-ON Delay Time			35	40	ns	$V_{DD} = -25V$ $I_D = -2.0A$ $R_{GEN} = 10\Omega$
t_r	Rise Time			20	30		
$t_{d(OFF)}$	Turn-OFF Delay Time			40	50		
t_f	Fall Time			10	20		
V_{SD}	Diode Forward Voltage Drop			-1.4	-2.5	V	$I_{SD} = -1.0A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			400		ns	$I_{SD} = -1.0A$, $V_{GS} = 0V$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

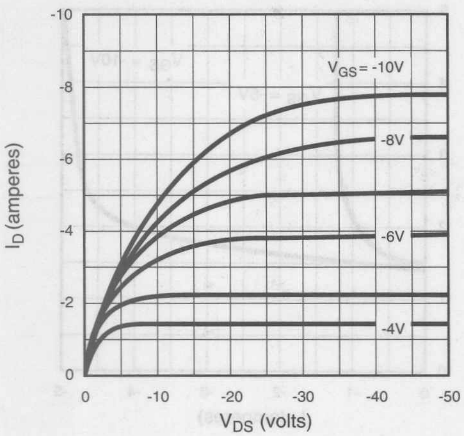
Switching Waveforms and Test Circuit



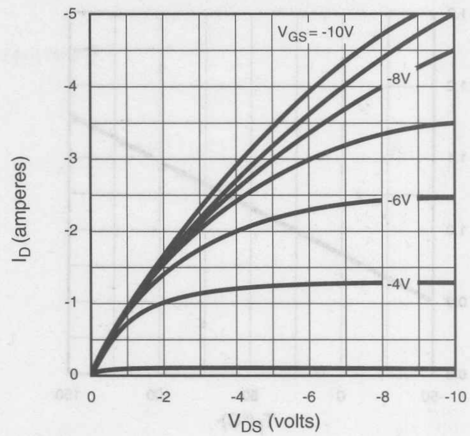


Typical Performance Curves

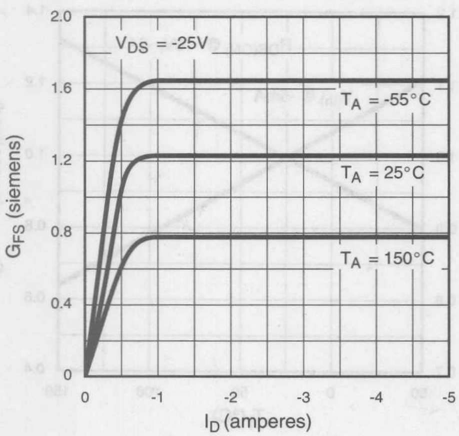
Output Characteristics



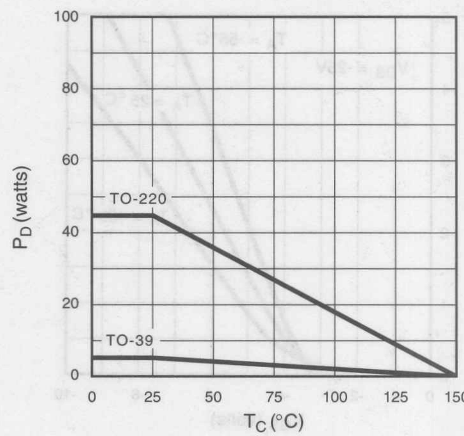
Saturation Characteristics



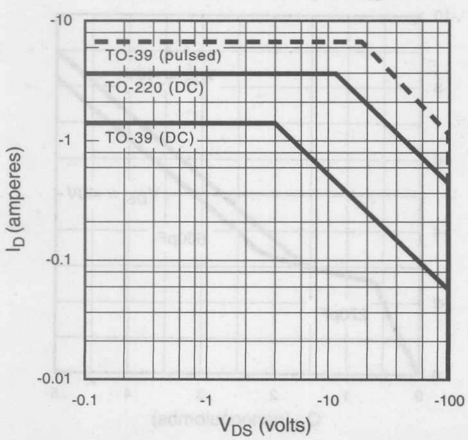
Transconductance vs. Drain Current



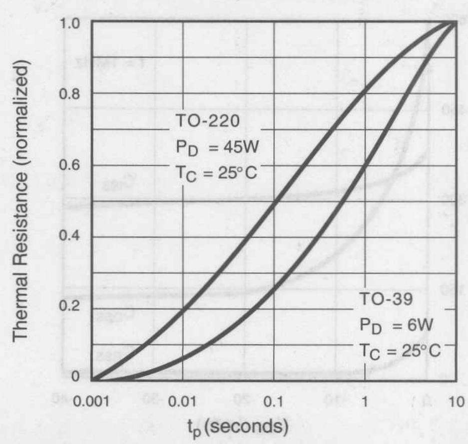
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

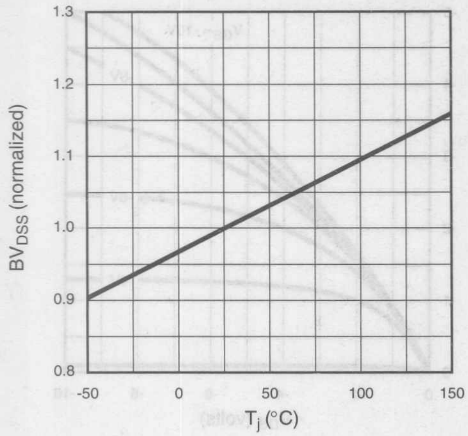


Thermal Response Characteristics

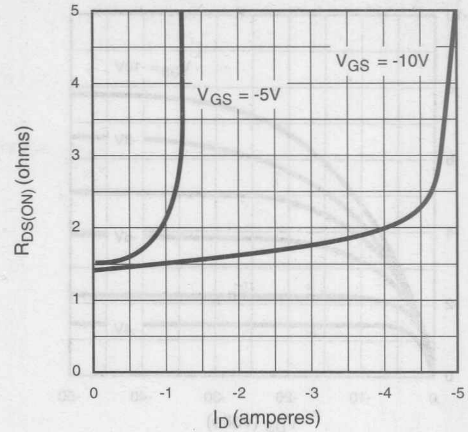


Typical Performance Curves

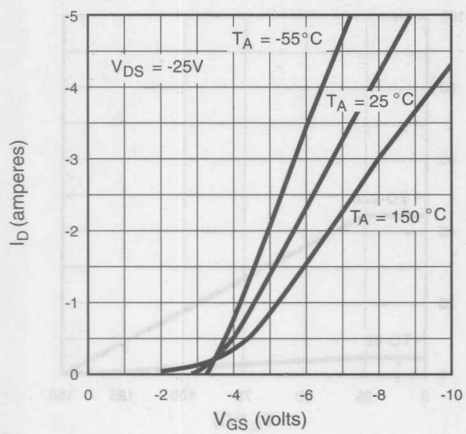
BV_{DSS} Variation with Temperature



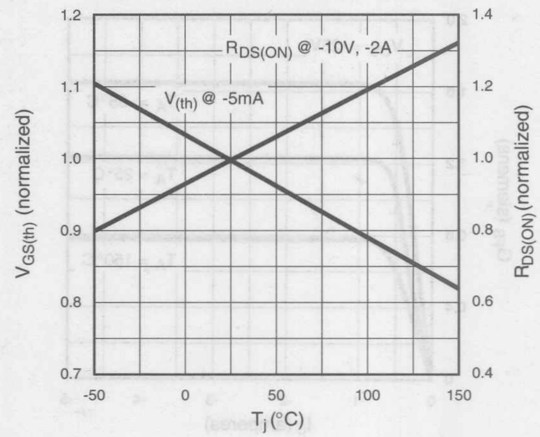
On-Resistance vs. Drain Current



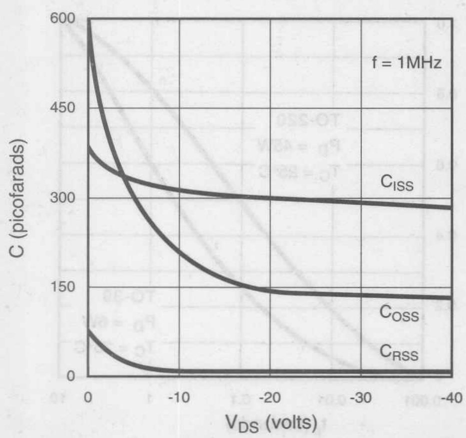
Transfer Characteristics



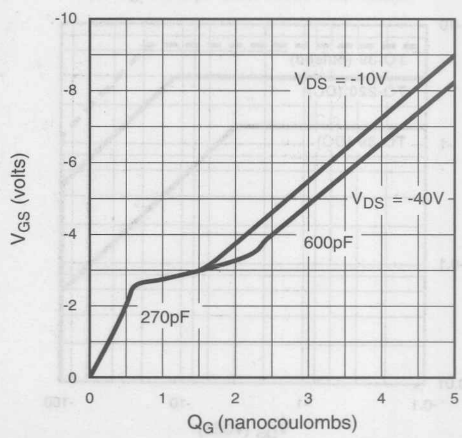
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-220	DICE†
-40V	0.8Ω	-6A	VP1204N2	VP1204N5	VP1204ND
-60V	0.8Ω	-6A	VP1206N2	VP1206N5	VP1206ND
-100V	0.8Ω	-6A	VP1210N2	VP1210N5	VP1210ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

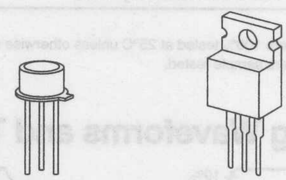
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	-2.5A	-11A	6.5W	125	20	-2.5A	-11A
TO-220	-5.0A	-14A	45W	70	2.75	-5A	-14A

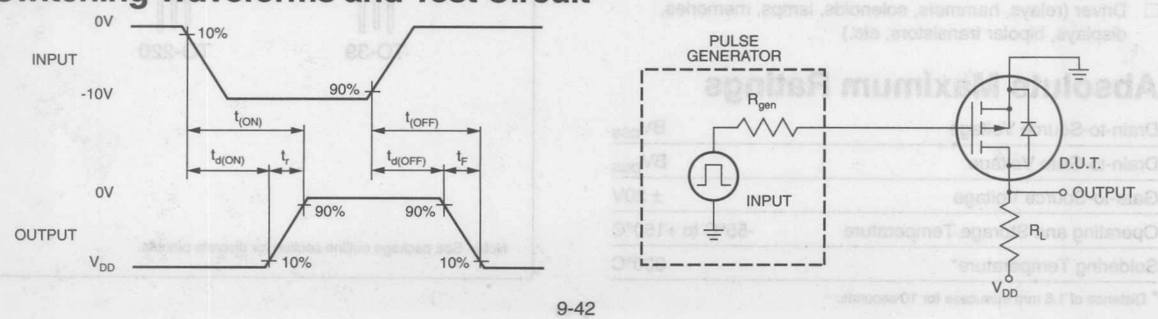
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1210	-100			V	$I_D = -10mA$, $V_{GS} = 0V$
		VP1206	-60				
		VP1204	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.7	5.5	mV/°C	$I_D = -10mA$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-100	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-10	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-1.5	-3.0		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-6.0	-14.0			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.0	1.4	Ω	$V_{GS} = -5V$, $I_D = -1A$
				0.5	0.8		$V_{GS} = -10V$, $I_D = -3A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	1.5	%/°C	$I_D = -3A$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		1	2		℧	$V_{DS} = -25V$, $I_D = -3A$
C_{ISS}	Input Capacitance			550	650	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			250	350		
C_{RSS}	Reverse Transfer Capacitance			50	65		
$t_{d(ON)}$	Turn-ON Delay Time			10	30	ns	$V_{DD} = -25V$ $I_D = -4A$ $R_{GEN} = 10\Omega$
t_r	Rise Time			17	40		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	105		
t_f	Fall Time			35	60		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.6	V	$I_{SD} = -5A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			500		ns	$I_{SD} = -1A$, $V_{GS} = 0V$

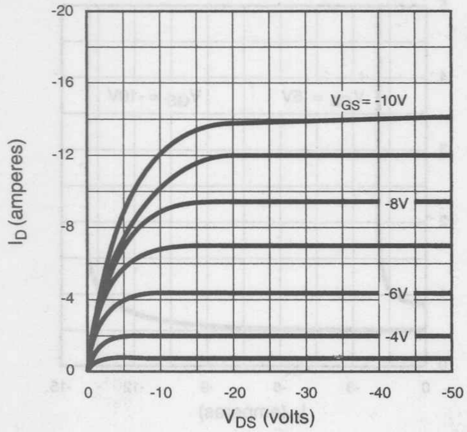
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

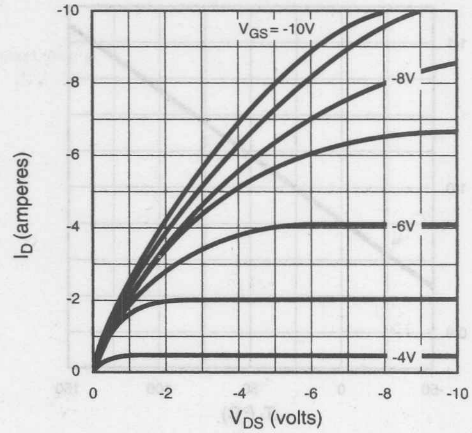


Typical Performance Curves

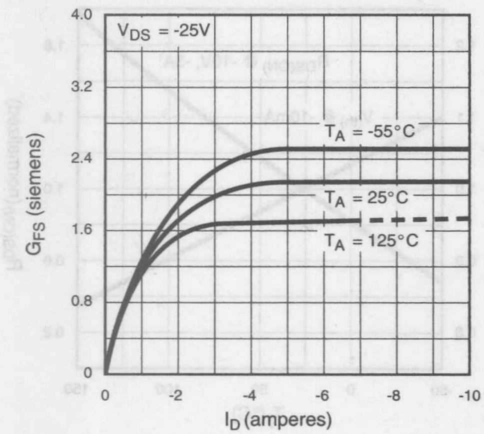
Output Characteristics



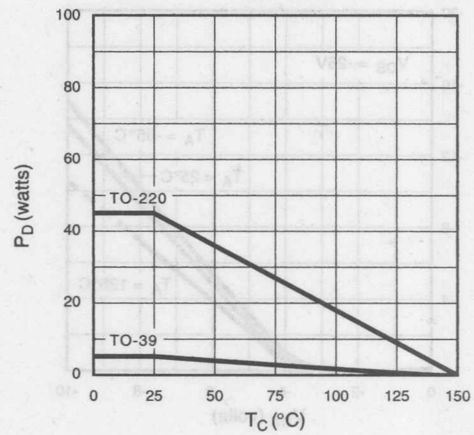
Saturation Characteristics



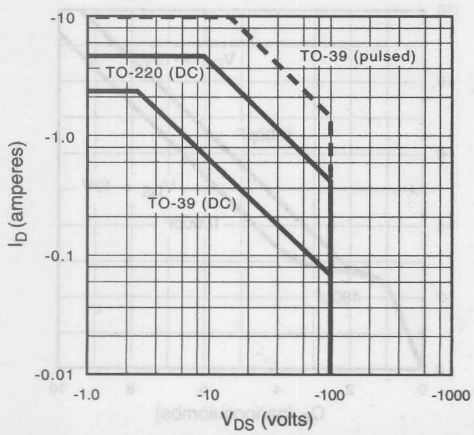
Transconductance vs. Drain Current



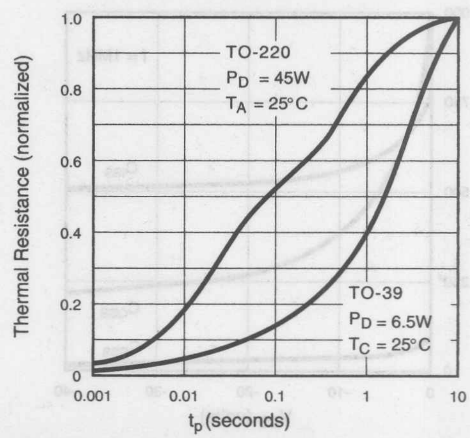
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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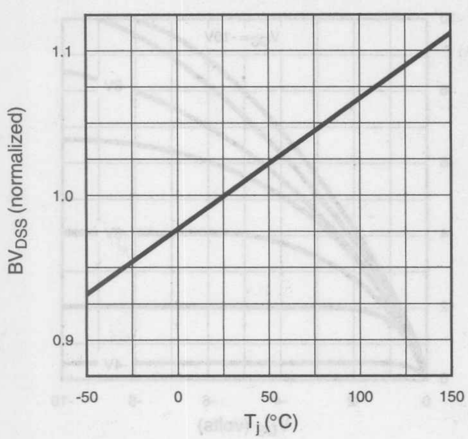
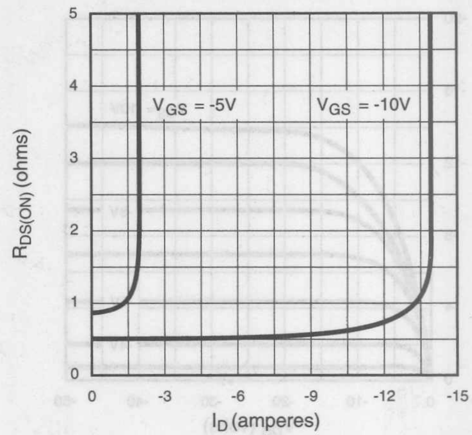
Typical Performance Curves

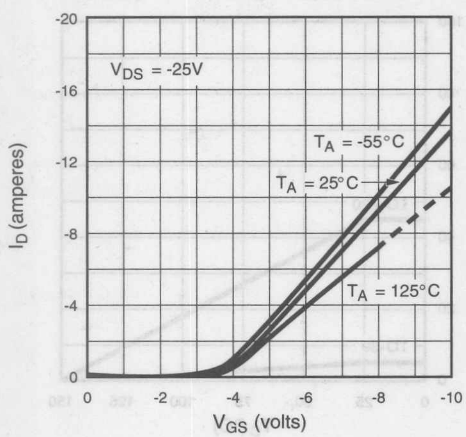
BV_{DSS} Variation with Temperature



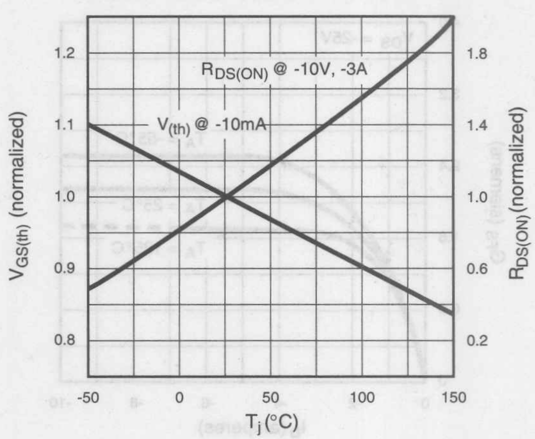
On-Resistance vs. Drain Current



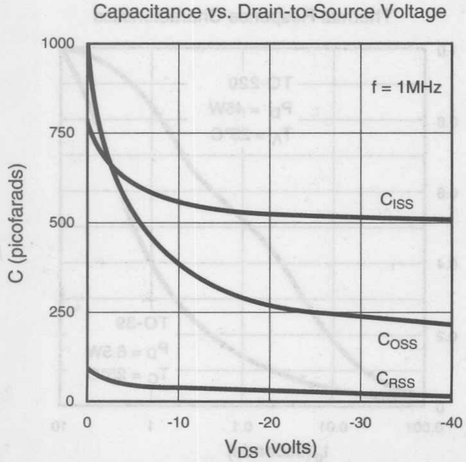
Transfer Characteristics



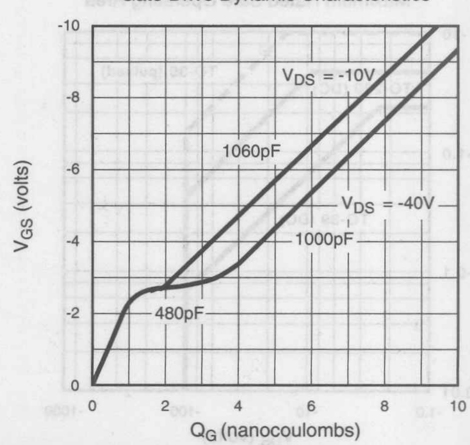
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92
-40V	25Ω	-0.25A	VP1304N2	VP1304N3
-60V	25Ω	-0.25A	VP1306N2	VP1306N3
-100V	25Ω	-0.25A	VP1310N2	VP1310N3

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{iss} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

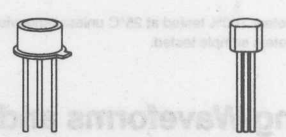
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39 TO-92

Note: See package outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.25A	-0.8A	3.0W	125	41	-0.25A	-0.8A
TO-92	-0.15A	-0.65A	0.8W	170	155	-0.15A	-0.65A

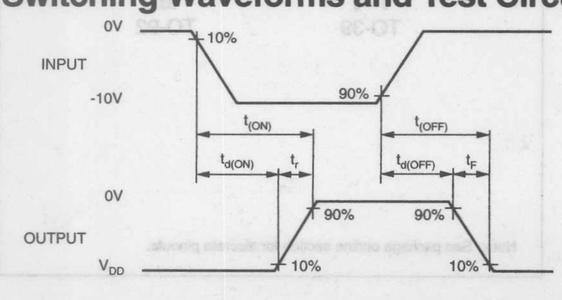
* I_D (continuous) is limited by max rated T_j.

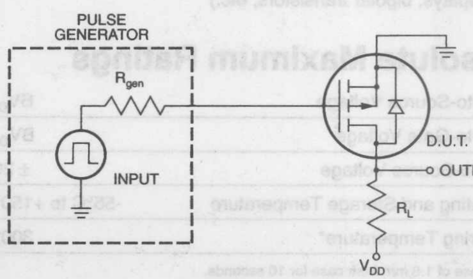
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1310	-100			V	$I_D = -1mA$, $V_{GS} = 0V$
		VP1306	-60				
		VP1304	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.2	-3.85	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage			-0.1	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	μA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-500		$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-.08	-0.23		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-0.25	-0.7			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			32	40	Ω	$V_{GS} = -5V$, $I_D = -50mA$
				19	25		$V_{GS} = -10V$, $I_D = -250mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	1.1	%/°C	$I_D = -250mA$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		75	120		m℧	$V_{DS} = -25V$, $I_D = -200mA$
C_{ISS}	Input Capacitance			20	35	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			12	15		
C_{RSS}	Reverse Transfer Capacitance			3	5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = -25V$ $I_D = -250mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time			3	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	5		
t_f	Fall Time			3	8		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.7	V	$I_{SD} = -1A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			350		ns	$I_{SD} = -1A$, $V_{GS} = 0V$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

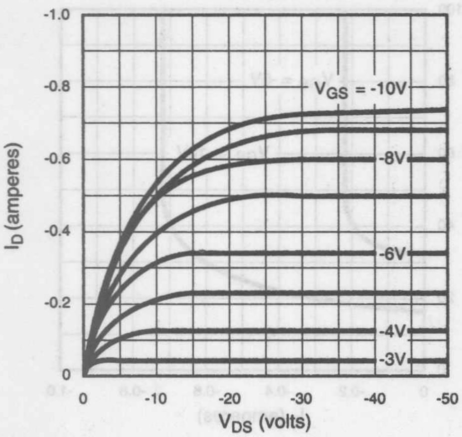
Switching Waveforms and Test Circuit



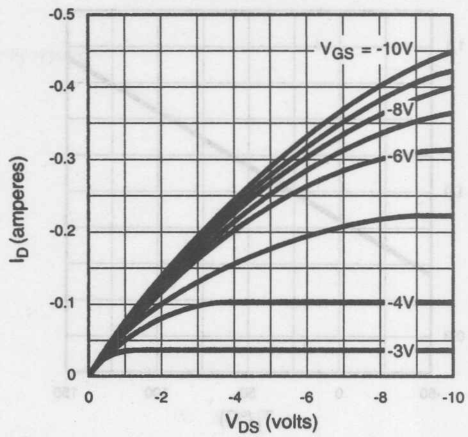


Typical Performance Curves

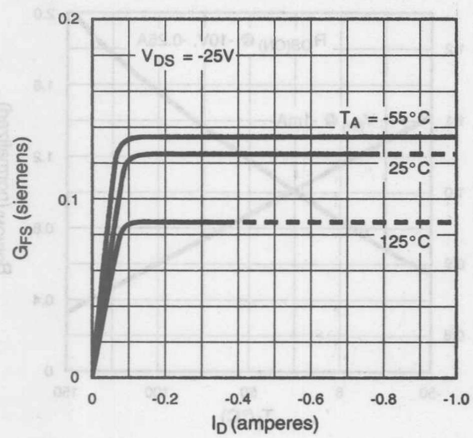
Output Characteristics



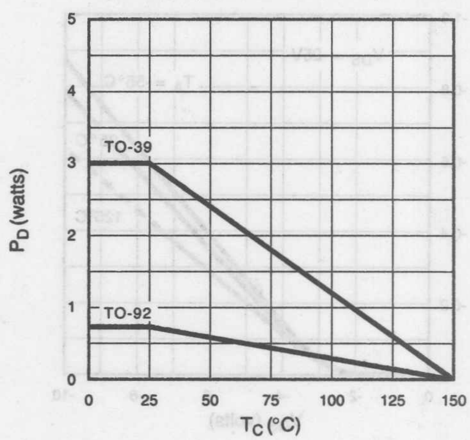
Saturation Characteristics



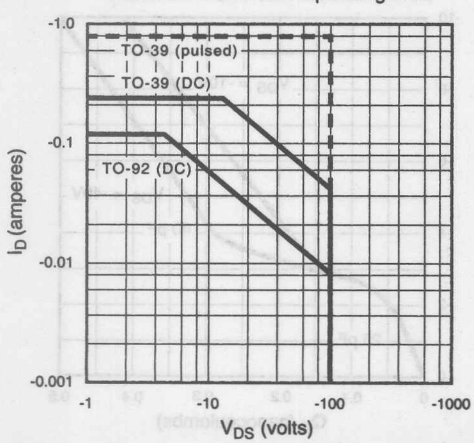
Transconductance vs. Drain Current



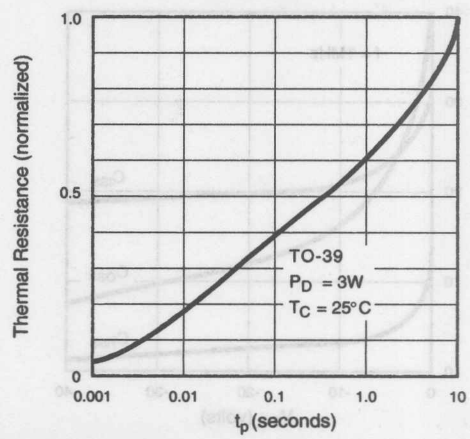
Power Dissipation vs. Case Temperature



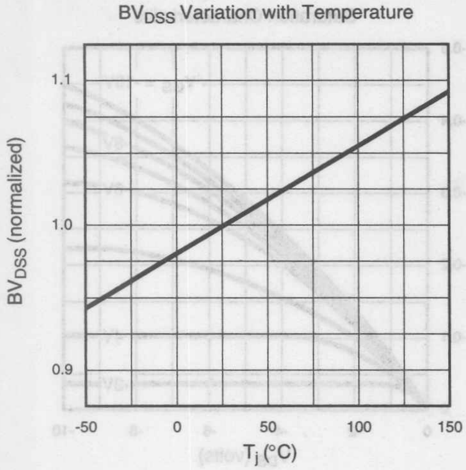
Maximum Rated Safe Operating Area

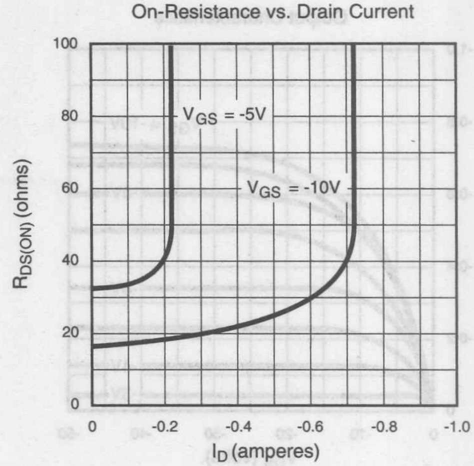


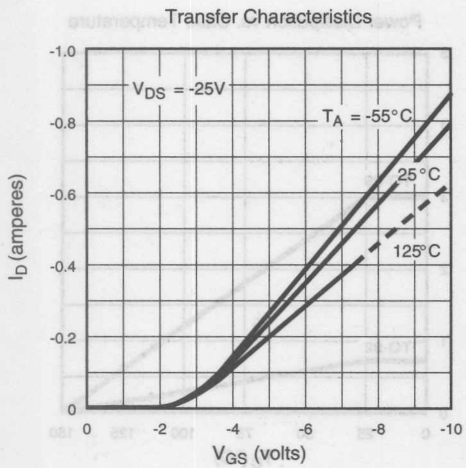
Thermal Response Characteristics

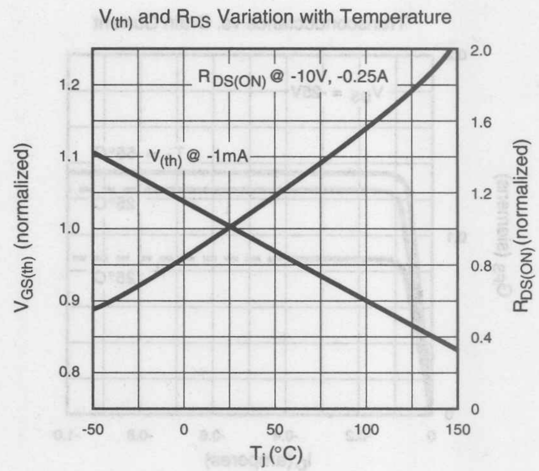


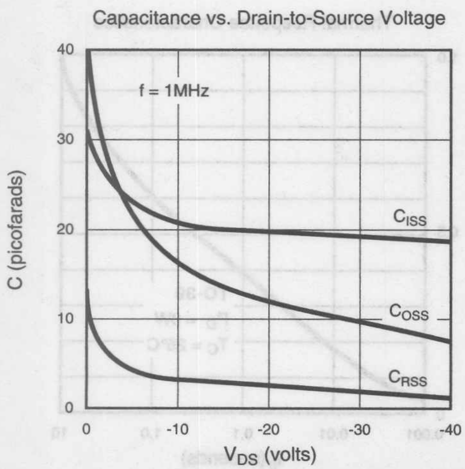
Typical Performance Curves

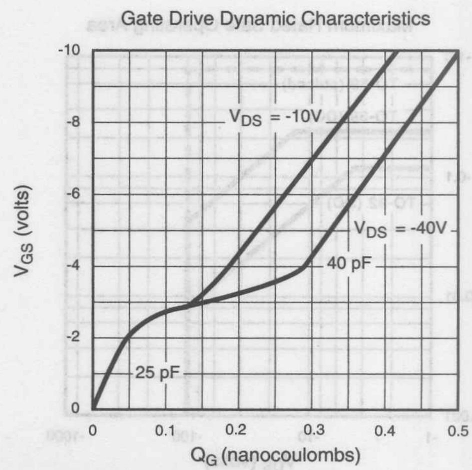












Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-92	DICE†
-40V	12Ω	-0.5A	VP2104N3	VP2104ND
-60V	12Ω	-0.5A	VP2106N3	VP2106ND
-100V	12Ω	-0.5A	VP2110N3	VP2110ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{iss} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

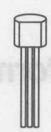
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-92

Note: See package outline section for discrete pinouts.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.25A	-0.8A	1.0W	170	125	-0.25A	-0.8A

* I_D (continuous) is limited by max rated T_j.

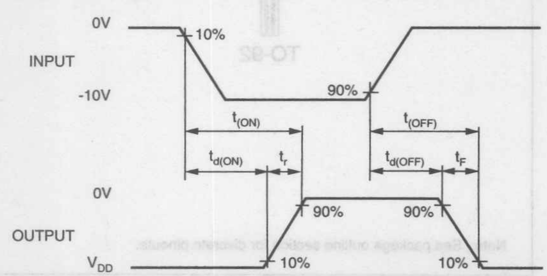
Electrical Characteristics (@ 25°C unless otherwise specified)

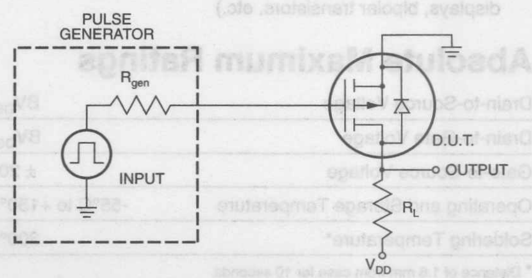
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP2110	-100			V	$I_D = -1.0mA$, $V_{GS} = 0V$
		VP2106	-60				
		VP2104	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			5.8	6.5	mV/°C	$I_D = -1.0mA$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage			-1.0	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-0.15	-0.25		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-0.50	-1.0			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			11	15	Ω	$V_{GS} = -5V$, $I_D = -0.1A$
				9	12		$V_{GS} = -10V$, $I_D = -0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/°C	$I_D = -0.5A$, $V_{GS} = -10V$
G_{FS}	Forward Transconductance		150	200		m℧	$V_{DS} = -25V$, $I_D = -0.5A$
C_{ISS}	Input Capacitance			45	60	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			22	30		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	5	ns	$V_{DD} = -25V$ $I_D = -0.5A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			5	9		
t_f	Fall Time			4	8		
V_{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	$I_{SD} = -0.5A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			400		ns	$I_{SD} = -1.0A$, $V_{GS} = 0V$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

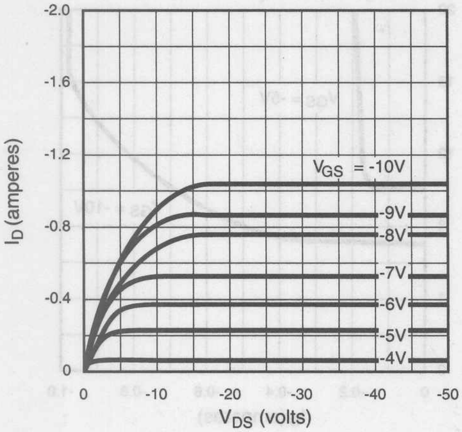
Switching Waveforms and Test Circuit



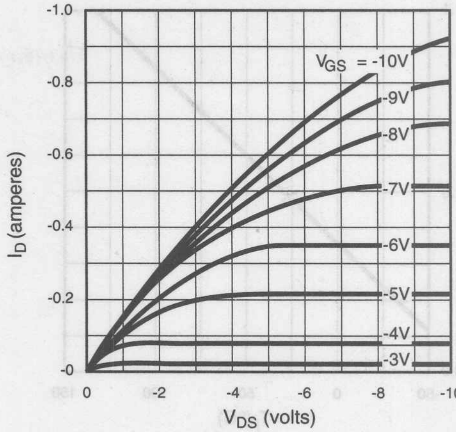


Typical Performance Curves

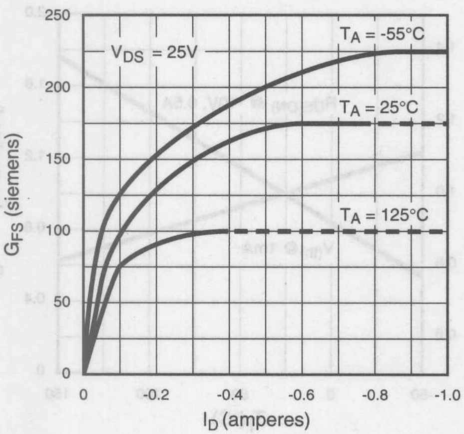
Output Characteristics



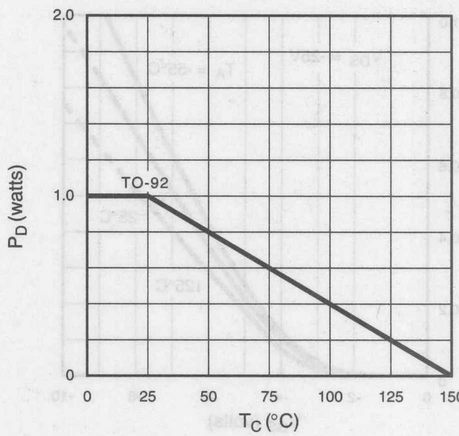
Saturation Characteristics



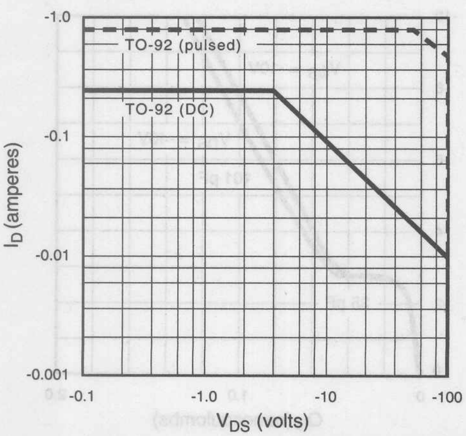
Transconductance vs. Drain Current



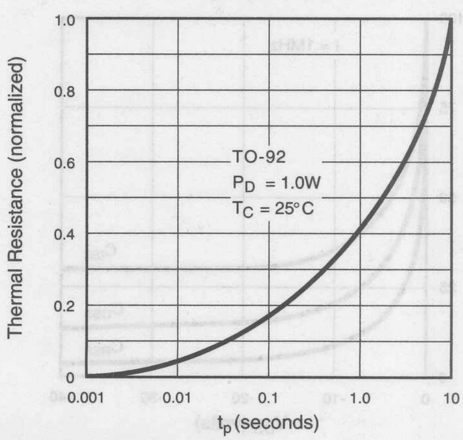
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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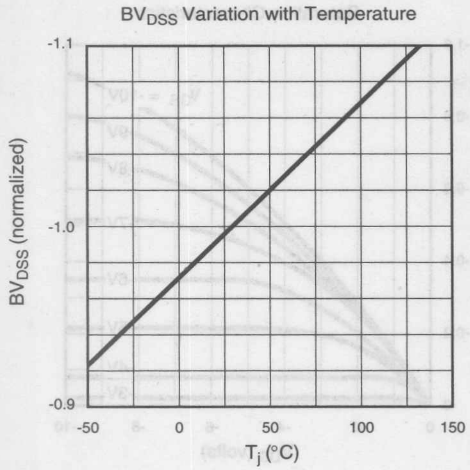
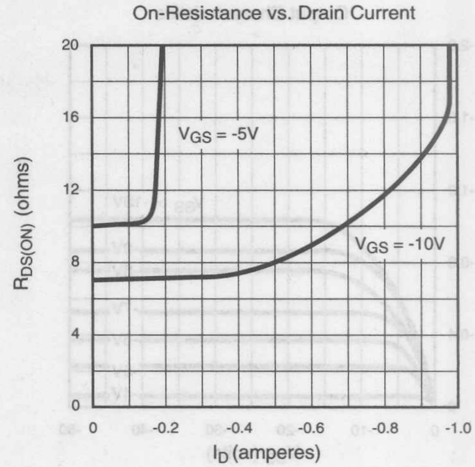
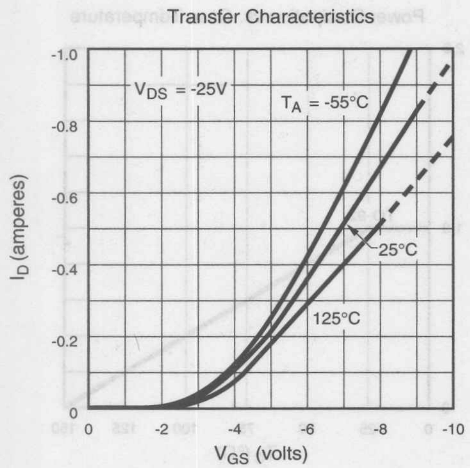
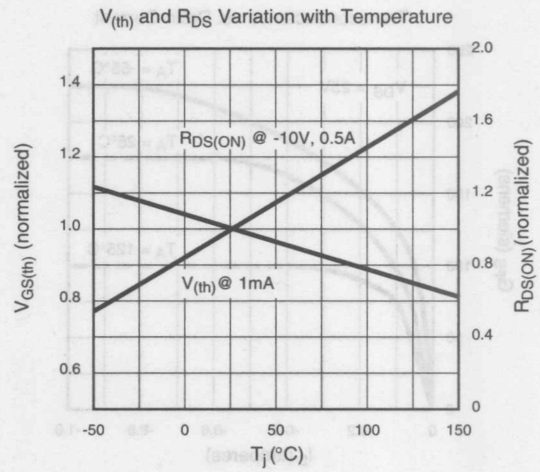
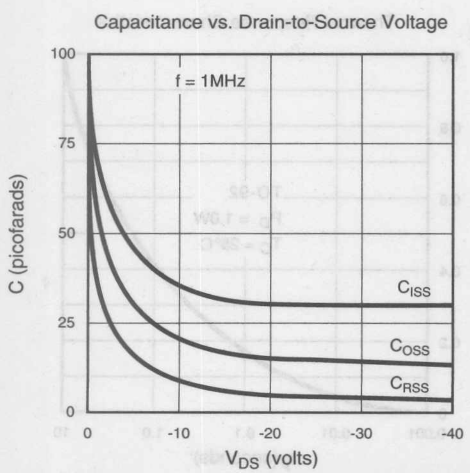
Typical Performance Curves

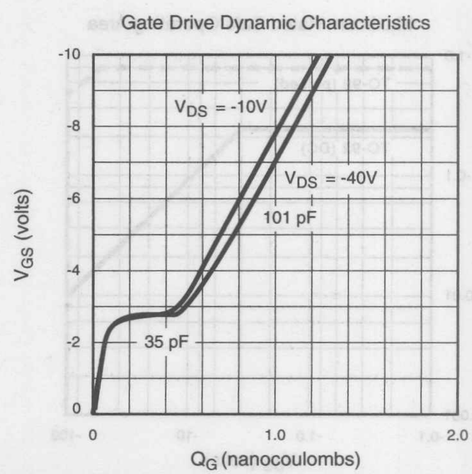












Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package TO-39	TO-92	DICE†
-40V	0.9Ω	-4A	VP2204N2	VP2204N3	VP2204ND
-60V	0.9Ω	-4A	VP2206N2	VP2206N3	VP2206ND
-100V	0.9Ω	-4A	VP2210N2	VP2210N3	VP2210ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

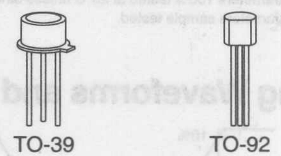
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39 TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-39	-1.6A	-8.0A	6.0W	125	20	-1.6A	-8.0A
TO-92	-0.65A	-4.0A	1.0W	170	125	-0.65A	-4.0A

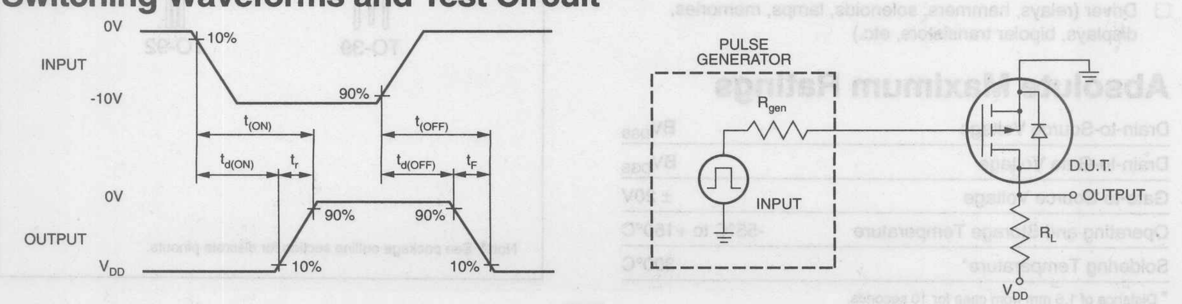
* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP2204	-40			V	$V_{GS} = 0V$, $I_D = -10mA$
		VP2206	-60				
		VP2210	-100				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.3		-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -10mA$
I_{GSS}	Gate Body Leakage		-1		-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				-50	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					-10	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		-1.5	-2		A	$V_{GS} = -5V$, $V_{DS} = -25V$
			-4	-9			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.3	1.5	Ω	$V_{GS} = -5V$, $I_D = -1A$
				0.75	0.9		$V_{GS} = -10V$, $I_D = -3.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	$V_{GS} = -10V$, $I_D = -3.5A$
G_{FS}	Forward Transconductance		0.8	1.4		℧	$V_{DS} = -25V$, $I_D = -2A$
C_{ISS}	Input Capacitance			325	450	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			125	180		
C_{RSS}	Reverse Transfer Capacitance			30	40		
$t_{d(ON)}$	Turn-ON Delay Time			4	10	ns	$V_{DD} = -25V$ $I_D = -4A$ $R_{GEN} = 10Ω$
t_r	Rise Time			16	30		
$t_{d(OFF)}$	Turn-OFF Delay Time			16	30		
t_f	Fall Time			22	40		
V_{SD}	Diode Forward Voltage Drop			-1.1	-1.6	V	$V_{GS} = 0V$, $I_{SD} = -3.5A$
t_{rr}	Reverse Recovery Time			500		ns	$V_{GS} = 0V$, $I_{SD} = -1A$

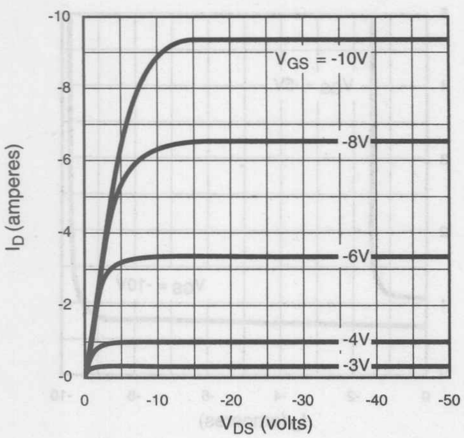
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

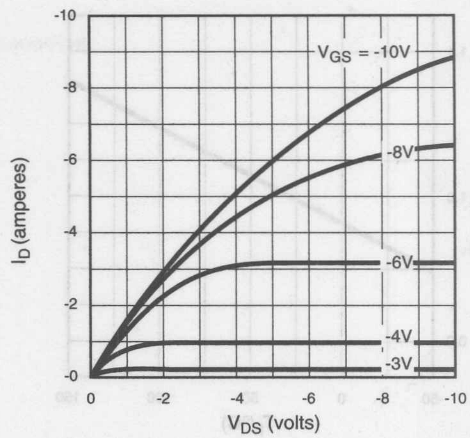


Typical Performance Curves

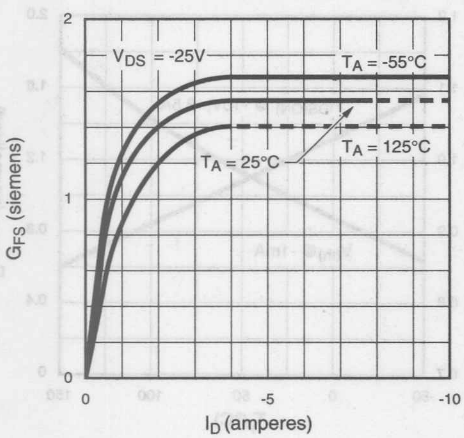
Output Characteristics



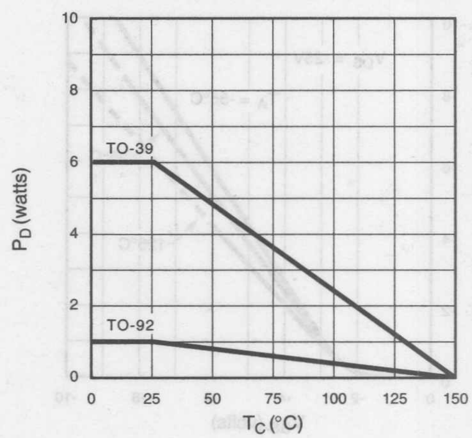
Saturation Characteristics



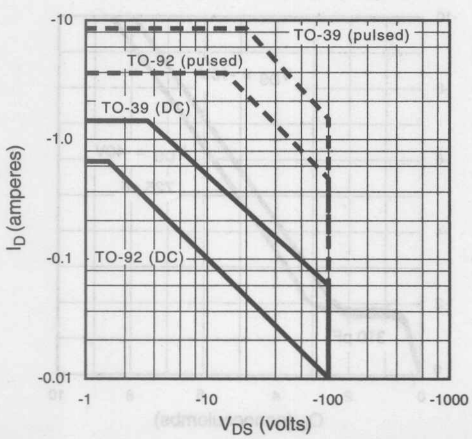
Transconductance vs. Drain Current



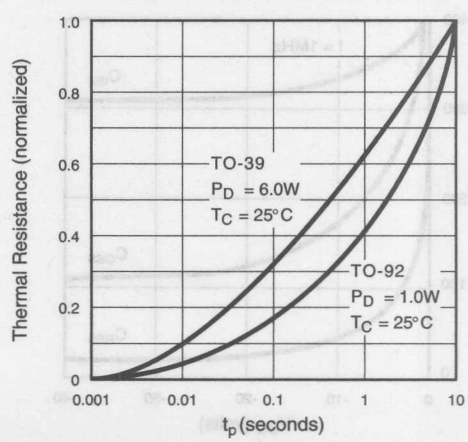
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

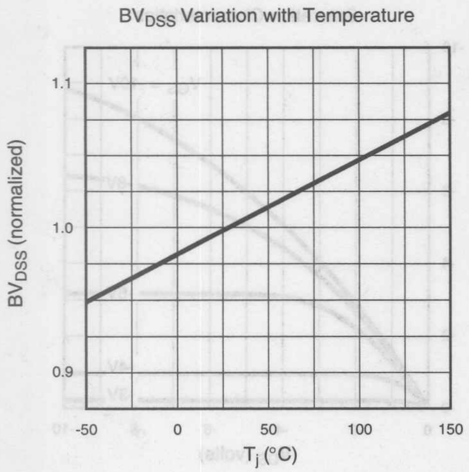


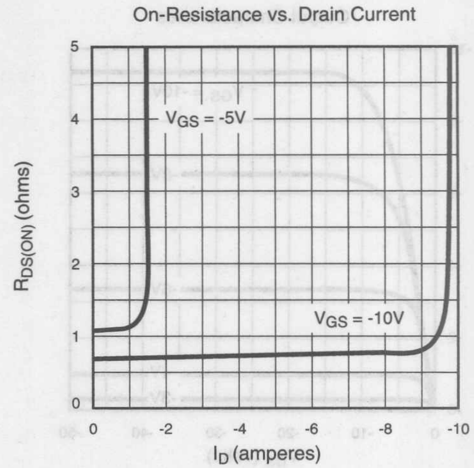
Thermal Response Characteristics

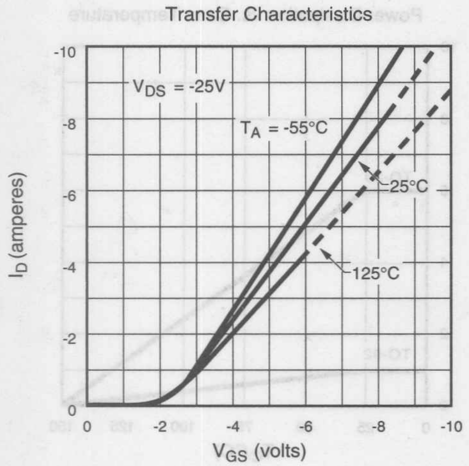


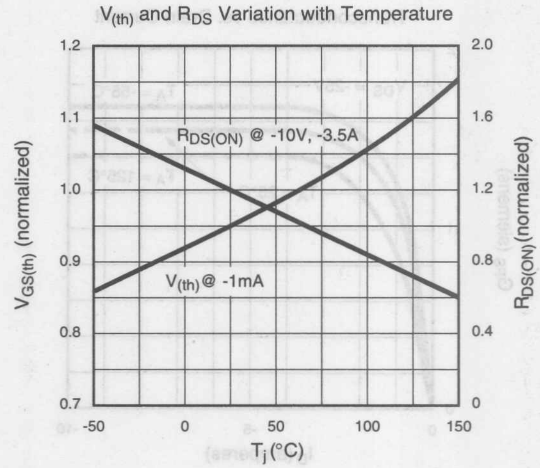
9

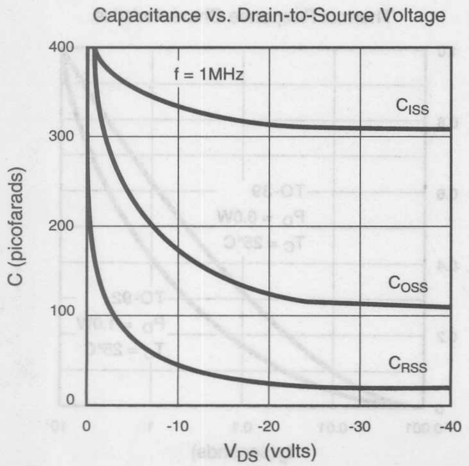
Typical Performance Curves

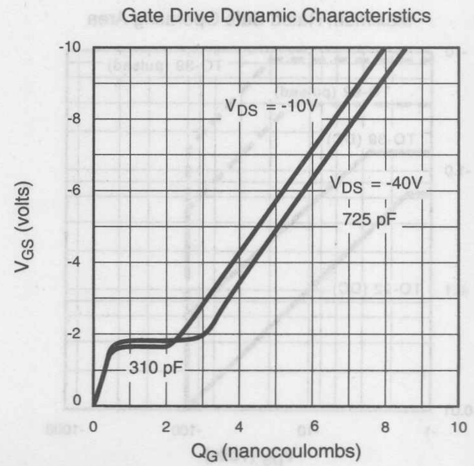












Chapter 10 – DMOS Arrays and Special Functions

Supertex inc.

8 Channel MOSFET Array
Monolithic N-Channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = 100V Max	I_{DSS}** @ V_{DS} = 250V Max	Order Number / Package: 18-Lead Plastic DIP	Plastic SOW-20*	Die†
160V	350Ω	25mA	1nA	—	AN0116NA	AN0116WG	AN0116ND
200V	300Ω	25mA	—	—	AN0120NA	—	AN0120ND
300V	300Ω	25mA	—	—	AN0130NA	—	AN0130ND
320V	350Ω	25mA	—	1nA	AN0132NA	AN0132WG	AN0132ND
400V	350Ω	25mA	—	—	AN0140NA	AN0140WG	AN0140ND

* Same as SO-20 with 300 mil wide body.
** Average current per channel, measured with all eight channels connected in parallel.
† MIL visual screening available

Features

- ☐ Low drain to source leakage for AN0116 and AN0132
- ☐ 160-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Free from secondary breakdown

Applications

- ☐ High impedance/low leakage measurements for bare board testers
- ☐ High voltage piezoelectric transducer drivers
- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

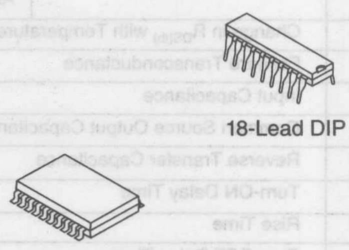
* Distance of 1.6 mm from case for 10 seconds.

General Description

The Supertex AN01 series of high voltage arrays is designed to provide the interface between CMOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AN0116 and AN0132 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 Lead Plastic	30mA	75mA	1.5W	135	83	30mA	75mA
SOW - 20	30mA	75mA	1.4W	110	89	30mA	75mA

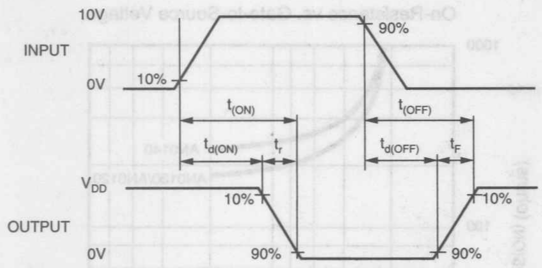
* I_D (continuous) is limited by max rated T_j.

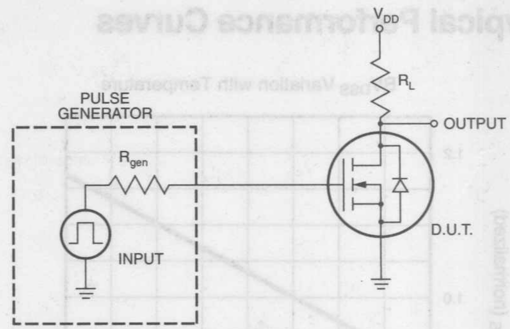
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AN0116	160			V	$V_{GS} = 0$, $I_D = 100\mu A$
		AN0120	200				
		AN0130	300				
		AN0132	320				
		AN0140	400				
$V_{GS(th)}$	Gate Threshold Voltage		2		5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5		mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage	AN0120			10	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0^{(3)}$
		AN0130					
		AN0140					
		AN0116			1	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0^{(3)}$
		AN0132					
I_{DSS}	Zero Gate Voltage Drain Current	AN0120			1	µA	$V_{GS} = 0$, V_{DS} = Max Rating$^{(3)}$
		AN0130			1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C^{(3)}$
		AN0140					
		AN0116			1	nA	$V_{GS} = 0V$, $V_{DS} = 100V^{(3)}$
					2	µA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C^{(3)}$
		AN0132			1	nA	$V_{GS} = 0V$, $V_{DS} = 250V^{(3)}$
					2	µA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C^{(3)}$
$I_{D(ON)}$	ON-State Drain Current		25			mA	$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	AN0120			300	Ω	$V_{GS} = 10V$, $I_D = 10mA$
		AN0130					
		AN0116			350	Ω	$V_{GS} = 10V$, $I_D = 10mA$
		AN0132					
		AN0140					
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			0.8		%/°C	$V_{GS} = 10V$, $I_D = 10mA$,
G_{FS}	Forward Transconductance		4.0	8.0		m℧	$\Delta V_{GS} = 1V$, $I_D = 10mA$
C_{ISS}	Input Capacitance			5.0	7.5	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1MHz
C_{OSS}	Common Source Output Capacitance			3.0	5.0		
C_{RSS}	Reverse Transfer Capacitance			0.8	1.5		
$t_{d(ON)}$	Turn-ON Delay Time			3		ns	$V_{DD} = 25V$, $I_D = 10mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time			3			
$t_{d(OFF)}$	Turn-OFF Delay Time			5			
t_f	Fall Time			3			
V_{SD}	Diode Forward Voltage Drop				1.3	V	$V_{GS} = 0$, $I_{SD} = 50mA$

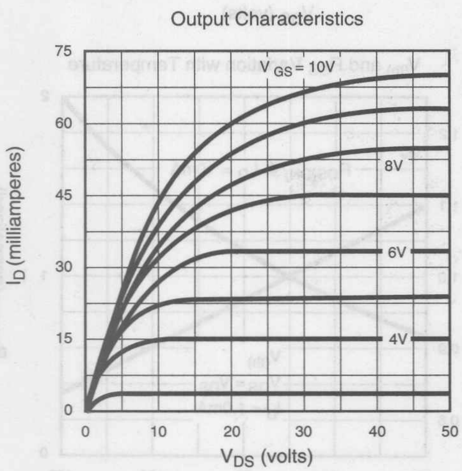
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
3. Average current per channel, measured with all 8 channels connected in parallel.

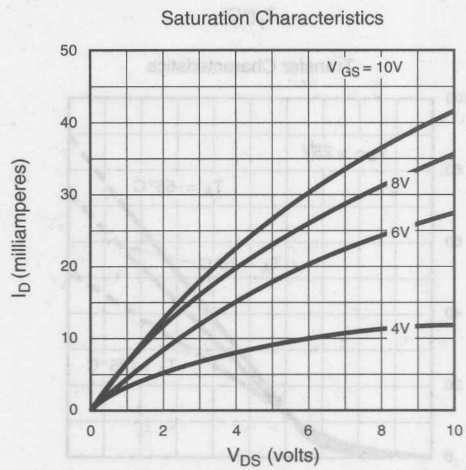
Switching Waveforms and Test Circuit

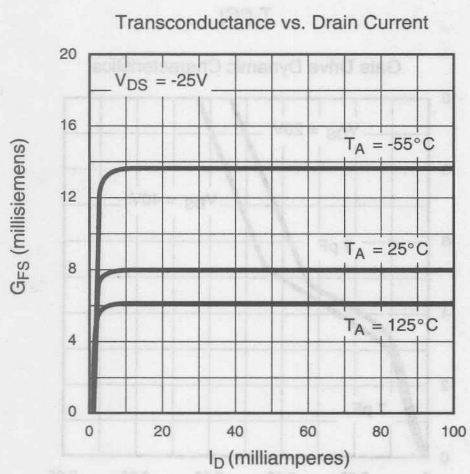


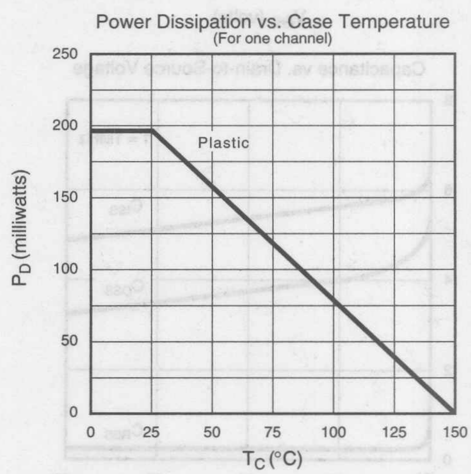


Typical Performance Curves

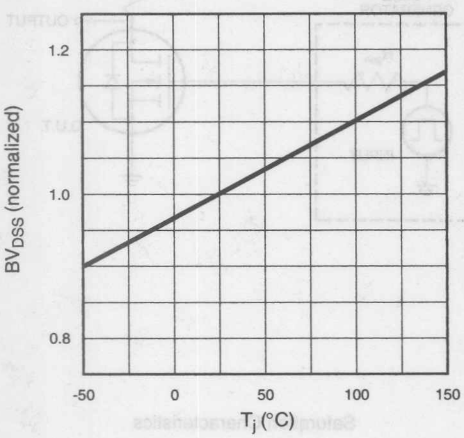




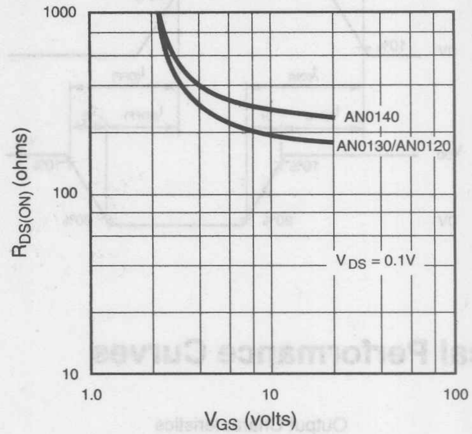




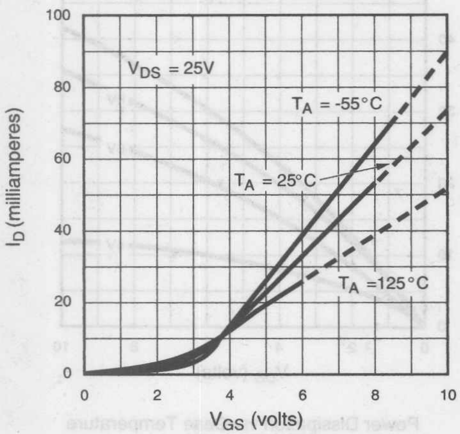
Typical Performance Curves



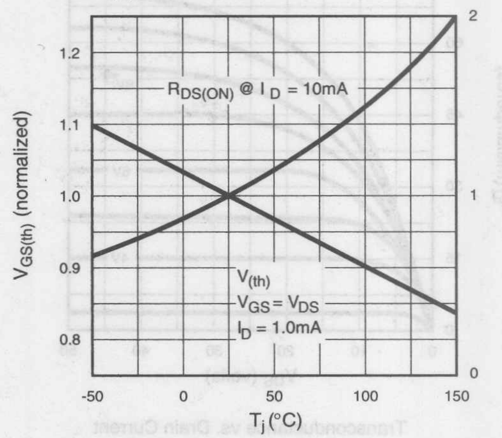
BV$_{DSS}$ Variation with Temperature



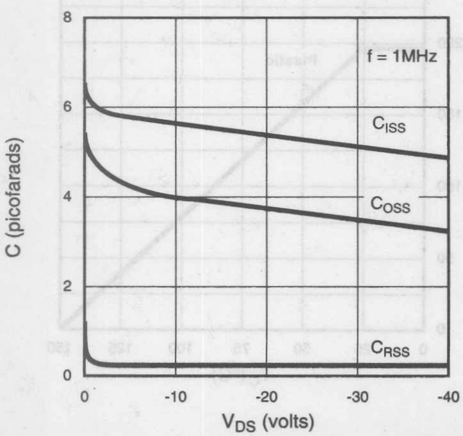
On-Resistance vs. Gate-to-Source Voltage



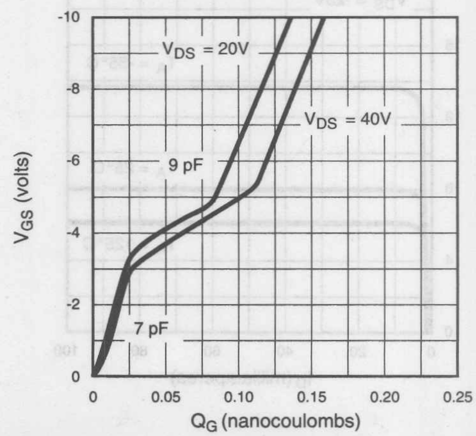
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature

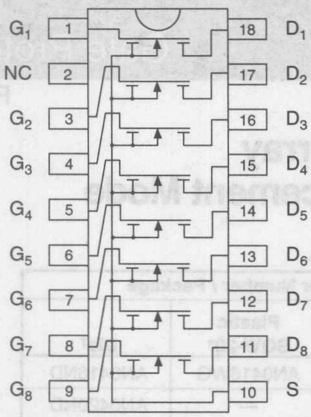


Capacitance vs. Drain-to-Source Voltage

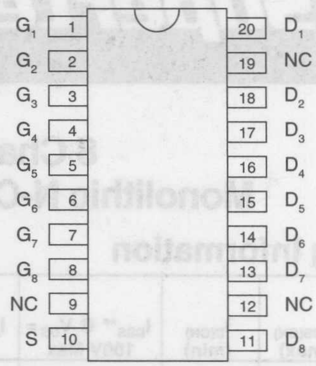


Gate Drive Dynamic Characteristics

Pin Configuration and Schematic



top view
18-pin DIP



top view
SOW - 20

10

Supertex inc.

Gate Protected

Preliminary

8 Channel MOSFET Array
Monolithic N-Channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = 100V Max	I_{DSS}** @ V_{DS} = 250V Max	Order Number / Package		
					18-Lead Plastic DIP	Plastic SOW-20*	Die†
160V	350Ω	25mA	1nA	—	AN0416NA	AN0416WG	AN0416ND
200V	300Ω	25mA	—	—	AN0420NA	—	AN0420ND
300V	300Ω	25mA	—	—	AN0430NA	—	AN0430ND
320V	350Ω	25mA	—	1nA	AN0432NA	AN0432WG	AN0432ND
400V	350Ω	25mA	—	—	AN0440NA	AN0440WG	AN0440ND

* Same as SO-20 with 300 mil wide body.
** Average current per channel, measured with all eight channels connected in parallel.
† MIL visual screening available

Features

- ☐ ESD Gate Protection
- ☐ Low drain to source leakage for AN0416 and AN0432
- ☐ 160-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Free from secondary breakdown

Applications

- ☐ High impedance/low leakage measurements for Bare Board Testers
- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

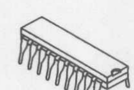
* Distance of 1.6 mm from case for 10 seconds.

General Description

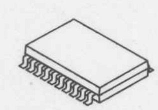
The Supertex AN04 series of high voltage arrays is a ruggedized ESD gate protected version of the Supertex AN01 series. These multichannel arrays meet the EIA ESD standard of 2000V, 100pF capacitor in series with a 1.5KΩ resistor. They are designed to provide interface between CMOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AN0416 and AN0432 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

Package Options



18-Lead DIP



SOW-20

Thermal Characteristics

Package	I_D(continuous)*	I_D(pulsed)*	Power Dissipation @T_C=25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	30mA	75mA	1.5W	135	83	30mA	75mA
SOW - 20	30mA	75mA	1.4W	110	89	30mA	75mA

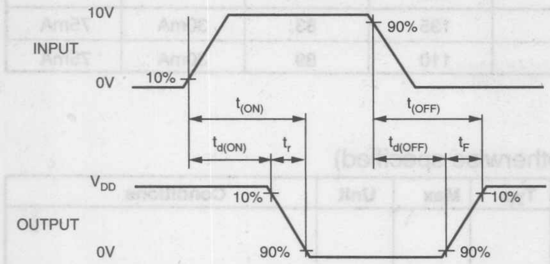
* I_D (continuous) is by max rated T_j

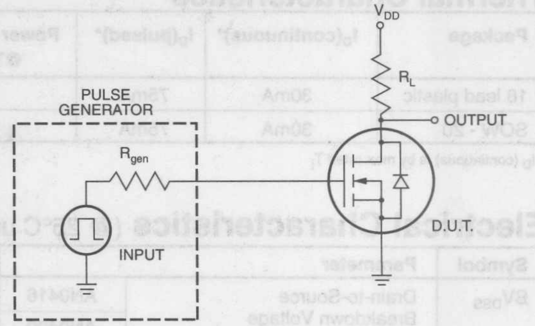
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AN0416	160			V	I_D = 100µA, V_{GS}= 0V
		AN0420	200				
		AN0430	300				
		AN0432	320				
		AN0440	400				
$V_{GS(th)}$	Gate Threshold Voltage		2		5	V	V_{GS} = V_{DS}, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5		mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage	AN0420 AN0430 AN0440			10	nA	V_{GS} = ±20V, V_{DS} = 0V (3)
		AN0416 AN0432			1	nA	V_{GS} = ±20V, V_{DS} = 0V (3)
I_{DSS}	Zero Gate Voltage Drain Current	AN0420			1	uA	V_{GS} = 0, V_{DS} = Max Rating (3)
		AN0430			1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating
		AN0440					T_A =125°C (3)
		AN0416			1	nA	V_{GS} = 0V, V_{DS} = 100V (3)
					2	µA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A=125°C (3)
		AN0432			1	nA	V_{GS} = 0V, V_{DS} = 250V (3)
					2	µA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C(3)
$I_{D(ON)}$	ON-State Drain Current		25			mA	V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source	AN0420 AN0430			300	Ω	V_{GS} = 10V, I_D = 10mA
	ON-State Resistance	AN0416 AN0432 AN0440			350	Ω	V_{GS} = 10V, I_D = 10mA
$\Delta R_{DS(ON)}$	Charge in $R_{DS(ON)}$ with Temperature			0.8		%/°C	V_{GS} = 10V, I_D = 10mA
G_{FS}	Forward Transconductance		4.0	8.0		m℧	ΔV_{GS} = 1V, I_D =10mA
C_{ISS}	Input Capacitance			8.0	12.0	pF	V_{DS} = 25V, V_{GS} = 0V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			5.0	8.0		
C_{RSS}	Reverse Transfer Capacitance			1.3	2.4		
$t_{d(ON)}$	Turn-ON Delay Time			5.0		ns	V_{DD} = 25V, I_D = 10mA, R_{GEN} = 25Ω
t_r	Rise Time			5.0			
$t_{d(OFF)}$	Turn-OFF Delay Time			8.0			
t_f	Fall Time			5.0			
V_{SD}	Diode Forward Voltage Drop				1.3	V	V_{GS} = 0V, I_{SD} = 50mA

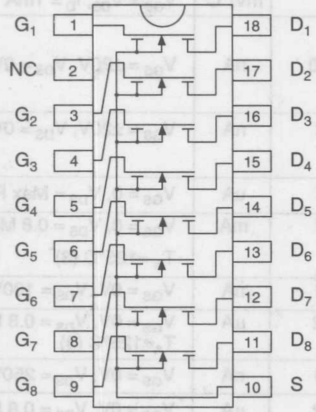
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
3. Average current per channel, measured with all 8 channels connected in parallel.

Switching Waveforms and Test Circuit

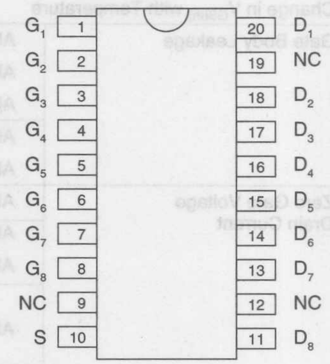




Pin Configuration and Schematic



top view
18-pin DIP



top view
SOW - 20

Semicustom 8 N-Channel Monolithic High Voltage Array With Logic

Ordering Information

HV_{OUT} (Max)	R_{OUT} (Max)	$I_{OUT(ON)}$ (Max)	$I_{OUT(OFF)}$* @ V_{OUT} = 100V Max	$I_{OUT(OFF)}$* @ V_{OUT} = 250V Max	Order Number†	Package Options
160V	350Ω	25mA	1nA	—	AN0516	Available in Plastic DIP, Surface Mount SOIC, and Die.
320V	350Ω	25mA	—	1nA	AN0532	

* Average current per channel, measured with all eight channels connected in parallel.
† Excluding package suffix.

Features

- ☐ Custom logic control
- ☐ Low output leakage current
- ☐ ESD input protection
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Free from secondary breakdown

Applications

- ☐ High impedance/low leakage measurements for bare board testers
- ☐ Sample and hold circuits
- ☐ High voltage electrostatic array drivers
- ☐ Addressable multi-channel driver array

Absolute Maximum Ratings[1]

Output Voltage, HV_{OUT}	320V†
Logic Supply Voltage, V_{DD}	-0.5V to 18V
Logic Input Voltage	-0.5V to V_{DD}+0.3V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature[2]	300°C
Channel to Channel Crosstalk	10mV/V

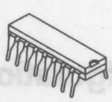
Notes:
1. All voltages referenced to V_{SS}.
2. Distance of 1.6mm from case for 10 seconds.
† For AN0532

General Description

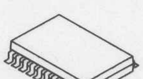
The Supertex AN05 series of semicustom high voltage monolithic devices consist of 8-channel open drain common source N-channel array with logic. The Logic configuration and packaging are determined by customer requirements.

The AN0516 and AN0532 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

Package Options



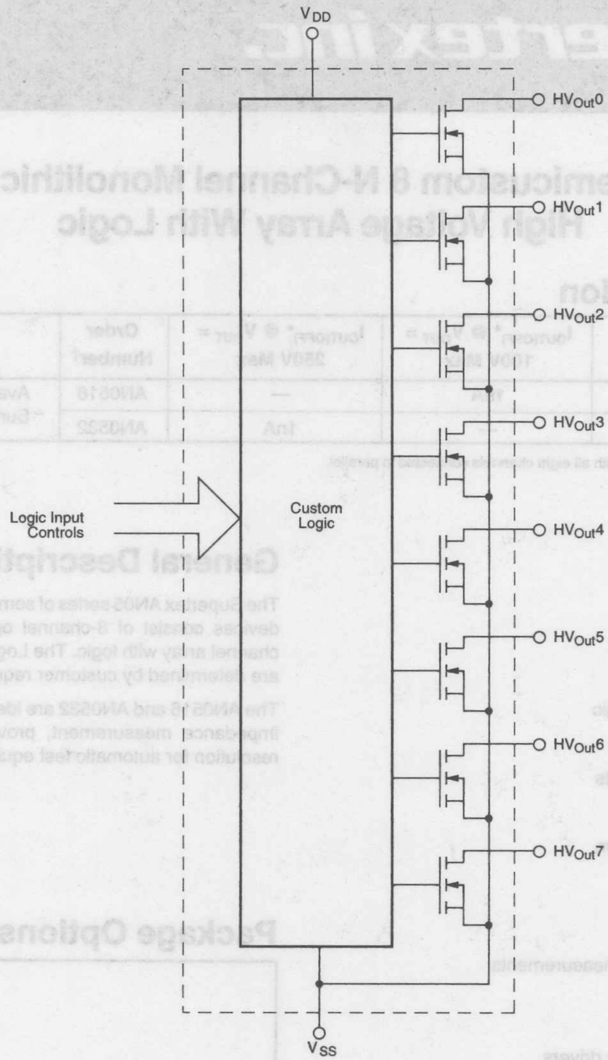
16-Lead DIP



SOW-20

Note1: Consult factory for other package options.

Block Diagram



Pin Configuration and Package

Based on customer requirements

8-Channel MOSFET Array
Monolithic P-Channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = -100V Max	I_{DSS}** @ V_{DS} = -250V Max	Order Number / Package: 18-Lead Plastic DIP	Plastic SOW-20*	Die†
-160V	700Ω	-15mA	-1.5nA	—	AP0116NA	AP0116WG	AP0116ND
-200V	600Ω	-15mA		—	AP0120NA	—	AP0120ND
-300V	600Ω	-15mA	—	—	AP0130NA	—	AP0130ND
-320V	700Ω	-15mA	—	-1.5nA	AP0132NA	AP0132WG	AP0132ND
-400V	700Ω	-15mA	—	—	AP0140NA	AP0140WG	AP0140ND

* Same as SO-20 with 300 mil wide body.
** Average current per channel, measured with all eight channels connected in parallel.
† MIL visual screening available

Features

- ☐ Low drain to source leakage for AP0116 and AP0132
- ☐ 160-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Free from secondary breakdown

Applications

- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

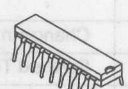
* Distance of 1.6 mm from case for 10 seconds.

General Description

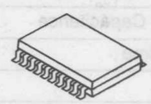
The Supertex AP01 series of high voltage arrays is designed to provide interface between CMOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AP0116 and AP0132 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

Package Options



18-Lead DIP



SOW-20

10

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25°C$	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	-15mA	-40mA	1.5W	135	83	-15mA	-40mA
SOW - 20	-15mA	-40mA	1.4W	110	89	-15mA	-40mA

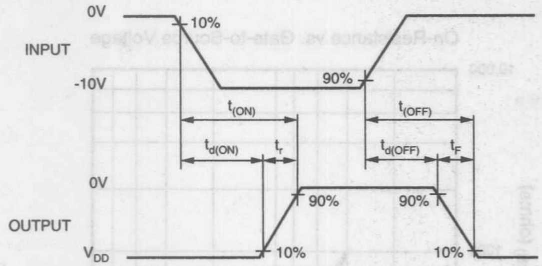
* I_D (continuous) is limited by max rated T_j.

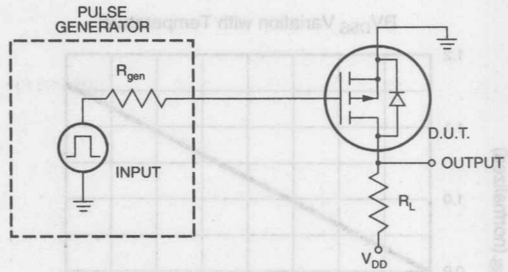
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AP0116	-160				
		AP0120	-200				
		AP0130	-300			V	$V_{GS} = 0$, $I_D = -100\mu A$
		AP0132	-320				
		AP0140	-400				
$V_{GS(th)}$	Gate Threshold Voltage		-2		-5	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5		mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage	AP0120					
		AP0130			-10	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V^{(3)}$
		AP0140					
		AP0116			-1	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V^{(3)}$
		AP0132					
I_{DSS}	Zero Gate Voltage Drain Current	AP0120			-1	µA	$V_{GS} = 0$, V_{DS} = Max Rating$^{(3)}$
		AP0130			-1	mA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C^{(3)}$
		AP0140					
		AP0116			-1.5	nA	$V_{GS} = 0V$, $V_{DS} = -100V^{(3)}$
					-3	µA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C^{(3)}$
		AP0132			-1.5	nA	$V_{GS} = 0V$, $V_{DS} = -250V^{(3)}$
					-3	µA	$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C^{(3)}$
$I_{D(ON)}$	ON-State Drain Current		-15			mA	$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	AP0120			600	Ω	$V_{GS} = -10V$, $I_D = -10mA$
		AP0130					
		AP0116					
		AP0132			700	Ω	$V_{GS} = -10V$, $I_D = -10mA$
		AP0140					
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			0.8		%/°C	$V_{GS} = -10V$, $I_D = -10mA$,
G_{FS}	Forward Transconductance		3.0	5.0		m℧	$V_{DS} = -25V$, $I_D = -5mA$
C_{ISS}	Input Capacitance			5.0	7.5		
C_{OSS}	Common Source Output Capacitance			3.0	5.0	pF	$V_{GS} = 0$, $V_{DS} = -25V$, f = 1MHz
C_{RSS}	Reverse Transfer Capacitance			1.0	2.0		
$t_{d(ON)}$	Turn-ON Delay Time			3			
t_r	Rise Time			3		ns	$V_{DD} = -25V$, $I_D = -10mA$
$t_{d(OFF)}$	Turn-OFF Delay Time			5			$R_{GEN} = 25\Omega$
t_f	Fall Time			3			
V_{SD}	Diode Forward Voltage Drop				-1.5	V	$V_{GS} = 0$, $I_{SD} = -25mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
3. Average current per channel, measured with all 8 channels connected in parallel.

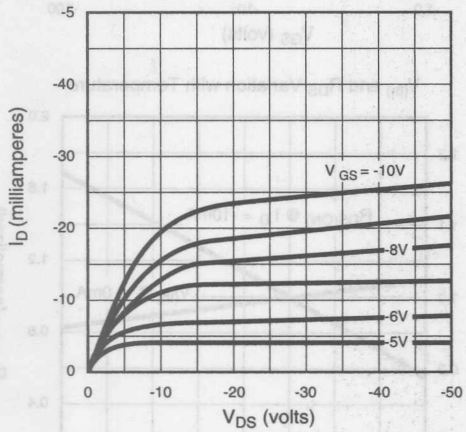
Switching Waveforms and Test Circuit



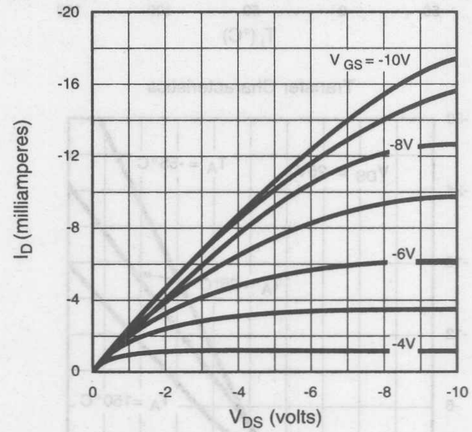


Typical Performance Curves

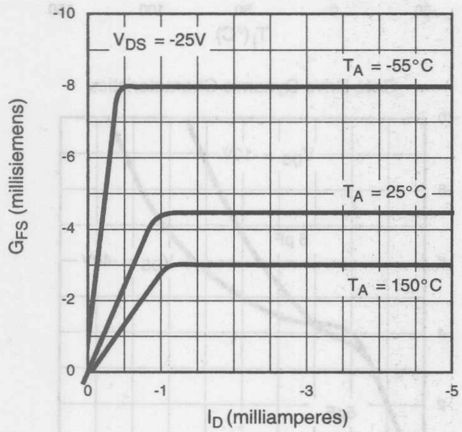
Output Characteristics



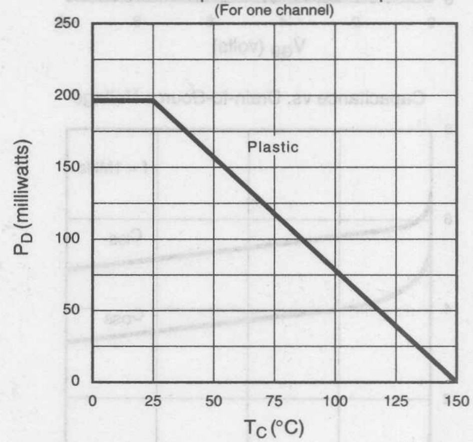
Saturation Characteristics

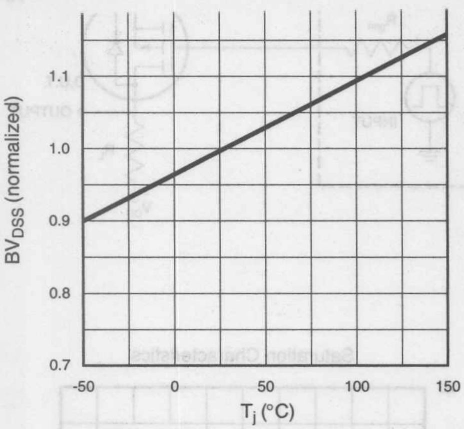


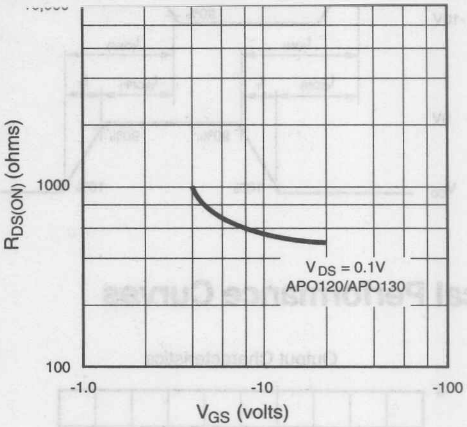
Transconductance vs. Drain Current



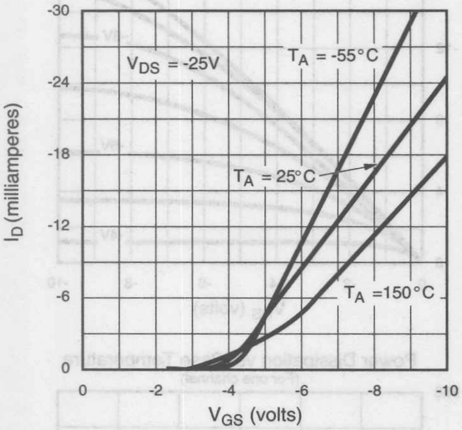
Power Dissipation vs. Case Temperature
(For one channel)



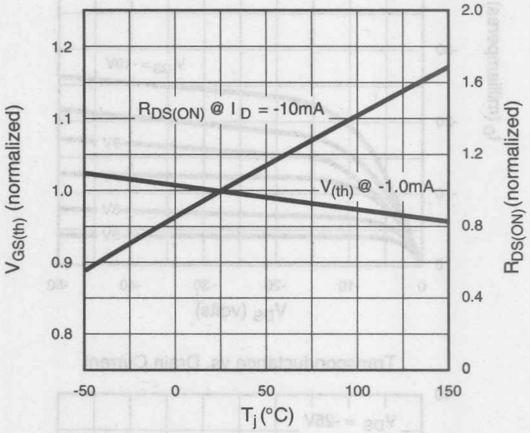




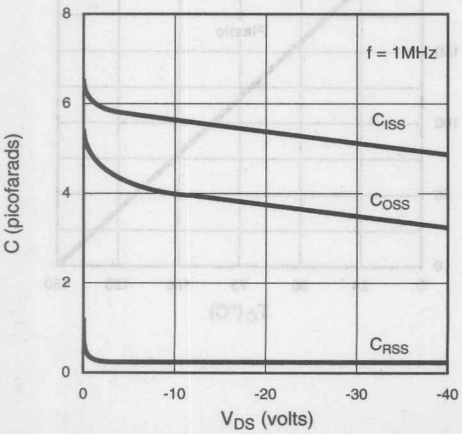
Transfer Characteristics



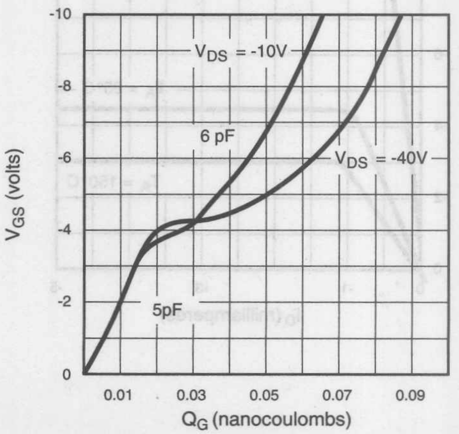
$V_{(th)}$ and R_{DS} Variation with Temperature



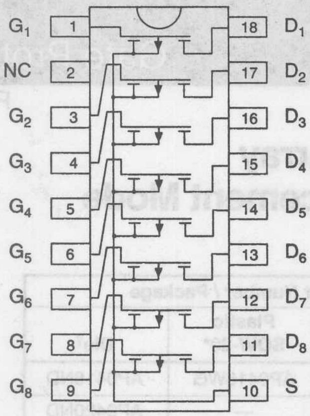
Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

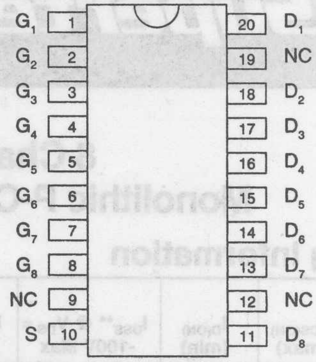


Pin Configuration and Schematic



top view

18-pin DIP



top view

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Supertex inc.

Gate Protected

Preliminary

8 Channel MOSFET Array
Monolithic P-Channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = -100V Max	I_{DSS}** @ V_{DS} = -250V Max	Order Number / Package		
					18-Lead Plastic DIP	Plastic SOW-20*	Die†
-160V	700Ω	-15mA	-1.5nA	—	AP0416NA	AP0416WG	AP0416ND
-200V	600Ω	-15mA	—	—	AP0420NA	—	AP0420ND
-300V	600Ω	-15mA	—	—	AP0430NA	—	AP0430ND
-320V	700Ω	-15mA	—	-1.5nA	AP0432NA	AP0432WG	AP0432ND
-400V	700Ω	-15mA	—	—	AP0440NA	AP0440WG	AP0440ND

* Same as SO-20 with 300 mil wide body.
** Average current per channel, measured with all eight channels connected in parallel.
† MIL visual screening available

Features

- ☐ ESD gate protection
- ☐ Low drain to source leakage for AP0416 and AP0432
- ☐ 160-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Free from secondary breakdown

Applications

- ☐ High impedance/low leakage measurements for bare board testers
- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

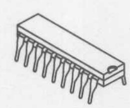
* Distance of 1.6 mm from case for 10 seconds.

General Description

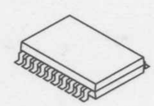
The Supertex AP04 series of high voltage arrays is a ruggedized ESD gate protected version of the Supertex AP01 series. These multichannel arrays meet the EIA ESD standard of 2000V, 100pF capacitor in series with a 1.5KΩ resistor. They are designed to provide interface between CMOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AP0416 and AP0432 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

Package Options



18-Lead DIP



SOW-20

Thermal Characteristics

Package	I_D(continuous)*	I_D(pulsed)*	Power Dissipation @T_C=25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	-15mA	-40mA	1.5W	135	83	-15mA	-40mA
SOW -20	-15mA	-40mA	1.4W	110	89	-15mA	-40mA

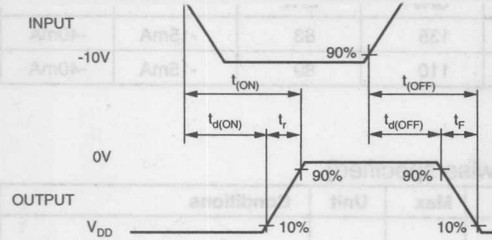
* I_D (continuous) is limited by max rated T_j

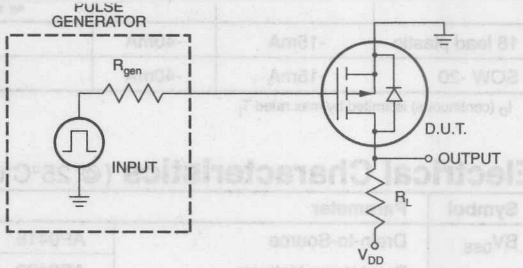
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AP0416	-160			V	I_D = -100µA, V_{GS}= 0V
		AP0420	-200				
		AP0430	-300				
		AP0432	-320				
		AP0440	-400				
$V_{GS(th)}$	Gate Threshold Voltage		-2		-5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5		mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage	AP0420			-10	nA	V_{GS} = ±20V, V_{DS} =0V (3)
		AP0430					
		AP0440					
		AP0416			-1	nA	V_{GS} = ±20V, V_{DS} =0V (3)
		AP0432					
I_{DSS}	Zero Gate Voltage Drain Current	AP0420			-1	µA	V_{GS} = 0, V_{DS} = Max Rating (3)
		AP0430			-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A =125°C (3)
		AP0440					
		AP0416			-1.5	nA	V_{GS} = 0V, V_{DS} = -100V (3)
					-3	µA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A=125°C (3)
		AP0432			-1.5	nA	V_{GS} = 0V, V_{DS} = -250V (3)
					-3	µA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C (3)
$I_{D(ON)}$	ON-State Drain Current		-15			mA	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	AP0420			600	Ω	V_{GS} = -10V, I_D = -10mA
		AP0430					
		AP0416			700	Ω	V_{GS} = -10V, I_D = -10mA
		AP0432					
		AP0440					
$\Delta R_{DS(ON)}$	Charge in $R_{DS(ON)}$ with Temperature			0.8		%/°C	V_{GS} = -10V, I_D = -10mA
G_{FS}	Forward Transconductance		3.0	5.0		m℧	V_{DS} = -25V, I_D = -5mA
C_{ISS}	Input Capacitance			8.0	12.0	pF	V_{DS} = -25V, V_{GS} = 0V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			5.0	8.0		
C_{RSS}	Reverse Transfer Capacitance			1.6	3.2		
$t_{d(ON)}$	Turn-ON Delay Time			5.0		ns	V_{DD} = -25V, I_D = -10mA, R_{GEN} = 25Ω
t_r	Rise Time			5.0			
$t_{d(OFF)}$	Turn-OFF Delay Time			8.0			
t_f	Fall Time			5.0			
V_{SD}	Diode Forward Voltage Drop				-1.5	V	V_{GS} = 0V, I_{SD} = -25mA

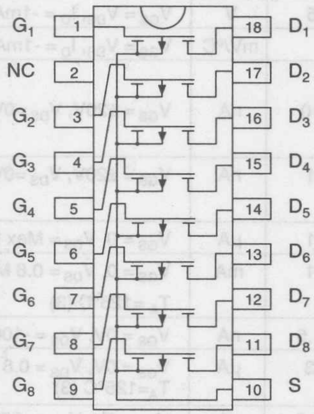
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.
3. Average current per channel, measured with all 8 channels connected in parallel.



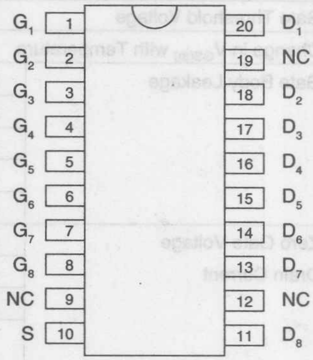


Pin Configuration and Schematic



top view

18-pin DIP



top view

SOW - 20

Supertex inc.

Semicustom 8 P-Channel Monolithic High Voltage Array With Logic

Ordering Information

HV_{OUT} (Max)	R_{OUT} (Max)	$I_{OUT(ON)}$ (Max)	$I_{OUT(OFF)}$* @ V_{OUT} = 100V Max	$I_{OUT(OFF)}$* @ V_{OUT} = 250V Max	Order Number†	Package Options
-160V	700Ω	-15mA	-1.5nA	—	AP0516	Available in Plastic DIP, Surface Mount SOIC, and Die.
-320V	700Ω	-15mA	—	-1.5nA	AP0532	

* Average current per channel, measured with all eight channels connected in parallel.
† Excluding package suffix.

Features

- ☐ Custom logic control
- ☐ Low output leakage current
- ☐ ESD Input protection
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Free from scecondary breakdown

Applications

- ☐ High impedance/low leakage measurements for bare board testers
- ☐ Sample and hold circuits
- ☐ High voltage electrostatic array drivers
- ☐ Addressable multi-channel driver array

Absolute Maximum Ratings[1]

Output Voltage, HV_{OUT}	-320V†
Logic Supply Voltage, V_{DD}	+0.5V to -18V
Logic Input Voltage	+0.5V to V_{DD}-0.3V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature [2]	300°C
Channel to Channel Crosstalk	10mV/V

Notes:
1. All voltages referenced to V_{SS}.
2. Distance of 1.6mm from case for 10 seconds.
† For AN0532

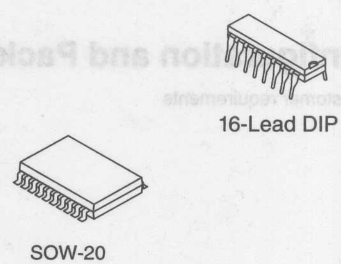
General Description

The Supertex AP05 series of semicustom high voltage monolithic devices consist of 8-channel open drain common source P-channel array with logic. The Logic configuration and packaging are determined by customer requirements.

The AP0516 and AP0532 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for automatic test equipment.

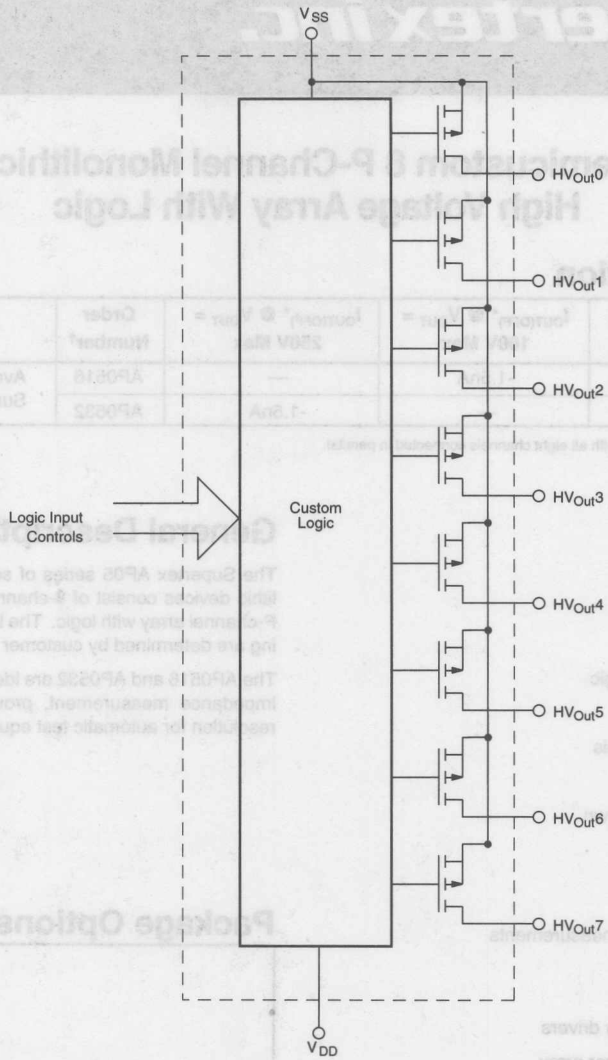
10

Package Options



Note: Consult factory for other package options.

Block Diagram



Pin Configuration and Package

Based on customer requirements

Supertex inc.

8-Channel Logic to High-Voltage Level Translator

Ordering Information

Device	Package Options			
	20 Lead C-DIP†	20 Lead Plastic DIP	Plastic SOW-20*	Die
HT01	HT0130C	HT0130P	HT0130WG	HT0130X

* Same as SO-20 300 mil wide body.
† Side brazed dual in-line package.

Features

- ☐ Operating voltage up to 300V
- ☐ 5V to 15V logic input capability
- ☐ Output swings below GND if required
- ☐ Drives high-voltage P-channel MOS from logic level signal
- ☐ Surface mount packaging available
- ☐ No "floating logic" required
- ☐ 8 independent channels

Applications

- ☐ ATE systems
- ☐ Printers/plotters
- ☐ P-channel MOSFET control

Absolute Maximum Ratings [1,2]

Supply Voltage, V_{DD}		V_{NN} - 0.3V to +16V
Supply Voltage, V_{PP}		V_{NN} - 0.3V to + 300V
Supply Voltage, V_{NN}		-16V to 0.3V
Logic inputs levels	V_{IN}	V_{NN} - 0.3V to V_{DD} + 0.3V
	V_{OUTPUT}	V_{PP} + 0.3V max
I_{OUT} — DC per Channel		30mA
Continuous total power dissipation[2]		700mW
Operating temperature range		0°C to 70°C
Storage temperature range		-65°C to + 150°C

Notes:
1: All voltages are referenced to chip ground.
2: For operation above 25°C ambient derate linearly to 85°C at 8mW/°C.

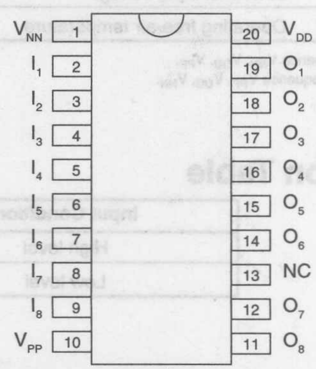
General Description

The Supertex HT01 8-channel level translator is designed to implement necessary level translation between logic level signals and voltage swings required to drive high-voltage P-channel MOSFET transistors. This device is intended to provide gate drive signals to devices such as the Supertex AP01 P-channel MOSFET array in applications requiring active pull-up to a high-voltage (V_{PP}) line of up to 300 volts. Logic input can be from 5 volts to 15 volts and is referenced to the logic supply (V_{DD}).

When an input is switched to 4.2 volts below the V_{DD} supply, the corresponding output will typically switch from V_{PP} to V_{PP} -14 volts. If the V_{PP} supply remains above 12 volts, the negative supply (V_{NN}) would be connected to system ground (GND). If variations of the V_{PP} supply level require the P-channel MOSFET gate drive to swing below GND in order to turn on, connect the V_{NN} pin to a negative supply of up to -15 volts. The logic inputs can remain between V_{DD} and system ground (GND) and still provide correct operation.

In an OFF condition, the HT01 is a low power device. In an ON condition, each channel will dissipate power determined by the V_{PP} and V_{NN} voltage. Internal power dissipation must be considered when the application requires that more than one channel be active at one time, especially at higher V_{PP} voltage values.

Pin Configuration



top view
20-pin DIP/SOW 20

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current			0.001	mA	All OFF
			0.6	3.50	mA	1 ch ON, no load
I_{PP}	V_{PP} Supply Current			0.001	mA	All OFF
			0.4	1.0	mA	1 ch ON, no load
I_{NN}	V_{NN} Supply Current			0.001	mA	All OFF
			1.0	4.50	mA	1 ch ON, no load
I_{SOURCE}	Output Current	135	200		µA	Capacitive load
I_{SINK}	Output Current	66	100		µA	Capacitive load
V_{ON}	Output Voltage	V_{PP} - 17		V_{PP} - 10	V	V_{DD} = 4.75V
		V_{PP} - 17		V_{PP} - 12.5	V	V_{DD} = 15V
V_{OFF}	Output Voltage	V_{PP} - 0.5			V	
V_Z	Zener Voltage	11	14	17	V	Output to V_{PP}

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{ON}	Turn on time, any channel		5		µs	V_{DD} = 10V, V_{NN} = GND
Δt_{ON}	Variation in t_{ON}, any 2 channels		5		%	V_{DD} = 10V, V_{NN} = GND
t_{OFF}	Turn off time, any channel		3		µs	V_{DD} = 10V, V_{NN} = GND
Δt_{OFF}	Variation in t_{OFF}, any 2 channels		5		%	V_{DD} = 10V, V_{NN} = GND

Recommended Operating Conditions*

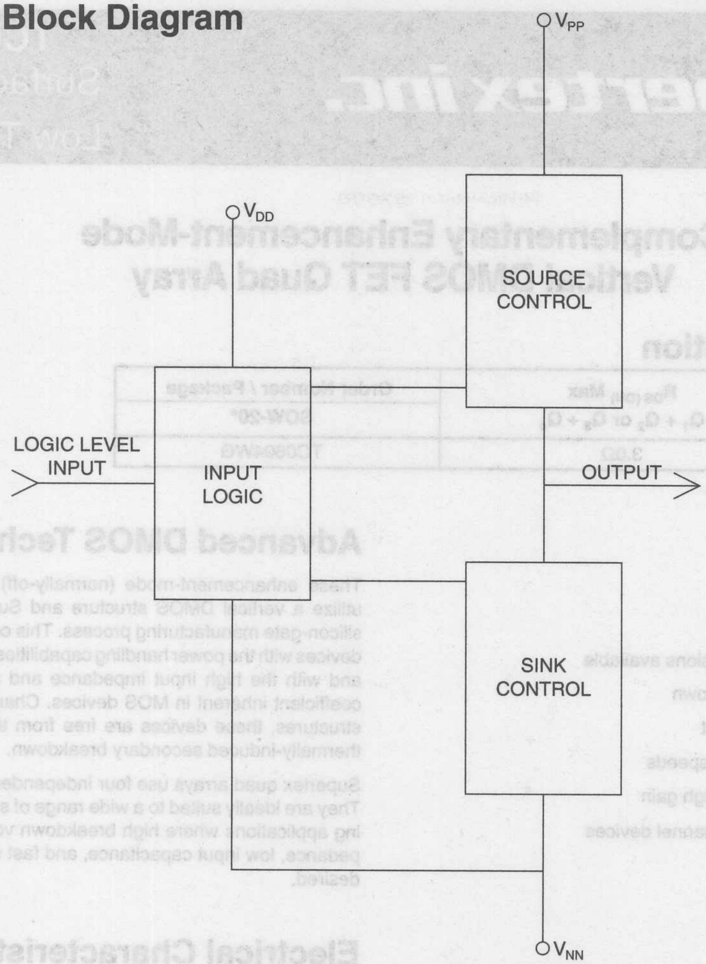
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.75		15	V
V_{PP}	Positive high voltage supply	V_{NN} + 12		275	V
V_{NN}	Negative supply	-15		0	V
V_{IH}	High-level input voltage	V_{DD} - 1.2		V_{DD}	V
V_{IL}	Low-level input voltage	0		V_{DD} - 4.2	V
T_A	Operating free-air temperature	0		+70	°C

* Power-up sequence V_{NN}, V_{DD}, V_{PP}.
Power-down sequence V_{PP}, V_{DD}, V_{NN}.

Function Table

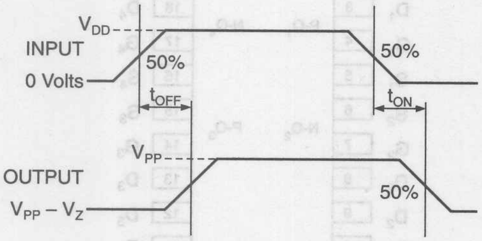
Input Condition	Output Stage
High level	V_{PP}
Low level	V_{PP} - V_Z

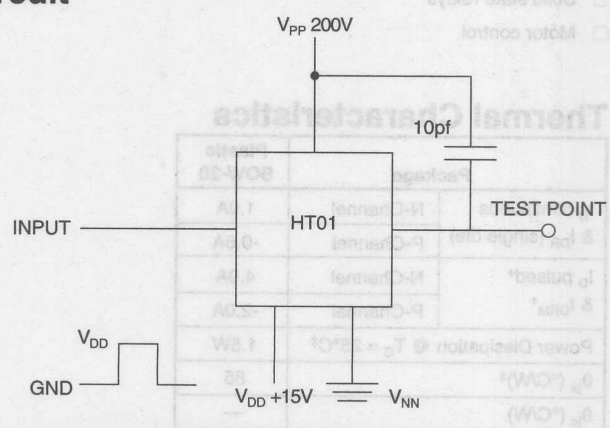
Functional Block Diagram



(One of eight channels within the HT01)

Switching Waveforms and Test Circuit





(One of eight channels within the HT01)

10

Complementary Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ Max $Q_1 + Q_2$ or $Q_3 + Q_4$	Order Number / Package SOW-20*
40V	3.0Ω	TC0604WG

* Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Telecom switches
- ☐ Logic level interface
- ☐ Battery operated system
- ☐ Photo voltaic drive
- ☐ Soild state relays
- ☐ Motor control

Thermal Characteristics

Package		Plastic SOW-20
I_D continuous & I_{DR} (single die)	N-Channel	1.0A
	P-Channel	-0.6A
I_D pulsed⁺ & I_{DRM}⁺	N-Channel	4.0A
	P-Channel	-2.0A
Power Dissipation @ $T_C = 25°C$‡		1.5W
θ_{ja} (°C/W)‡		85
θ_{jc} (°C/W)		—

⁺ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

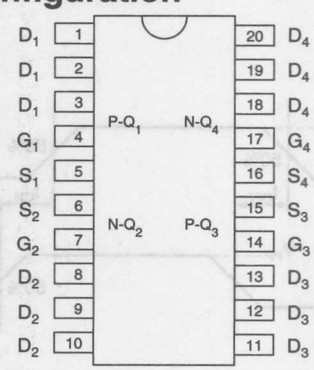
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TN06L and TP06L data sheets for detailed characteristics of N- and P-channel devices.

Pin Configuration



top view
SOW-20

N-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ Max	Order Number / Package SOW-20*
40V	1.0Ω	TN0604WG

* Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Telecom switches
- ☐ Logic level interface
- ☐ Battery operated system
- ☐ Photo voltaic drive
- ☐ Soild state relays
- ☐ Motor control

Thermal Characteristics

Package	Plastic SOW-20
I_D continuous & I_{DR} (single die)	1.0A
I_D pulsed⁺ & I_{DRM}⁺	4.0A
Power Dissipation @ $T_C = 25°C$‡	1.5W
θ_{ja} (°C/W)‡	85
θ_{jc} (°C/W)	—

⁺ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

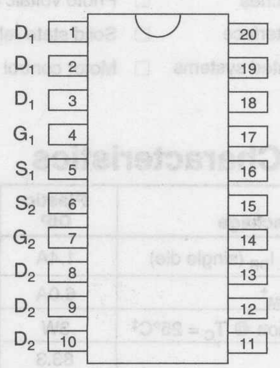
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TN06L data sheet for detailed characteristics.

Pin Configuration



top view
SOW-20

N-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
60V	1.5Ω	TN0606N6	TN0606N7

* 14 pin side brazed ceramic DIP

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- 4 independent channels
- 4 electrically isolated die
- Commercial and military versions available
- Free from secondary breakdown
- Low power drive requirement
- Low C_{ISS} and fast switching speeds
- High input impedance and high gain

Applications

- Telecom switches
- Logic level interface
- Battery operated systems
- Photo voltaic drive
- Soild state relays
- Motor control

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	1.4A	1.60A
I_D pulsed$^+$ & $I_{DRM}$$^+$	6.0A	6.0A
Power Dissipation @ $T_C = 25°C$‡	3W	4W
θ_{ja} (°C/W)‡	83.3	62.5
θ_{jc} (°C/W)‡	41.6	31.2

$^+$ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

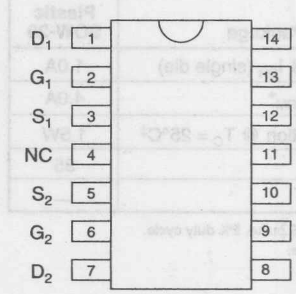
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TN06A data sheet for detailed characteristics.

Pin Configuration



top view
14-pin DIP

Supertex inc.

TP0604WG
Surface Mount
Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS (ON)}$ Max	Order Number / Package SOW-20*
-40V	2.0Ω	TP0604WG

* Same as SO-20 with 300 mil wide body.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Telecom switches
- ☐ Logic level interface
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Soild state relays
- ☐ Motor control

Thermal Characteristics

Package	Plastic SOW-20
I_D continuous & I_{DR} (single die)	-0.6A
I_D pulsed* & I_{DRM}*	-2.0A
Power Dissipation @ T_C = 25°C‡	1.5W
θ_{ja} (°C/W)‡	85
θ_{jc} (°C/W)	—

* Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

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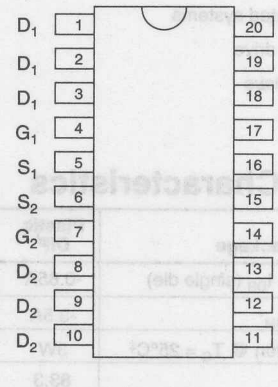
Electrical Characteristics

Refer to TP06L data sheet for detailed characteristics.

Pin Configuration



top view
20-pin DIP
SOW 20

Supertex inc.

TP0606N6
TP0606N7
Low Threshold

P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
-60V	3.5Ω	TP0606N6	TP0606N7

* 14 pin side brazed ceramic DIP

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and Military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Telecom switches
- ☐ Logic level interface
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Soild state relays
- ☐ Motor control

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	-0.65A	-0.75A
I_D pulsed⁺ & I_{DRM}⁺	-3.5A	-3.5A
Power Dissipation @ $T_C = 25°C$‡	3W	4W
θ_{ja} (°C/W)‡	83.3	62.5
θ_{jc} (°C/W)‡	41.6	31.2

⁺ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

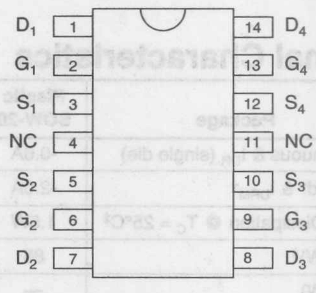
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to TP06A data sheet for detailed characteristics.

Pin Configuration



top view
14-pin DIP

Supertex inc.

TQ3001 VQ3001 VQ7254

Surface Mount

N- and P-Channel Quad Power MOSFET Arrays

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS\,(ON)}$ (max) Q1 + Q2 or Q3 + Q4	$V_{GS\,(th)}$ (max) N-Channel	P-Channel	Order Number / Package 14-Pin P-Dip	14-Pin C-Dip*	20 Terminal LCC Quad
40V	3Ω	2.0V	-3.0V	VQ3001N6	VQ3001N7	VQ3001NF
40V	3Ω	1.6V	-2.4V	TQ3001N6	TQ3001N7	TQ3001NF
20V	3Ω	2.0V	-3.0V	VQ7254N6	VQ7254N7	—

* 14 pin side brazed ceramic DIP

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices
- ☐ Low threshold version available

Applications

- ☐ Telecom switches
- ☐ Logic level interface
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Soild state relays
- ☐ Motor control

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

10

Plastic Dip	1.4A	-0.65A	3.0A	-3.0A	1.5W	—	83.3	1.4A	-0.65A	3.0A	-3.0A
20 Terminal LCC	410mA	-300mA	3.0A	-3.0A	1.0W	—	125.0	410mA	-300mA	3.0A	-3.0A

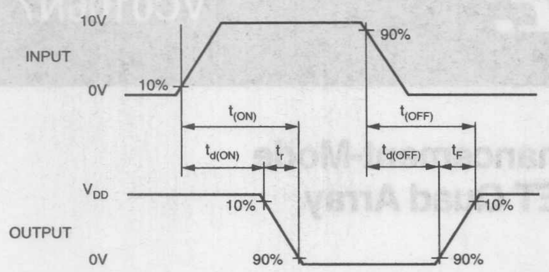
* Total for 4 die.
† Each die.

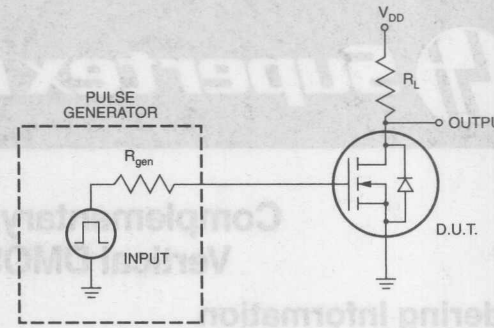
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		N-Channel Min	N-Channel Max	P-Channel Min	P-Channel Max	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TQ3001, VQ3001	40		-40		V	$V_{GS} = 0$, $I_D = 10\mu A$
		VQ7254	20		-20			
$V_{GS(th)}$	Gate Threshold Voltage	VQ3001, VQ7254	0.8	2.0	-0.8	-3.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$, $T_A = 25°C$
		TQ3001	0.6	1.6	-1.0	-2.4	V	
		VQ7254	0.5		-0.65		V	$V_{GS} = V_{DS}$, $I_D = 1mA$, $T_A = 85°C$
I_{GSS}	Gate Body Leakage			100		-100	nA	$V_{GS} = \pm16V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10		-10	µA	$V_{GS} = 0V$, $V_{DS} = 0.8$ Min. Rating
				500		-500	µA	$V_{GS} = 0V$, $V_{DS} = 0.8$ Min. Rating, $T_A = 125°C$
$V_{DS (ON)}$	Total Static Drain-to-Source ON-State Voltage	VQ3001, TQ3001		1.0		-2.0	V	$V_{GS} = 11.4V$, $I_D = 1A$
		VQ7254		1.0		-2.0		
$R_{DS (ON)}$	Total Static Drain-to-Source ON-State Resistance	TQ3001		1.5		3.5	Ω	$V_{GS} = 5.0V$, $I_D = 250mA$
		VQ3001, TQ3001		1.0		2.0		$V_{GS} = 11.4V$, $I_D = 1A$
		VQ7254		1.0		2.0		
G_{FS}	Forward Transconductance		200		200		m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			190		195	pF	$V_{GS} = 0V$, $V_{DS} = 20V$, f = 1Mz
C_{OSS}	Output Capacitance			110		120		
C_{RSS}	Reverse Transfer Capacitance			50		60		
$t_{(ON)}$	Turn-ON Time			30		30	ns	$V_{DD} = 15V$, $I_D = 0.65A$,
$t_{(OFF)}$	Turn-OFF Time			30		30	ns	$R_{GEN} = 25\Omega$
V_{SD}	Forward ON Voltage	VQ7254		1.8		-2	V	$V_{GS} = 0V$, $I_F = 1.5A$
		VQ3001, TQ3001		1.8		-2		$V_{GS} = 0V$, $I_F = 1.5A$

Notes:
1. All D.C. parameters 100% tested (pulse test: 300µs pulse, 2% duty cycle).
2. All A.C. parameters sample tested.
3. Refer to device types TN06L and TP06L for characteristic curves.

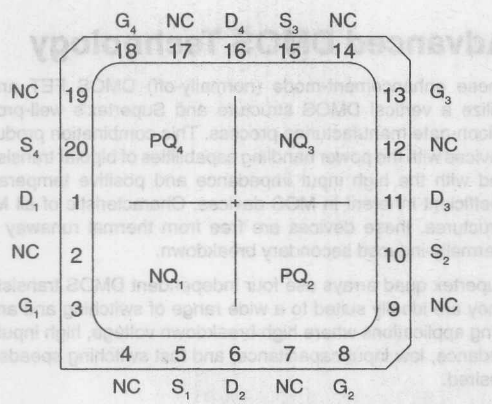
Switching Waveforms and Test Circuit



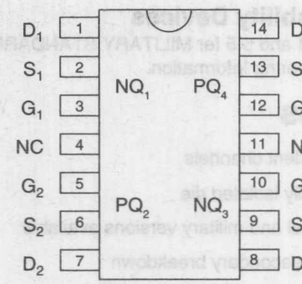


FET polarity in test circuit is N-channel only.

Pin Configurations



20-pin Ceramic LCC



top view
14-pin DIP

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Supertex inc.

VC0106N6
VC0106N7

Complementary Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max) Q1 + Q2 or Q3 + Q4	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
60V	11Ω	VC0106N6	VC0106N7

* 14-pin Side Brazed Ceramic Dip.

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)
- ☐ Amplifiers
- ☐ Switches

Thermal Characteristics

Package		Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	N-Channel	0.56A	0.7A
	P-Channel	-0.35A	-0.4A
I_D pulsed⁺ & I_{DRM}⁺	N-Channel	2.0A	2.0A
	P-Channel	-1.0A	-1.0A
Power Dissipation @ $T_C = 25°C$‡		2W	3W
θ_{ja} (°C/W)‡		110	83.3
θ_{jc} (°C/W)‡		62.5	41.6

⁺ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

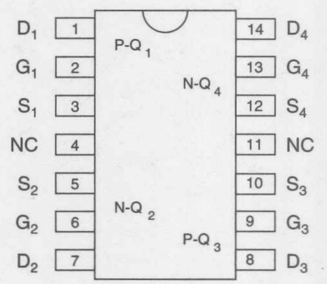
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN01A and VP01A data sheets for detailed characteristics of N- and P-channel devices.

Pin Configuration



top view
14-pin DIP

VN0104N6 / VN0104N7
VN0106N6 / VN0106N7

N-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
40V	3Ω	VN0104N6	VN0104N7
60V	3Ω	VN0106N6	VN0106N7

* 14-pin Side Brazed Ceramic Dip.

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)
- ☐ Amplifiers
- ☐ Switches

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	0.56A	0.7A
I_D pulsed$^+$ & $I_{DRM}$$^+$	2.0A	2.0A
Power Dissipation @ $T_C = 25°C$‡	2W	3W
θ_{ja} (°C/W)‡	110	83.3
θ_{jc} (°C/W)‡	62.5	41.6

$^+$ Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN01A data sheet for detailed characteristics.

Pin Configuration

top view
14-pin DIP

VP0104N6 / VP0104N7
VP0106N6 / VP0106N7

P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package	
		14-Pin P-DIP	14-Pin C-DIP*
-40V	8Ω	VP0104N6	VP0104N7
-60V	8Ω	VP0106N6	VP0106N7

* 14-pin Side Brazed Ceramic DIP.

Features

- ☐ 4 independent channels
- ☐ 4 electrically isolated die
- ☐ Commercial and military versions available
- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Low C_{ISS} and fast switching speeds
- ☐ High input impedance and high gain

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Power supply circuits
- ☐ Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)
- ☐ Amplifiers
- ☐ Switches

Thermal Characteristics

Package	Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	-0.35A	-0.4A
I_D pulsed† & I_{DRM}†	-1.0A	-1.0A
Power Dissipation @ $T_C = 25°C$‡	2W	3W
θ_{ja} (°C/W)‡	110	83.3
θ_{jc} (°C/W)‡	62.5	41.6

† Pulse test 300 µS pulse, 2% duty cycle.
‡ Total for package.

Advanced DMOS Technology

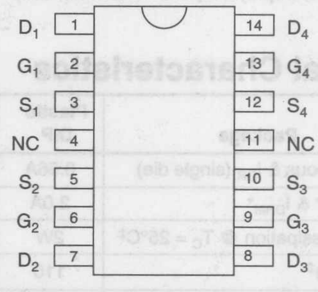
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VP01A Data Sheet for detailed characteristics.

Pin Configuration



top view
14-pin DIP

Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			14-Pin P-DIP	14-Pin C-DIP*
60V	5.5Ω	0.5A	VQ1000N6	VQ1000N7

* 14 pin side brazed ceramic DIP

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Very high input impedance
- Very high speed
- Low on-resistance
- No secondary breakdown
- High reliability

Applications

- Logic to high current interface
- High speed line driver
- LED digit strobe driver
- Linear amplifiers
- Stepper motor drive

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

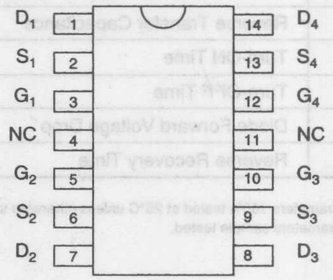
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

14-pin DIP

Thermal Characteristics (@ $T_A = 25°C$)

Test	Unit	Each Transistor	All four Transistors VQ1000N7
Total Power Dissipation	Watts	1.30	2.0
Thermal Resistance	°C/W	96.2	62.5
Thermal Coupling Factor (K)			
Q_1 - Q_4 or Q_2 - Q_3	%	60	
Q_1 - Q_2, Q_3 - Q_4, Q_1 - Q_3 or Q_4 - Q_2	%	50	
Continuous Drain Current [2, 3]	A	0.225	—
Pulsed Drain Current [1, 3]	A	1.0	—

Notes:
1. All D.C. parameter 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs, 2% duty cycle.)
2. I_D (continuous) is limited by max rated T_j.
3. $T_C = 25°C$.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V$, $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.0	-5.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
				500		$V_{GS} = 0$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	0.5			A	$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			7.5	Ω	$V_{GS} = 5V$, $I_D = 0.2A$
				5.5		$V_{GS} = 10V$, $I_D = 0.3A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.6	1.1	%/°C	$V_{GS} = 10V$, $I_D = 0.3A$
G_{FS}	Forward Transconductance	100			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			60	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 15V$, $I_D = 0.6A$ $R_{GEN} = 50\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.85		V	$V_{GS} = 0$, $I_{SD} = 0.5A$
t_{rr}	Reverse Recovery Time		165		ns	$V_{GS} = 0$, $I_{SD} = 0.3A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Thermal Coupling and Effective Thermal Resistance

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

$$\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4} \quad (1)$$

where ΔT_{J1} is the change injunction temperature of die 1.

$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4.

P_{D1} thru 4 is the power dissipated in die 1 through 4.

$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

$$R_{\theta\,(EFF)} = \Delta T_{J1}/P_{DT} \quad (2)$$

where P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

$$\Delta T_{J1} = R_{\theta 1}(P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4}) \quad (3)$$

For conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4P_D$, equation (3) can be further simplifed and, by substituting into equation (2), results in:

$$R\theta_{(EFF)} = R_{\theta 1}\,(1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4 \quad (4)$$

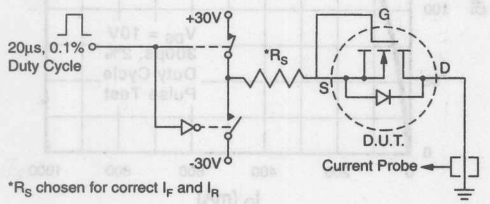
Values for the coupling factors when the ambient is used as a reference are given in the previous table. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest position junction temperatures will result.

Drain-Source Diode (t_{rr} - Reverse Recovery Time)

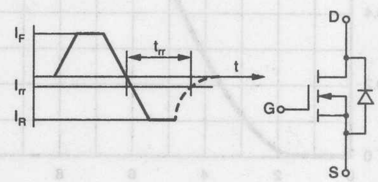
The internal drain-source diodes of DMOS FETs may be used as catch diodes or free-wheeling diodes. Current ratings for these diodes are the same as the contnuous and peak drain current ratings for the DMOS FET.

Reverse recovery time is measured using the circuit below. Forward and reverse current I_F and I_R are equal and are tested at the continuous and peak current ratings of the DMOS FET.

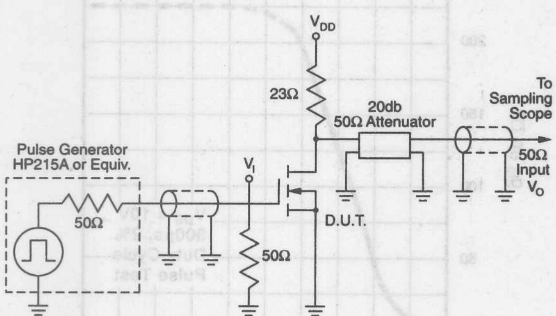
Switching Waveforms and Test Circuits



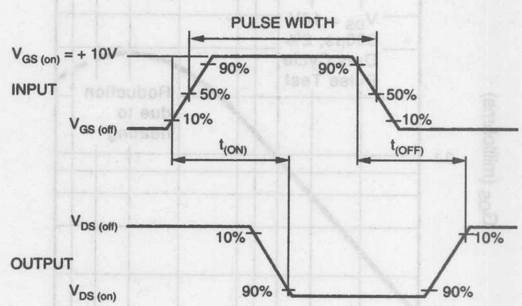
T_{RR} **Test Circuit**



T_{RR} **Test Waveforms**



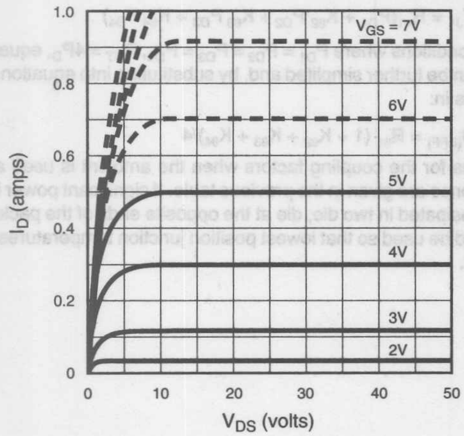
Switching Time Test Circuit



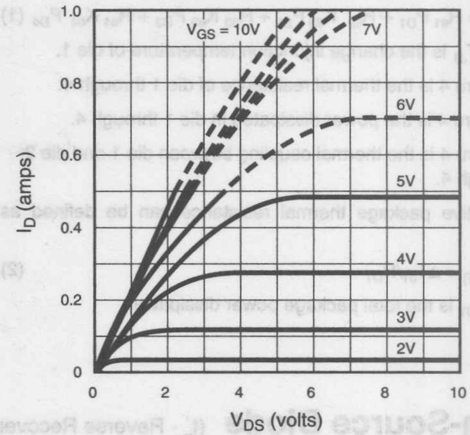
Switching Time Test Waveform

Typical Performance Curves

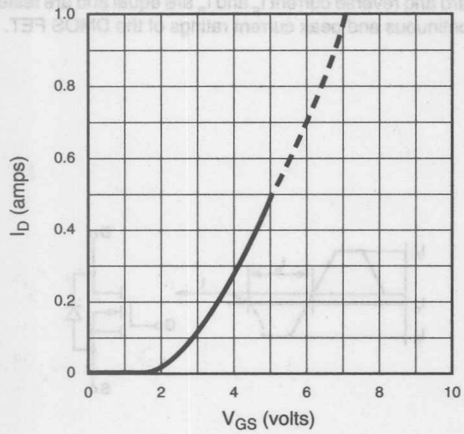
Output Characteristics



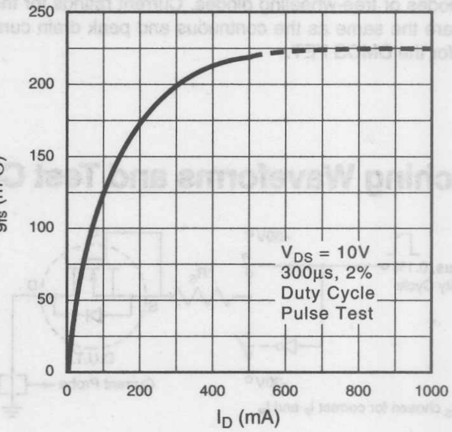
Saturation Characteristics



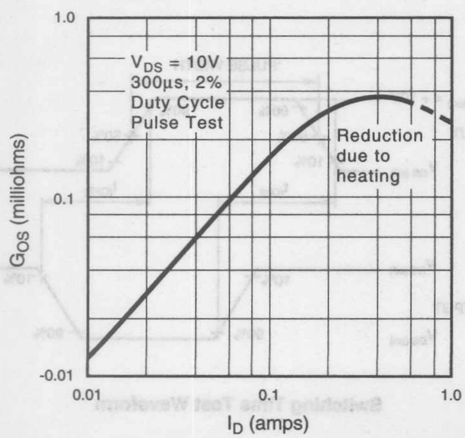
Static Transfer Characteristics



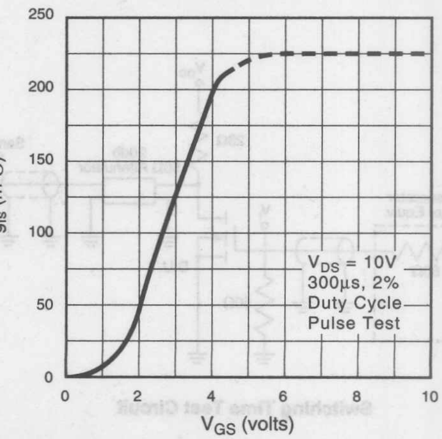
Transconductance vs. Drain Current



Output Conductance vs. Drain Current

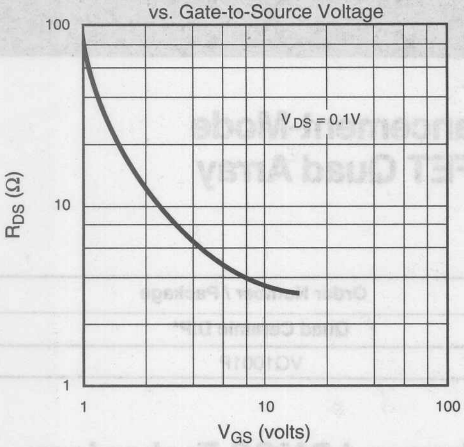


Transconductance vs. Gate-Source Voltage

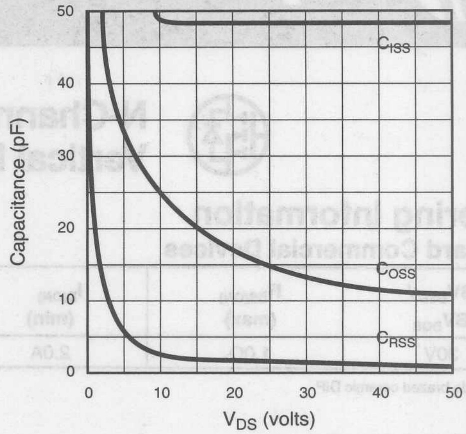


Typical Performance Curves

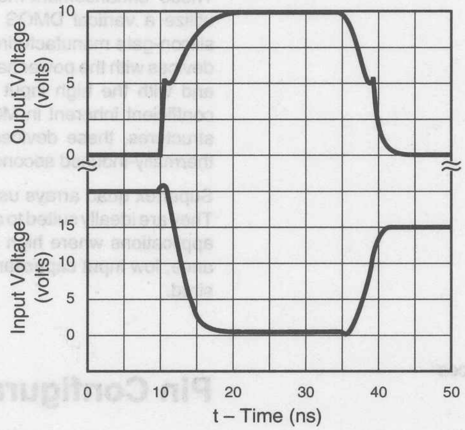
Drain-to-Source ON Resistance vs. Gate-to-Source Voltage



Capacitance vs. Drain-to-Source Voltage



Switching Speed



N-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package Quad Ceramic DIP*
30V	1.0Ω	2.0A	VQ1001P

* 14 pin side brazed ceramic DIP

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

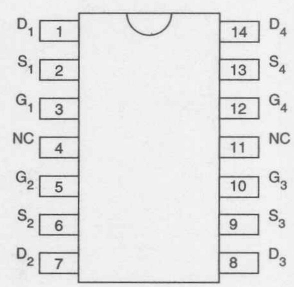
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view
14-pin DIP

Thermal Characteristics

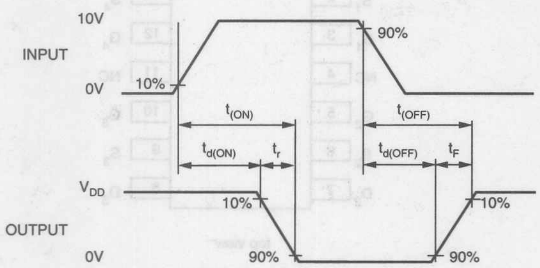
Test	Unit	Each Transistor VQ1001P	All Four Transistors VQ1001P
Total Power Dissipation	Watts	1.3	2.0
Thermal Resistance	°C/W	96.2	62.5
Continuous Drain Current	A	0.85	
Pulsed Drain Current	A	3.0	

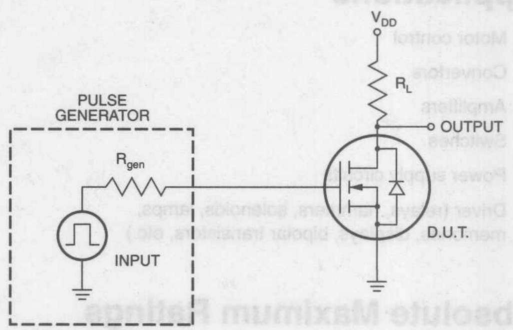
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30			V	$V_{GS} = 0V$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0V$, V_{DS} = Max Rating
				500		$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	2			A	$V_{GS} = 12V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1	Ω	$V_{GS} = 12V$, $I_D = 1.0A$
G_{FS}	Forward Transconductance	200			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			110	pF	$V_{GS} = 0$, $V_{DS} = 15V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			110		
C_{RSS}	Reverse Transfer Capacitance			35		
$t_{(ON)}$	Turn-ON Time			30	ns	$V_{DD} = 15V$, $I_D = 0.6A$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			30		
V_{SD}	Diode Forward Voltage Drop		0.85		V	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

VQ1004

N-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			Quad Ceramic DIP*	Quad Plastic DIP
60V	3.5Ω	1.5A	VQ1004P	VQ1004J

* 14 pin side brazed ceramic DIP

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

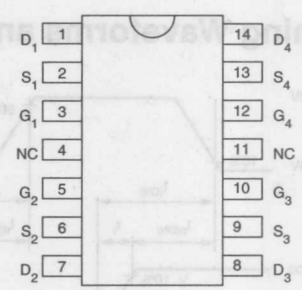
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

14-pin DIP

Thermal Characteristics

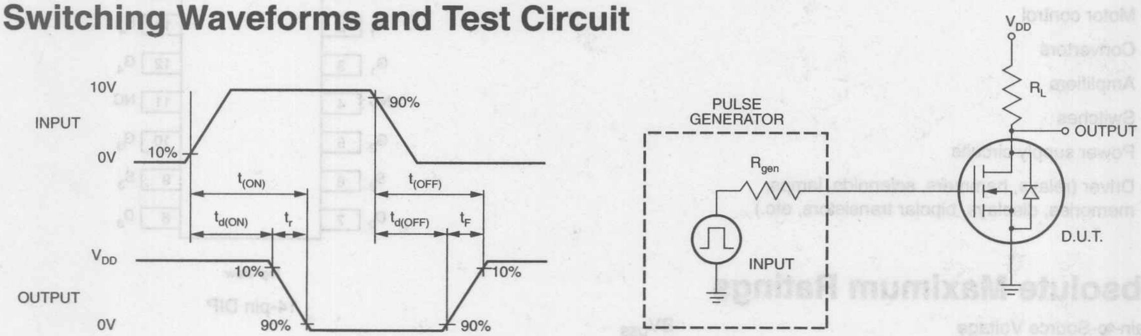
Test	Unit	Each Transistor		All Four Transistors	
		VQ1004P	VQ1004J	VQ1004P	VQ1004J
Total Power Dissipation	Watts	1.3	1.3	2.0	2.0
Thermal Resistance	°C/W	96.2	96.2	62.5	62.5
Continuous Drain Current	A	0.46	0.46		
Pulsed Drain Current	A	2.0	2.0		

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.5	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			1	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
				500		$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	1.5			A	$V_{GS} = 10V$, $V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
				3.5		$V_{GS} = 10V$, $I_D = 1.0A$
G_{FS}	Forward Transconductance	170			m℧	$V_{DS} = 10V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			60	pF	$V_{GS} = 0V$, $V_{DS} = 15V$, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			50		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 25V$, $I_D = 1A$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.9		V	$V_{GS} = 0$, $I_{SD} = 1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



VQ2001

Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package Quad Ceramic DIP*
-30V	2.0Ω	-1.5A	VQ2001P

* 14-pin side-brazed ceramic DIP.

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

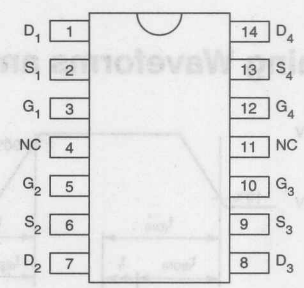
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Pin Configuration



top view

14-pin DIP

Thermal Characteristics ($T_A = 25°C$)

Test	Unit	Each Transistor	All Four Transistors
Total Power Dissipation	Watts	1.3	2.0
Thermal Resistance	°C/W	96.2	62.5
Continuous Drain Current	A	-0.6	—
Pulsed Drain Current	A	-2.0	—

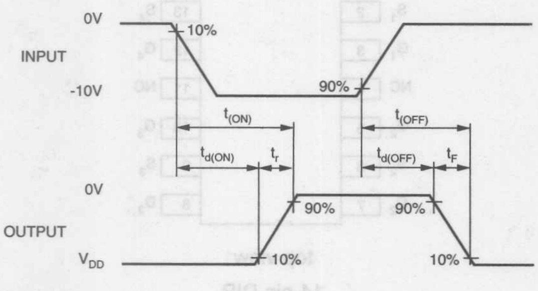
Electrical Characteristics (@ 25°C unless otherwise specified)

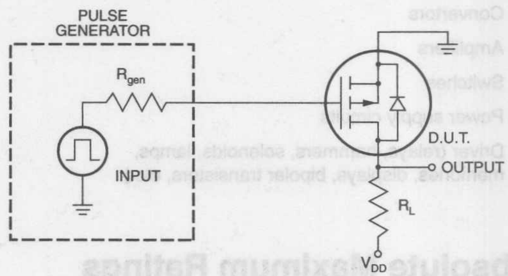
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30			V	V_{GS} = 0V, V_{DS}= -10µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.4	-1.8	-4.5	V	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±15V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-10	µA	V_{GS} = 0V, V_{DS}= Max Rating
				-500		V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-1.5			A	V_{GS} = -12V, V_{DS} = -10V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		1.5	2.0	Ω	V_{GS} = -12V, I_D = -1A
G_{FS}	Forward Transconductance	200			m℧	V_{DS} = -10V, I_D = -0.5A
C_{ISS}	Input Capacitance			150	pF	V_{GS} = 0V, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			120		
C_{RSS}	Reverse Transfer Capacitance			60		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = -15V, I_D = -0.6A
$t_{(OFF)}$	Turn-OFF Time			30	ns	R_{GEN} = 25Ω
V_{SD}	Diode Forward Voltage Drop			-1.8	V	V_{GS} = 0, I_{SD} = -1A

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package Quad Ceramic DIP*
-90V	5.0Ω	-1.0A	VQ2006P

* 14-pin side-brazed ceramic DIP.

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

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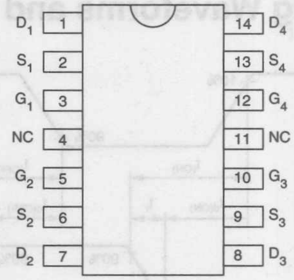
Pin Configuration



top view
14-pin DIP

Thermal Characteristics ($T_A = 25°C$)

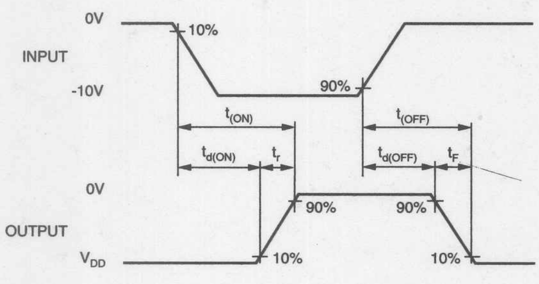
Test	Unit	Each Transistor	All Four Transistors
Total Power Dissipation	Watts	1.3	2.0
Thermal Resistance	°C/W	96.2	62.5
Continuous Drain Current	A	-0.41	—
Pulsed Drain Current	A	-3.0	—

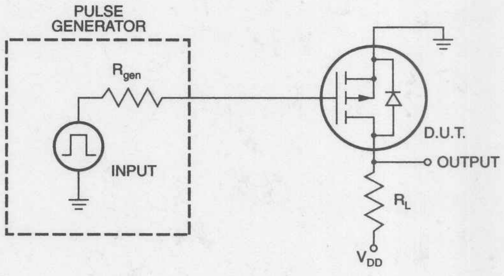
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-90			V	$V_{GS} = 0V$, $V_{DS}= -10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	-1.4	-1.8	-4.5	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm30V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			-10	µA	$V_{GS} = 0V$, V_{DS}= Max Rating
				-500	µA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	-1.0			A	$V_{GS} = -10V$, $V_{DS} = -10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2.5	5.0	Ω	$V_{GS} = -10V$, $I_D = -1A$
G_{FS}	Forward Transconductance	200			m ℧	$V_{DS} = -10V$, $I_D = -0.5A$
C_{ISS}	Input Capacitance			150	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			65	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{RSS}	Reverse Transfer Capacitance			25	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
t_r	Rise Time			15	ns	$V_{DD} = -25V$, $I_D = -0.5A$ $R_{GEN} = 25\Omega$
$t_{d(ON)}$	Turn-ON Delay Time			40	ns	$V_{DD} = -25V$, $I_D = -0.5A$ $R_{GEN} = 25\Omega$
t_f	Fall Time			30	ns	$V_{DD} = -25V$, $I_D = -0.5A$ $R_{GEN} = 25\Omega$
$t_{d(OFF)}$	Turn-OFF Delay Time			30	ns	$V_{DD} = -25V$, $I_D = -0.5A$ $R_{GEN} = 25\Omega$
V_{SD}	Diode Forward Voltage Drop			-1.8	V	$V_{GS} = 0$, $I_{SD} = -1A$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Chapter 11 – High Voltage Driver/Interface ICs

Supertex inc.

High-Voltage Integrated Circuit Custom Design and Process Capabilities

HVIC Custom Capabilities

Supertex, Inc. is a supplier of technologically-advanced high-voltage MOS transistors and integrated circuits. The standard devices in our catalogs are found in military, industrial and commercial applications requiring high voltage, high circuit density, low turn-on thresholds, and logic-plus-power on the same chip, known as high voltage integrated circuits (HVIC).

Some of the special applications of our HVICs include drivers for printer heads and plotters, flat panel displays (including plasma and electroluminescent, vacuum fluorescent and liquid crystal displays), medical ultrasound transducers, and bare-board testers. Our special high-voltage manufacturing and design capabilities have been used for many years to provide unique solutions for many customers. The capability summary shown here provides a brief overview of current Supertex custom capabilities to design and manufacture HVICs. These HVICs provide not only proprietary protection for our customers, but also offer them improved performance, lower power dissipation, better reliability, space savings and above all, lower total system cost.

High-Voltage Circuit Design

Supertex provides over twelve years of experience in high voltage integrated circuit design with true complementary N–channel and P–channel output configurations. These may be output devices for push-pull drive, or for fast pull-up or pull-down, providing high density with cost effectiveness. Supertex also offers proprietary low-power level translators for driving high-side drivers with minimal quiescent dissipation.

By design, our logic circuitry is particularly latch-up resistant for increased reliability in noisy environments. This is especially important because many circuits need to perform beyond 20MHz, as in high speed graphic equipment. Where higher speeds are needed, multiple shift registers can be put on a chip for parallel multiplex feeds to conserve power dissipation.

Standard High-Voltage Processes

The foundation for any semiconductor manufacturer is process technology. At Supertex, we have developed and refined a family of high-voltage CMOS/DMOS processes, working closely with our customers for over ten years. They are summarized as follows:

HVCMOS I:	160V or ±80V analog switch with 12V CMOS logic
HVCMOS II-S1:	80V push-pull, 400V open drain with 5V or 12V CMOS logic
HVCMOS II-S2:	275V push-pull with 5V or 12V CMOS logic
HVCMOS III:	200V bilateral analog switch with 5V or 12V CMOS logic

The choice of 5V or 12V is usually dictated by logic interface (5V) or noise-immunity and higher turn-on (12V) requirements. These processes produce truly low power CMOS designs. Our HVICs have low power dissipation that are uniquely suited for low cost high pin count packages.

Custom Product Capability Summary

	Open-Drain Outputs (N-Channel or P-Channel)	Complementary Push-Pull Outputs	Analog Output
Output Breakdown Voltage	30V–400V	30V–275V	30V–160V
Output Current	10µA–3A	10µA–1A	10µA–1A
Number of Outputs	1–160	1–160	1–32
Logic Supply Voltage	5V or 12V		
Package Material	Ceramic or Plastic		
Package Types	J-Lead (PLCC), Gullwing†, DIP, or Dice		
Temperature Ranges	0° to 70°C (commercial), -40° to 85°C (industrial), -55° to 125°C (military)		
Technologies	CMOS/DMOS, Analog, Digital, or Mixed Signal		
Frequencies	DC to Video		100kHz

†Flat packs with leads on 3 or 4 sides

11

Packages and Die Options

One of our main strengths is providing the advantages of high-voltage ICs in high pin count packages.

We can provide:

- Standard QFP packages up to 100 leads
- Special packages for more than 84 leads
- J-lead (PLCC), gullwing, or DIP packages
- Small-outline packages
- Custom lead frames and special lead bends
- Hybrids and arrays

These offerings provide space efficiency and reduced insertion costs to our customers. They are particularly appropriate in flat-panel displays and printer assemblies as well as other applications where space is at a premium. All offerings are available in industrial temperature range versions, and most can be supplied as military versions as well.

For the ultimate packaging density, we can supply dice. Using pad pitches down to 100 microns or less, with aspect ratios up to 7 to 1, optimum interface to printers and displays can be achieved. The user thus has several choices: die in waffle pack, in wafer form, or as bumped die for tape automated bonding (TAB); chip-on-glass or die on printed circuit board. All of these offer cost and space savings. However, packaged products provide testability and field repairability as well as the capability of machine (robot) insertion or placement.

Quality Monitoring

The latest statistical methods are used continuously to improve quality levels. Statistical Quality Control (SQC) is an ongoing tightening of such levels in-process.

Our Parts per Million (PPM) program is a continual feedback loop to ensure conformance to the customer's specifications using computerized data generated from each processed lot. Custom parts receive the same benefits from our Quality and Reliability Programs as standard parts. Supertex routinely supplies 883C parts to manufacturers of military equipment.

Reliability

We also have in-house activities to ensure the reliability of our products in the field. These include:

Reliability Monitoring Program - Lot samples are tested and monitored on a periodic basis for infant mortalities and long-term degradation.

Failure Analysis Laboratory - We have our own lab on the premises, with SEM, SRP, LCD thermal, and other analytical equipment. This lab enables us to get fast feedback for corrective action whenever necessary.

Our R & D departments are continually developing improved circuit and processing techniques for raising the electrostatic discharge (ESD) protection on our devices (presently at ±2KV). Manufactured parts are put in anti-static coated plastic tubes to protect them in shipment. All assembly facilities are meticulously inspected for adherence to ESD procedures.

Solutions to Design Needs

Supertex has a proven track record in the development and production of custom and semi-custom high voltage integrated circuits. Since its inception in 1976, Supertex has provided custom solutions for computers, military, telecommunications, medical instrumentation, and consumer products. Based on its pioneering HVCMOS® technology, and supported by a staff with uniquely diverse expertise and experience, Supertex provides the research and development environment which provides its customers with the most advanced solutions to custom and semi-custom HVIC requirements. A thorough understanding of customer requirements by our application engineers and circuit designers results in practical and commercially viable solutions. Working closely with its customers, Supertex develops meaningful time lines and specifications for production and provides continuous progress updates to ensure quality solutions on a timely basis.

If your product requires a custom or semi-custom high voltage integrated circuit, Supertex can provide you with the resources necessary to accomplish your goals. Contact your nearest Supertex sales office or the Sunnyvale headquarters directly to begin creating the solution to your custom or semi-custom HVIC requirements.

HV03
HV05

64-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options: 80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die	80-Lead Quad Cerpak Gullwing (MIL-STD-883 Processed*)
HV03	220V	HV0322DG	HV0322PG	HV0322T	HV0322X	RBHV0322DG
	300V	HV0330DG	HV0330PG	HV0330T	HV0330X	—
HV05	220V	HV0522DG	HV0522PG	HV0522T	HV0522X	RBHV0522DG
	300V	HV0530DG	HV0530PG	HV0530T	HV0530X	—

*For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- HVCMOS® technology
- Output voltages up to 300V using a ramped supply
- Sink current minimum 100 mA
- Shift register speed 8 MHz
- Latched outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +15V
Supply voltage, V_{PP}[2]		-0.5V to +315V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		6.0A
Continuous total power dissipation[4]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV03 and HV05 are low voltage serial to high voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic printheads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV03 shifts in the counterclockwise direction when viewed from the top of the package and the HV05 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV03 and HV05 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

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I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current				100	µA	All outputs high, All SWS parallel
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_I = 0V
V_{OH}	High-Level Output Data Out		V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			15	V	IHV_{OUT} = +100mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

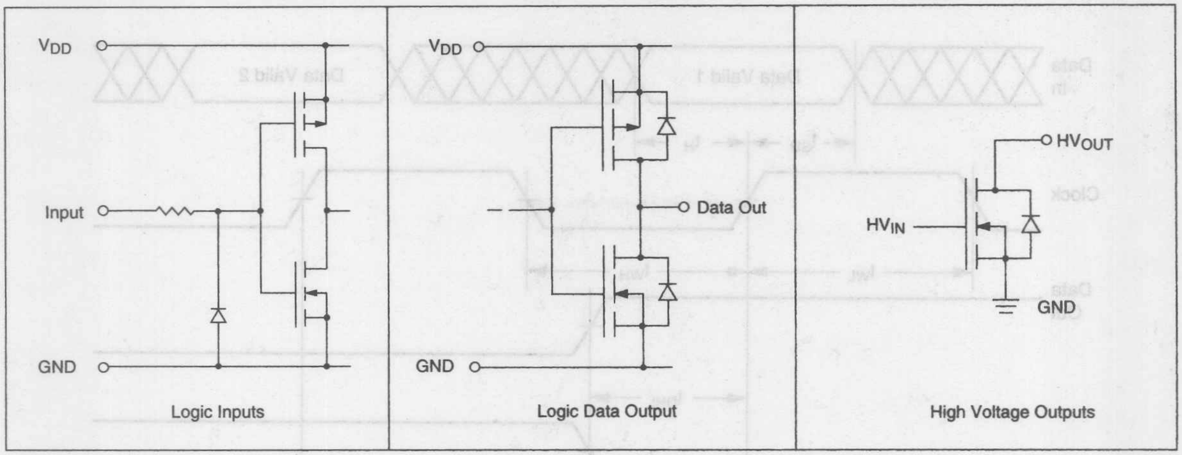
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Falls	25			ns	
t_H	Data Hold Time After Clock Falls	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Falling Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Falling Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in $\overline{LE}$, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from Falling Edge $\overline{LE}$ to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLK}	Delay Time Clock to Data Low to High			100	ns	

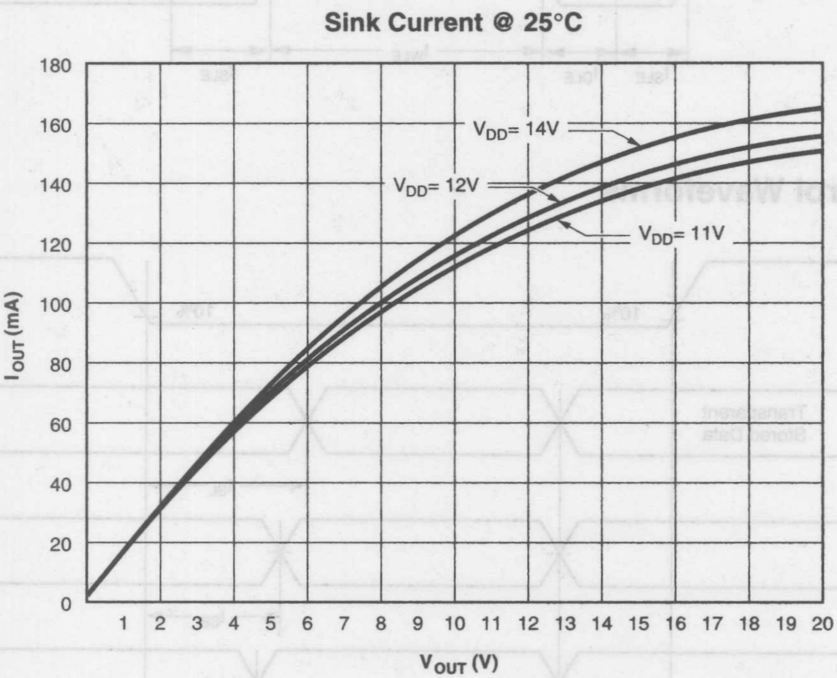
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply	HV0322/HV0522	-0.3		220	V
		HV0330/HV0530	-0.3		300	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
dV/dt	V_{PP} ramp rate				80	V/µs
T_A	Operating free-air temperature		-40		+85	°C

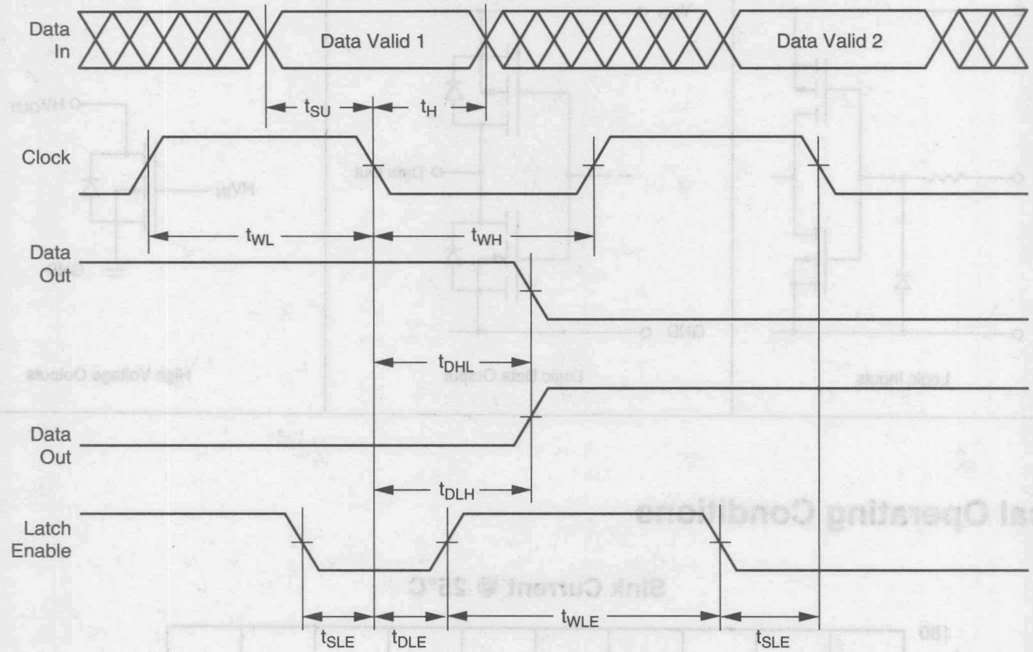
Input and Output Equivalent Circuit



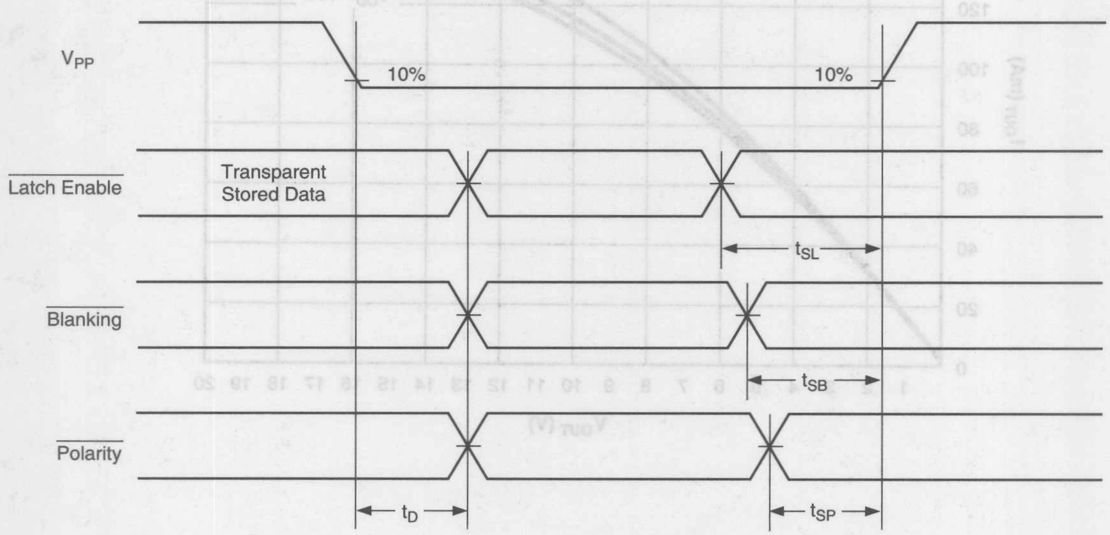
Typical Operating Conditions



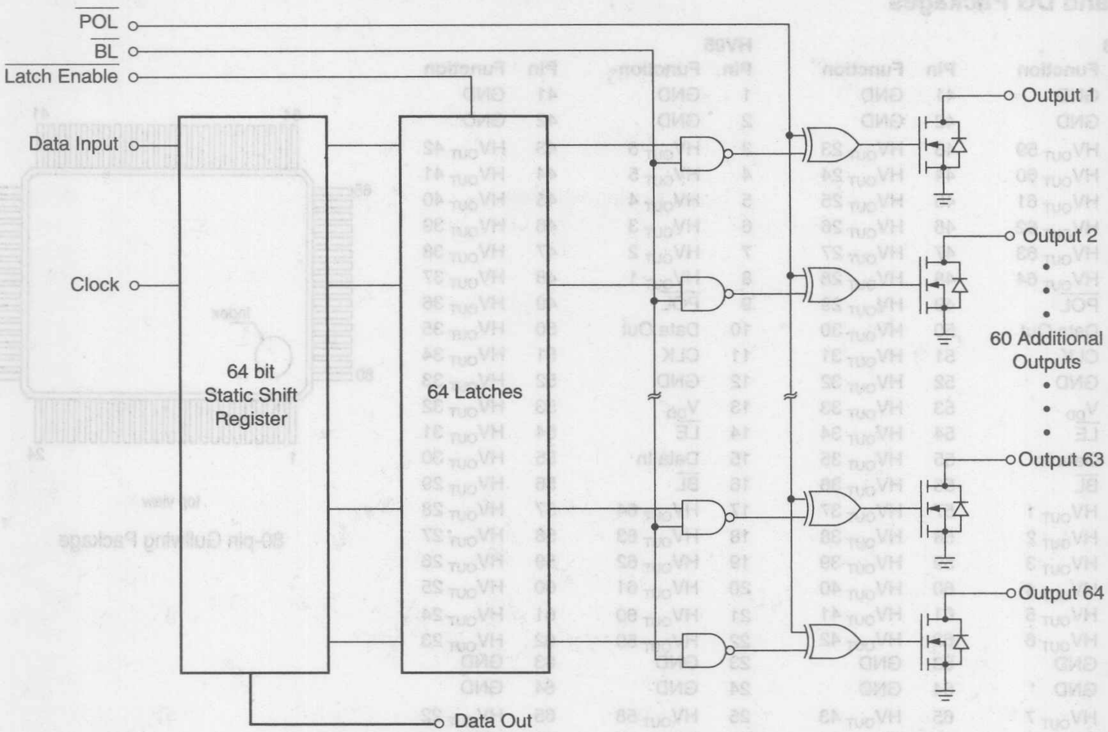
Switching Waveforms



Output Control Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…64	HV Outputs 1	HV Outputs 2…64	Data Out
All on	X	X	X	L	L	*	*…*	L	L…L	*
All off	X	X	X	L	H	*	*…*	H	H…H	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*…*	*	*…*	*
Load Latches	X	X	H	X	X	*	*…*	*	*…*	*
Transparent Latch mode	L	↓	H	H	H	L	*…*	H	*…*	*
	H	↓	H	H	H	H	*…*	L	*…*	*

Notes:
H = high level, L = low level, X = irrelevant, ↓= high-to-low transition.
* = dependent on previous stage's state before the last CLK or last LE high.

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Pin Configurations

PG and DG Packages

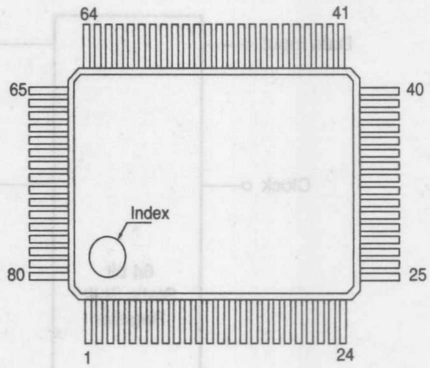
HV03

Pin	Function	Pin	Function
1	GND	41	GND
2	GND	42	GND
3	HV_{OUT} 59	43	HV_{OUT} 23
4	HV_{OUT} 60	44	HV_{OUT} 24
5	HV_{OUT} 61	45	HV_{OUT} 25
6	HV_{OUT} 62	46	HV_{OUT} 26
7	HV_{OUT} 63	47	HV_{OUT} 27
8	HV_{OUT} 64	48	HV_{OUT} 28
9	$\overline{POL}$	49	HV_{OUT} 29
10	Data Out	50	HV_{OUT} 30
11	CLK	51	HV_{OUT} 31
12	GND	52	HV_{OUT} 32
13	V_{DD}	53	HV_{OUT} 33
14	$\overline{LE}$	54	HV_{OUT} 34
15	Data In	55	HV_{OUT} 35
16	$\overline{BL}$	56	HV_{OUT} 36
17	HV_{OUT} 1	57	HV_{OUT} 37
18	HV_{OUT} 2	58	HV_{OUT} 38
19	HV_{OUT} 3	59	HV_{OUT} 39
20	HV_{OUT} 4	60	HV_{OUT} 40
21	HV_{OUT} 5	61	HV_{OUT} 41
22	HV_{OUT} 6	62	HV_{OUT} 42
23	GND	63	GND
24	GND	64	GND
25	HV_{OUT} 7	65	HV_{OUT} 43
26	HV_{OUT} 8	66	HV_{OUT} 44
27	HV_{OUT} 9	67	HV_{OUT} 45
28	HV_{OUT} 10	68	HV_{OUT} 46
29	HV_{OUT} 11	69	HV_{OUT} 47
30	HV_{OUT} 12	70	HV_{OUT} 48
31	HV_{OUT} 13	71	HV_{OUT} 49
32	HV_{OUT} 14	72	HV_{OUT} 50
33	HV_{OUT} 15	73	HV_{OUT} 51
34	HV_{OUT} 16	74	HV_{OUT} 52
35	HV_{OUT} 17	75	HV_{OUT} 53
36	HV_{OUT} 18	76	HV_{OUT} 54
37	HV_{OUT} 19	77	HV_{OUT} 55
38	HV_{OUT} 20	78	HV_{OUT} 56
39	HV_{OUT} 21	79	HV_{OUT} 57
40	HV_{OUT} 22	80	HV_{OUT} 58

HV05

Pin	Function	Pin	Function
1	GND	41	GND
2	GND	42	GND
3	HV_{OUT} 6	43	HV_{OUT} 42
4	HV_{OUT} 5	44	HV_{OUT} 41
5	HV_{OUT} 4	45	HV_{OUT} 40
6	HV_{OUT} 3	46	HV_{OUT} 39
7	HV_{OUT} 2	47	HV_{OUT} 38
8	HV_{OUT} 1	48	HV_{OUT} 37
9	$\overline{POL}$	49	HV_{OUT} 36
10	Data Out	50	HV_{OUT} 35
11	CLK	51	HV_{OUT} 34
12	GND	52	HV_{OUT} 33
13	V_{DD}	53	HV_{OUT} 32
14	$\overline{LE}$	54	HV_{OUT} 31
15	Data In	55	HV_{OUT} 30
16	$\overline{BL}$	56	HV_{OUT} 29
17	HV_{OUT} 64	57	HV_{OUT} 28
18	HV_{OUT} 63	58	HV_{OUT} 27
19	HV_{OUT} 62	59	HV_{OUT} 26
20	HV_{OUT} 61	60	HV_{OUT} 25
21	HV_{OUT} 60	61	HV_{OUT} 24
22	HV_{OUT} 59	62	HV_{OUT} 23
23	GND	63	GND
24	GND	64	GND
25	HV_{OUT} 58	65	HV_{OUT} 22
26	HV_{OUT} 57	66	HV_{OUT} 21
27	HV_{OUT} 56	67	HV_{OUT} 20
28	HV_{OUT} 55	68	HV_{OUT} 19
29	HV_{OUT} 54	69	HV_{OUT} 18
30	HV_{OUT} 53	70	HV_{OUT} 17
31	HV_{OUT} 52	71	HV_{OUT} 16
32	HV_{OUT} 51	72	HV_{OUT} 15
33	HV_{OUT} 50	73	HV_{OUT} 14
34	HV_{OUT} 49	74	HV_{OUT} 13
35	HV_{OUT} 48	75	HV_{OUT} 12
36	HV_{OUT} 47	76	HV_{OUT} 11
37	HV_{OUT} 46	77	HV_{OUT} 10
38	HV_{OUT} 45	78	HV_{OUT} 9
39	HV_{OUT} 44	79	HV_{OUT} 8
40	HV_{OUT} 43	80	HV_{OUT} 7

Package Outline



top view

80-pin Gullwing Package

Supertex inc.

HV04
HV06

64-Channel Serial To Parallel Converter With High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options				
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die	80-Lead Quad Cerpak Gullwing (MIL-STD-883 Processed*)
HV04	60V	HV0406DG	HV0406PG	HV0406T	HV0406X	—
	80V	HV0408DG	HV0408PG	HV0408T	HV0408X	RBHV0408DG
HV06	60V	HV0606DG	HV0606PG	HV0606T	HV0606X	—
	80V	HV0608DG	HV0608PG	HV0608T	HV0608X	RBHV0608DG

* For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- ☐ HVCMOS® technology
- ☐ Output voltages up to 90V using a ramped supply
- ☐ Low power level shifting
- ☐ Shift register speed 8 MHz
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +15V
Supply voltage, V_{PP}[2]		-0.5V to +90V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		3.0A
High voltage supply current[3]		2.6A
Continuous total power dissipation[4]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C

Notes:

1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

Not recommended for new designs. Please use HV577, with improved performance.

The HV04 and HV06 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04 shifts in the counterclockwise direction when viewed from the top of the package and the HV06 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV04 and HV06 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 80V All outputs high
					0.50	mA	V_{PP} = 80V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_I = 0V
V_{OH}	High-Level Output	HV_{OUT}	74			V	V_{PP} = 80V, IHV_{OUT} = -20mA
		Data Out	V_{DD} - 1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			6	V	V_{PP} = 80V, IHV_{OUT} = +10mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} + 1.5	V	I_{OL} = +10mA
					-1.5	V	I_{OL} = -20mA

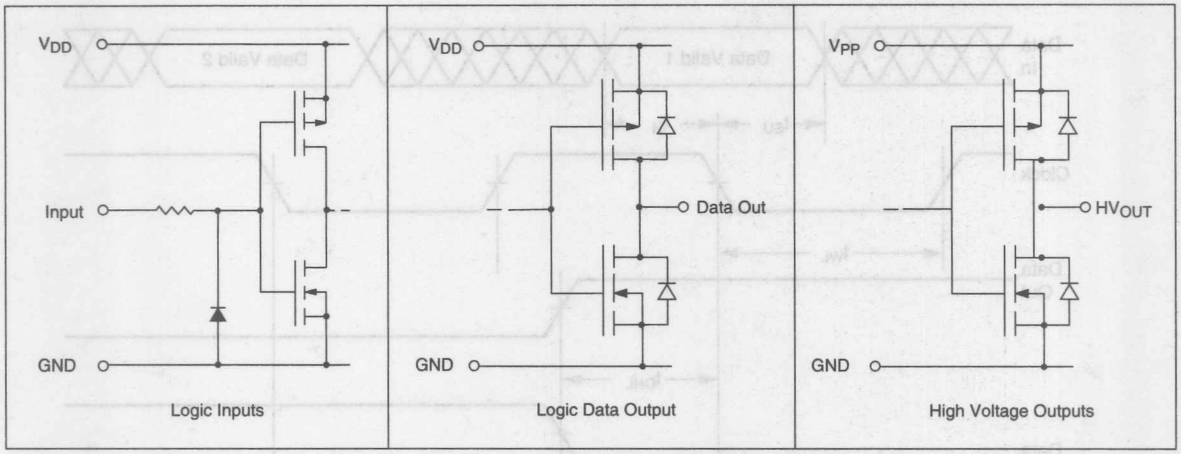
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in $\overline{LE}$, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from $\overline{LE}$ Rise to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

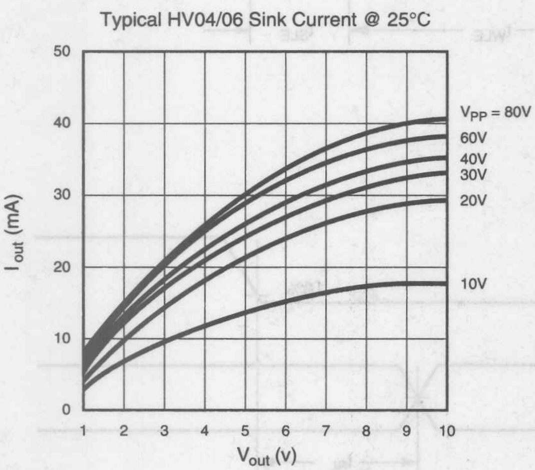
Recommended Operating Conditions

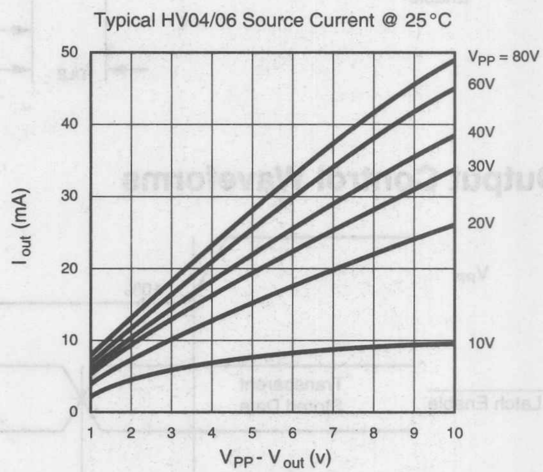
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
dV/dt	V_{PP} ramp rate			80	V/µs
T_A	Operating free-air temperature	-40		+85	°C

Input and Output Equivalent Circuits

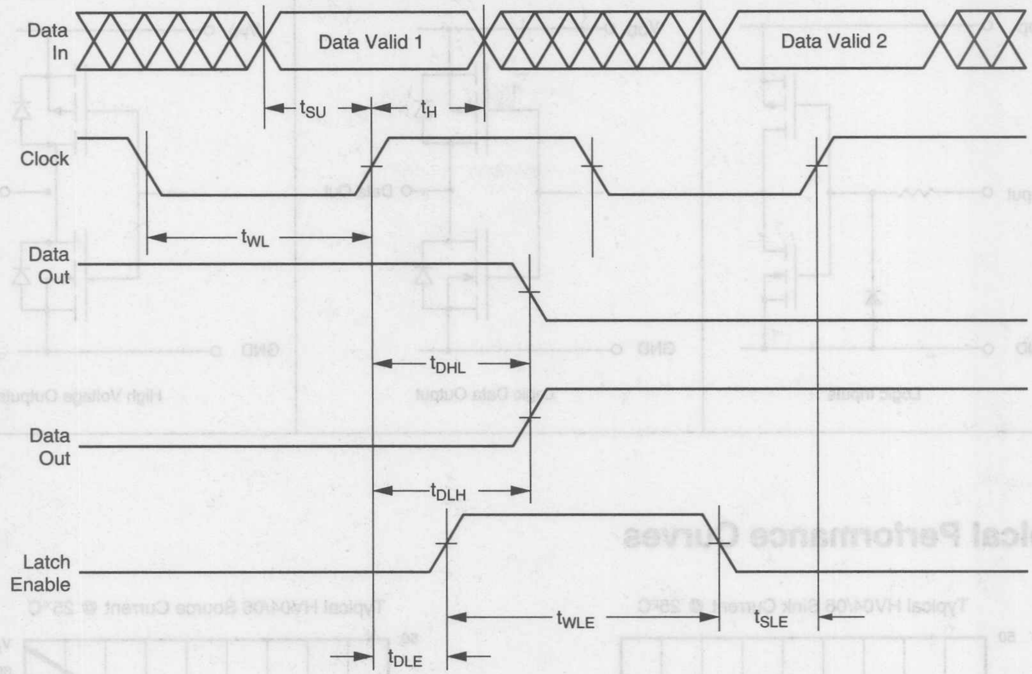


Typical Performance Curves

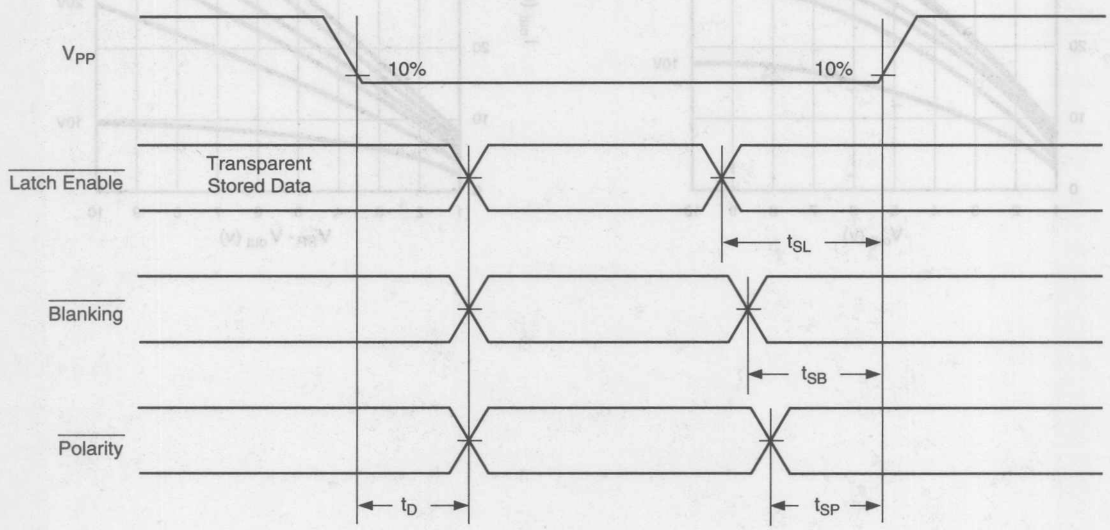




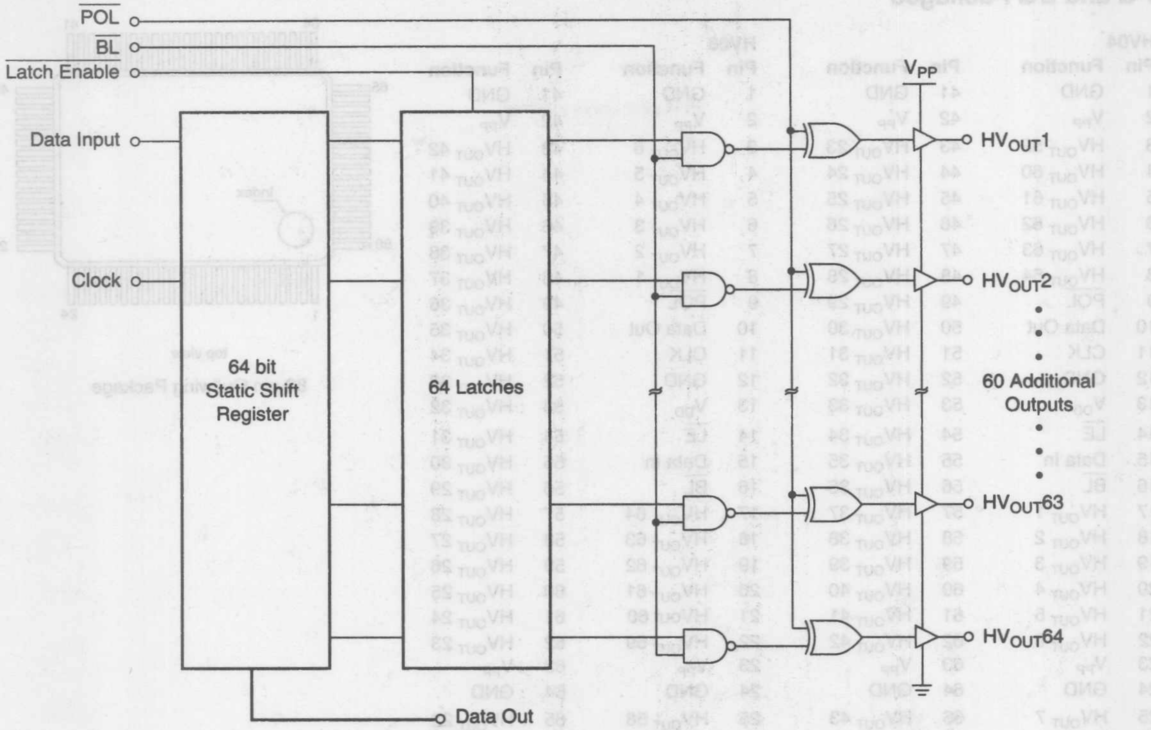
Switching Waveforms



Output Control Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…64	HV Outputs 1	HV Outputs 2…64	Data Out *
All on	X	X	X	L	L	*	*…*	H	H…H	*
All off	X	X	X	L	H	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*…*	*	*…*	*
Load Latches	X	H or L	H	H	H	*	*…*	*	*…*	*
	X	H or L	H	H	L	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Transparent Latch mode	L	↑	H	H	H	L	*…*	L	*…*	*
	H	↑	H	H	H	H	*…*	H	*…*	*

Notes:

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.

* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

Pin Configurations

PG and DG Packages

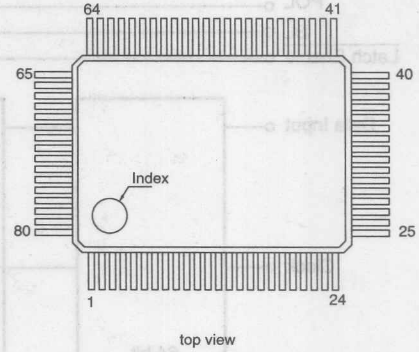
HV04

Pin	Function	Pin	Function
1	GND	41	GND
2	V_{PP}	42	V_{PP}
3	HV_{OUT} 59	43	HV_{OUT} 23
4	HV_{OUT} 60	44	HV_{OUT} 24
5	HV_{OUT} 61	45	HV_{OUT} 25
6	HV_{OUT} 62	46	HV_{OUT} 26
7	HV_{OUT} 63	47	HV_{OUT} 27
8	HV_{OUT} 64	48	HV_{OUT} 28
9	$\overline{POL}$	49	HV_{OUT} 29
10	Data Out	50	HV_{OUT} 30
11	CLK	51	HV_{OUT} 31
12	GND	52	HV_{OUT} 32
13	V_{DD}	53	HV_{OUT} 33
14	$\overline{LE}$	54	HV_{OUT} 34
15	Data In	55	HV_{OUT} 35
16	$\overline{BL}$	56	HV_{OUT} 36
17	HV_{OUT} 1	57	HV_{OUT} 37
18	HV_{OUT} 2	58	HV_{OUT} 38
19	HV_{OUT} 3	59	HV_{OUT} 39
20	HV_{OUT} 4	60	HV_{OUT} 40
21	HV_{OUT} 5	61	HV_{OUT} 41
22	HV_{OUT} 6	62	HV_{OUT} 42
23	V_{PP}	63	V_{PP}
24	GND	64	GND
25	HV_{OUT} 7	65	HV_{OUT} 43
26	HV_{OUT} 8	66	HV_{OUT} 44
27	HV_{OUT} 9	67	HV_{OUT} 45
28	HV_{OUT} 10	68	HV_{OUT} 46
29	HV_{OUT} 11	69	HV_{OUT} 47
30	HV_{OUT} 12	70	HV_{OUT} 48
31	HV_{OUT} 13	71	HV_{OUT} 49
32	HV_{OUT} 14	72	HV_{OUT} 50
33	HV_{OUT} 15	73	HV_{OUT} 51
34	HV_{OUT} 16	74	HV_{OUT} 52
35	HV_{OUT} 17	75	HV_{OUT} 53
36	HV_{OUT} 18	76	HV_{OUT} 54
37	HV_{OUT} 19	77	HV_{OUT} 55
38	HV_{OUT} 20	78	HV_{OUT} 56
39	HV_{OUT} 21	79	HV_{OUT} 57
40	HV_{OUT} 22	80	HV_{OUT} 58

HV06

Pin	Function	Pin	Function
1	GND	41	GND
2	V_{PP}	42	V_{PP}
3	HV_{OUT} 6	43	HV_{OUT} 42
4	HV_{OUT} 5	44	HV_{OUT} 41
5	HV_{OUT} 4	45	HV_{OUT} 40
6	HV_{OUT} 3	46	HV_{OUT} 39
7	HV_{OUT} 2	47	HV_{OUT} 38
8	HV_{OUT} 1	48	HV_{OUT} 37
9	$\overline{POL}$	49	HV_{OUT} 36
10	Data Out	50	HV_{OUT} 35
11	CLK	51	HV_{OUT} 34
12	GND	52	HV_{OUT} 33
13	V_{DD}	53	HV_{OUT} 32
14	$\overline{LE}$	54	HV_{OUT} 31
15	Data In	55	HV_{OUT} 30
16	$\overline{BL}$	56	HV_{OUT} 29
17	HV_{OUT} 64	57	HV_{OUT} 28
18	HV_{OUT} 63	58	HV_{OUT} 27
19	HV_{OUT} 62	59	HV_{OUT} 26
20	HV_{OUT} 61	60	HV_{OUT} 25
21	HVout 60	61	HV_{OUT} 24
22	HV_{OUT} 59	62	HV_{OUT} 23
23	V_{PP}	63	V_{PP}
24	GND	64	GND
25	HV_{OUT} 58	65	HV_{OUT} 22
26	HV_{OUT} 57	66	HV_{OUT} 21
27	HV_{OUT} 56	67	HV_{OUT} 20
28	HV_{OUT} 55	68	HV_{OUT} 19
29	HV_{OUT} 54	69	HV_{OUT} 18
30	HV_{OUT} 53	70	HV_{OUT} 17
31	HV_{OUT} 52	71	HV_{OUT} 16
32	HV_{OUT} 51	72	HV_{OUT} 15
33	HV_{OUT} 50	73	HV_{OUT} 14
34	HV_{OUT} 49	74	HV_{OUT} 13
35	HV_{OUT} 48	75	HV_{OUT} 12
36	HV_{OUT} 47	76	HV_{OUT} 11
37	HV_{OUT} 46	77	HV_{OUT} 10
38	HV_{OUT} 45	78	HV_{OUT} 9
39	HV_{OUT} 44	79	HV_{OUT} 8
40	HV_{OUT} 43	80	HV_{OUT} 7

Package Outline



80-pin Gullwing Package

Supertex inc.

HV04H
HV06H

64-Channel Serial To Parallel Converter With Ruggedized High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options: 80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die	80-Lead Quad Cerpak Gullwing (MIL-STD-883 Processed*)
HV04H	60V	HV04H06DG	HV04H06PG	HV04H06T	HV04H06X	—
	80V	HV04H08DG	HV04H08PG	HV04H08T	HV04H08X	RBHV04H08DG
HV06H	60V	HV06H06DG	HV06H06PG	HV06H06T	HV06H06X	—
	80V	HV06H08DG	HV06H08PG	HV06H08T	HV06H08X	RBHV06H08DG

* For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- HVCMOS® technology
- Output voltages up to 80V
- Low power level shifting
- Shift register speed 8 MHz
- Latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +15V
Supply voltage, V_{PP}		-0.5V to +80V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		3.0A
High voltage supply current[2]		2.6A
Continuous total power dissipation[3]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C

Notes:

1 All voltages are referenced to ground.
2. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

Not recommended for new designs. Please use HV577, with improved performance.

The HV04H and HV06H are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04H shifts data in the counterclockwise direction when viewed from the top of the package and the HV06H shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV04H and HV06H devices are ruggedized versions of our standard HV04 and HV06. They are designed to be used in circuits where ramping of the high voltage supply is not feasible. Care must be taken to limit the load capacitance and surge current in any particular application.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V or V_{DD}
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 80V All outputs high
					0.50	mA	V_{PP} = 80V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_{IL} = 0V
V_{OH}	High-Level Output	HV_{OUT}	74			V	V_{PP} = 80V, IHV_{OUT} = -20mA
		Data Out	V_{DD} - 1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			6.0	V	V_{PP} = 80V, IHV_{OUT} = +10mA
		Data Out			1.0	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} + 1.5	V	I_{OL} = +10mA
					-1.5	V	I_{OL} = -20mA

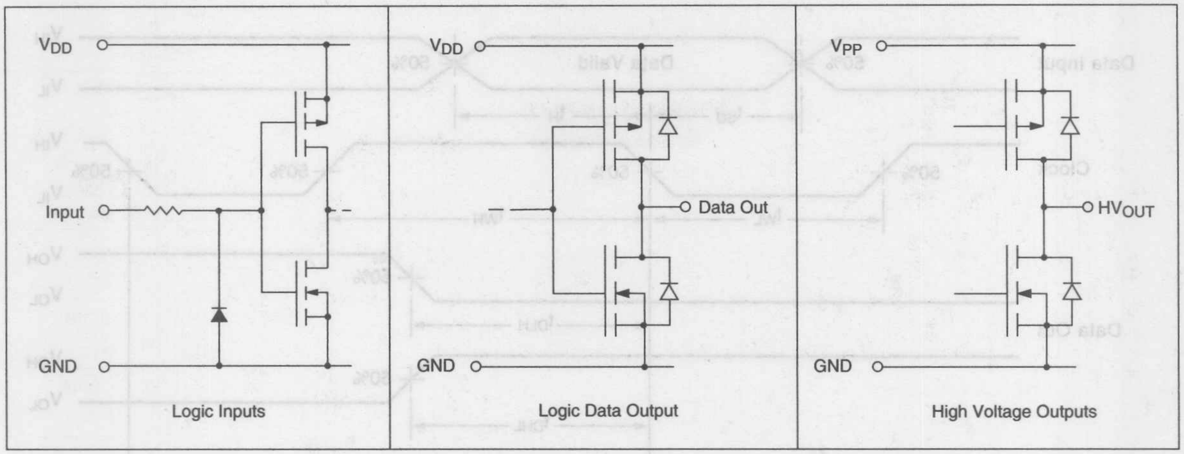
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30			ns	
t_{ON}, t_{OFF}	Time from Latch Enable to HV_{OUT}			50	ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

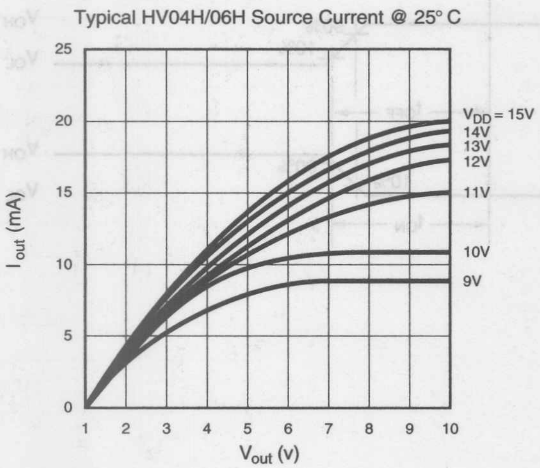
Recommended Operating Conditions

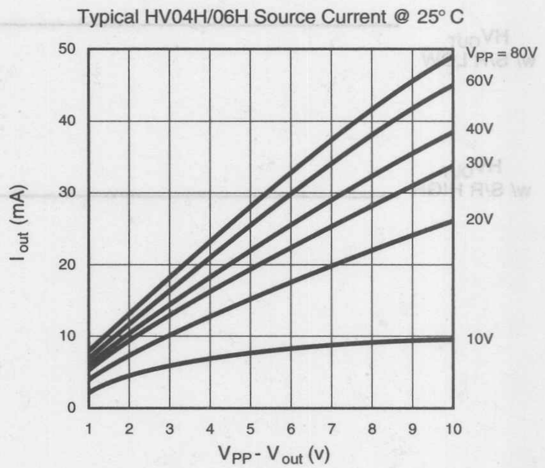
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
T_A	Operating free-air temperature	-40		+85	°C

Input and Output Equivalent Circuits

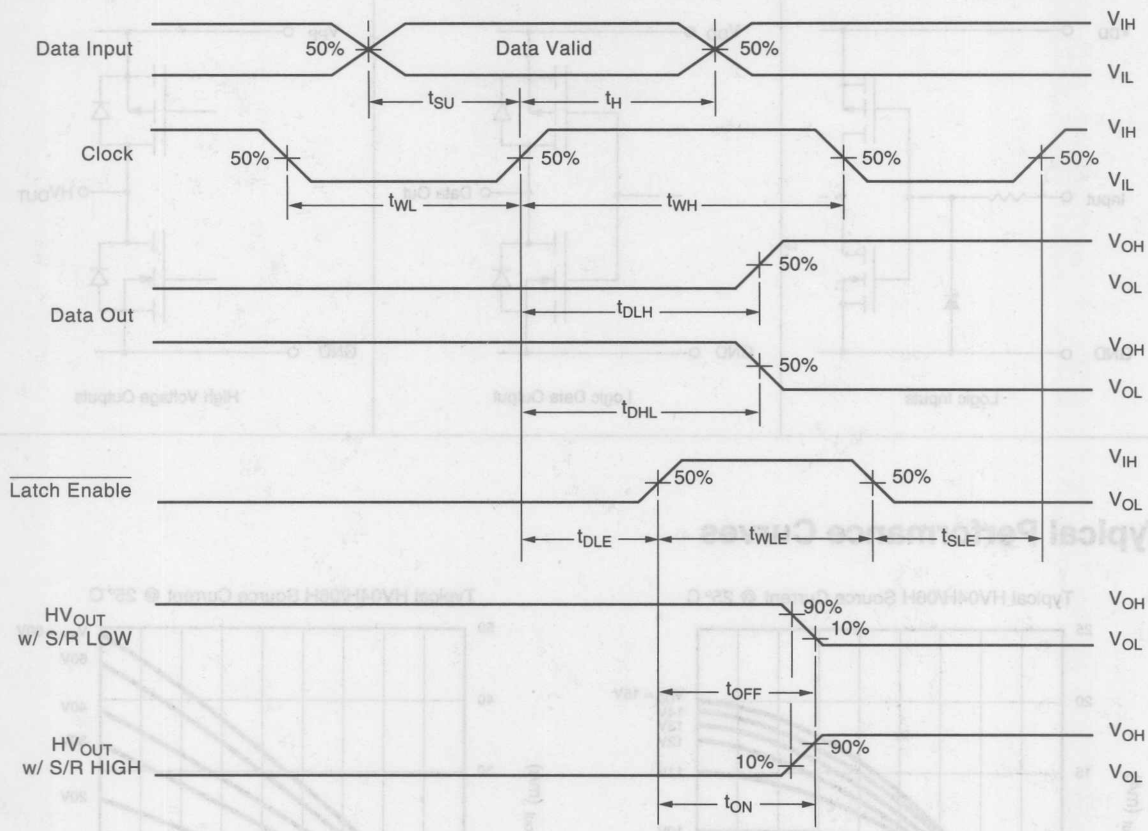


Typical Performance Curves

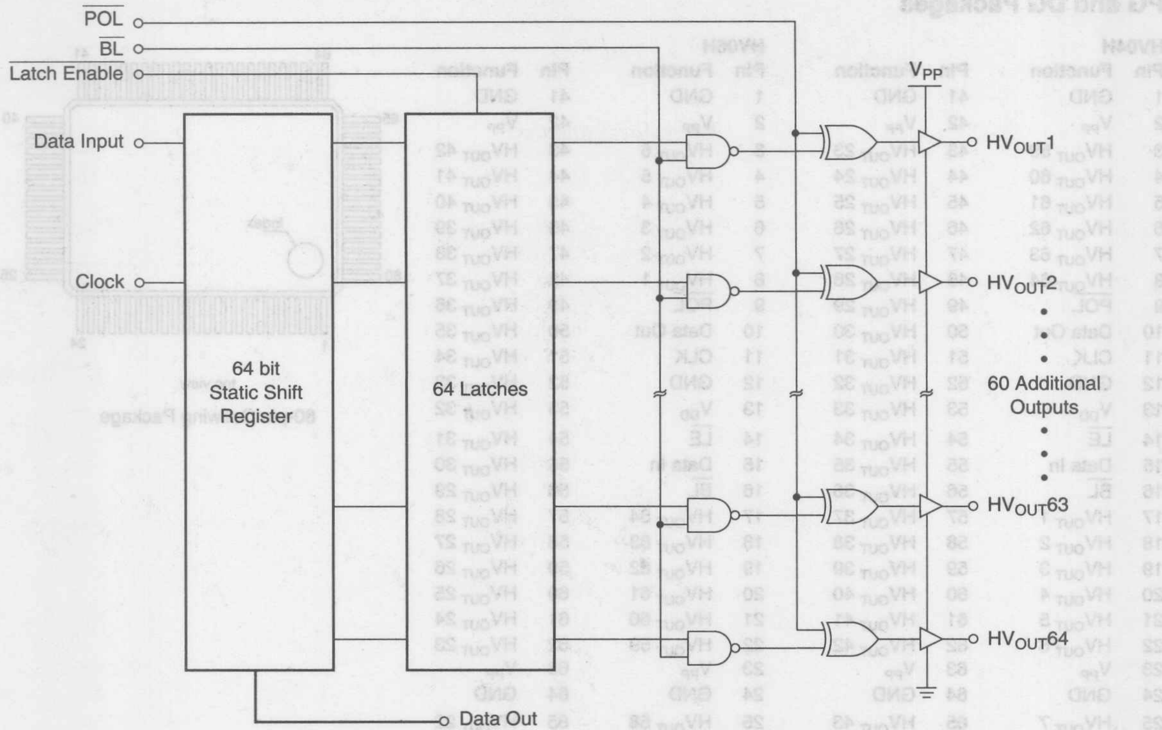




Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…64	HV Outputs 1	HV Outputs 2…64	Data Out
All on	X	X	X	L	L	*	*…*	H	H…H	*
All off	X	X	X	L	H	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*…*	*	*…*	*
Load Latches	X	H or L	↑	H	H	*	*…*	*	*…*	*
	X	H or L	↑	H	L	*	*…*	*	*…*	*
Transparent Latch mode	L	↑	H	H	H	L	*…*	L	*…*	*
	H	↑	H	H	H	H	*…*	H	*…*	*

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

Pin Configurations

PG and DG Packages

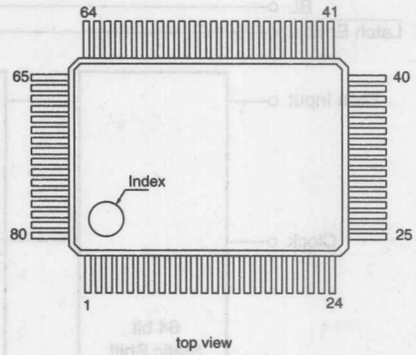
HV04H

Pin	Function	Pin	Function
1	GND	41	GND
2	V_{PP}	42	V_{PP}
3	HV_{OUT} 59	43	HV_{OUT} 23
4	HV_{OUT} 60	44	HV_{OUT} 24
5	HV_{OUT} 61	45	HV_{OUT} 25
6	HV_{OUT} 62	46	HV_{OUT} 26
7	HV_{OUT} 63	47	HV_{OUT} 27
8	HV_{OUT} 64	48	HV_{OUT} 28
9	$\overline{POL}$	49	HV_{OUT} 29
10	Data Out	50	HV_{OUT} 30
11	CLK	51	HV_{OUT} 31
12	GND	52	HV_{OUT} 32
13	V_{DD}	53	HV_{OUT} 33
14	$\overline{LE}$	54	HV_{OUT} 34
15	Data In	55	HV_{OUT} 35
16	$\overline{BL}$	56	HV_{OUT} 36
17	HV_{OUT} 1	57	HV_{OUT} 37
18	HV_{OUT} 2	58	HV_{OUT} 38
19	HV_{OUT} 3	59	HV_{OUT} 39
20	HV_{OUT} 4	60	HV_{OUT} 40
21	HV_{OUT} 5	61	HV_{OUT} 41
22	HV_{OUT} 6	62	HV_{OUT} 42
23	V_{PP}	63	V_{PP}
24	GND	64	GND
25	HV_{OUT} 7	65	HV_{OUT} 43
26	HV_{OUT} 8	66	HV_{OUT} 44
27	HV_{OUT} 9	67	HV_{OUT} 45
28	HV_{OUT} 10	68	HV_{OUT} 46
29	HV_{OUT} 11	69	HV_{OUT} 47
30	HV_{OUT} 12	70	HV_{OUT} 48
31	HV_{OUT} 13	71	HV_{OUT} 49
32	HV_{OUT} 14	72	HV_{OUT} 50
33	HV_{OUT} 15	73	HV_{OUT} 51
34	HV_{OUT} 16	74	HV_{OUT} 52
35	HV_{OUT} 17	75	HV_{OUT} 53
36	HV_{OUT} 18	76	HV_{OUT} 54
37	HV_{OUT} 19	77	HV_{OUT} 55
38	HV_{OUT} 20	78	HV_{OUT} 56
39	HV_{OUT} 21	79	HV_{OUT} 57
40	HV_{OUT} 22	80	HV_{OUT} 58

HV06H

Pin	Function	Pin	Function
1	GND	41	GND
2	V_{PP}	42	V_{PP}
3	HV_{OUT} 6	43	HV_{OUT} 42
4	HV_{OUT} 5	44	HV_{OUT} 41
5	HV_{OUT} 4	45	HV_{OUT} 40
6	HV_{OUT} 3	46	HV_{OUT} 39
7	HV_{OUT} 2	47	HV_{OUT} 38
8	HV_{OUT} 1	48	HV_{OUT} 37
9	$\overline{POL}$	49	HV_{OUT} 36
10	Data Out	50	HV_{OUT} 35
11	CLK	51	HV_{OUT} 34
12	GND	52	HV_{OUT} 33
13	V_{DD}	53	HV_{OUT} 32
14	$\overline{LE}$	54	HV_{OUT} 31
15	Data In	55	HV_{OUT} 30
16	$\overline{BL}$	56	HV_{OUT} 29
17	HV_{OUT} 64	57	HV_{OUT} 28
18	HV_{OUT} 63	58	HV_{OUT} 27
19	HV_{OUT} 62	59	HV_{OUT} 26
20	HV_{OUT} 61	60	HV_{OUT} 25
21	HV_{OUT} 60	61	HV_{OUT} 24
22	HV_{OUT} 59	62	HV_{OUT} 23
23	V_{PP}	63	V_{PP}
24	GND	64	GND
25	HV_{OUT} 58	65	HV_{OUT} 22
26	HV_{OUT} 57	66	HV_{OUT} 21
27	HV_{OUT} 56	67	HV_{OUT} 20
28	HV_{OUT} 55	68	HV_{OUT} 19
29	HV_{OUT} 54	69	HV_{OUT} 18
30	HV_{OUT} 53	70	HV_{OUT} 17
31	HV_{OUT} 52	71	HV_{OUT} 16
32	HV_{OUT} 51	72	HV_{OUT} 15
33	HV_{OUT} 50	73	HV_{OUT} 14
34	HV_{OUT} 49	74	HV_{OUT} 13
35	HV_{OUT} 48	75	HV_{OUT} 12
36	HV_{OUT} 47	76	HV_{OUT} 11
37	HV_{OUT} 46	77	HV_{OUT} 10
38	HV_{OUT} 45	78	HV_{OUT} 9
39	HV_{OUT} 44	79	HV_{OUT} 8
40	HV_{OUT} 43	80	HV_{OUT} 7

Package Outline



80-pin Gullwing Package

Supertex inc.

64-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Package Options	
	80-Lead Quad Plastic Gullwing	Die
HV31	HV3137PG	HV3137X

Features

- ☐ HVCMOS® technology
- ☐ Output voltages up to 375V
- ☐ Sink current minimum 1 mA
- ☐ Shift register speed 6 MHz
- ☐ Latched outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +9V
Supply voltage, V_{PP}	-0.5V to +375V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current	0.75A
Continuous total power dissipation[2]	1200mW
Operating temperature range	0°C to +85°C
Storage temperature range	-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. For operation above 25°C ambient derate linearly by 15mW/°C up to 85°C.

General Description

The HV31 is a low voltage serial to high voltage parallel converter with open drain outputs. It has been designed especially for use as a driver for electrostatic printers.

This device consists of a 64-bit shift register, 64 latches, latch enable (LE), and output enable (OE). Data is shifted through the shift register on the high to low transition of the clock. When the DIR pin is set high, the HV31 shifts in the counterclockwise direction when viewed from the top of the package. When the DIR pin is set low, the HV31 shifts in the clockwise direction. A serial data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE or the OE inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is stored when LE is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				15	mA	f_{CLK} = 6MHz, f_{DATA} = 3MHz
							$\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				250	µA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current at 25°C, per Switch				100	nA	Output high, and at 375V
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_I = 0V
V_{OH}	High-Level Data Out		V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			10	V	IHV_{OUT} = +1mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-3.0	V	I_{OL} = -1mA
C_{HVO}	Output Capacitance per Channel				3	pF	V_{DS} = 100V

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			6	MHz	
t_W	Clock Width High or Low	83			ns	
t_{SU}	Data Setup Time Before Clock Falls	35			ns	
t_H	Data Hold Time After Clock Falls	15			ns	
t_{WLE}	Width of Latch Enable Pulse	83			ns	
t_{DLE}	$\overline{LE}$ Delay Time After Falling Edge of Clock	35			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Falling Edge of Clock	40			ns	
t_{DHL}	Clock Delay Time Data High to Low			135	ns	
t_{DLH}	Clock Delay Time Data Low to High			135	ns	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.5	5	5.5	V
V_{PP}	High voltage supply	8.0		375	V
V_{IH}	High-level input voltage	3.5		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.8	V
T_A	Operating free-air temperature	0		+85	°C

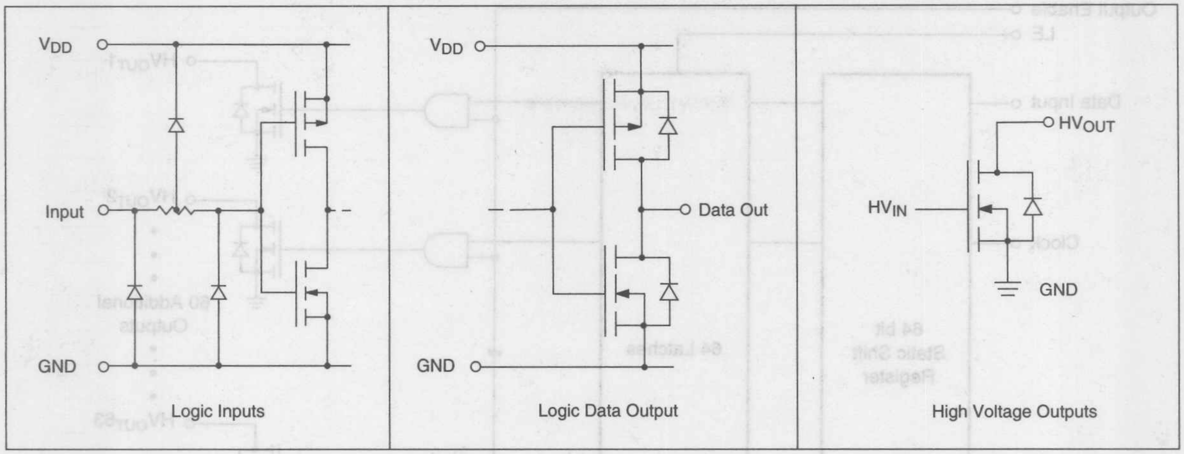
Note:

Power-up sequence should be the following:

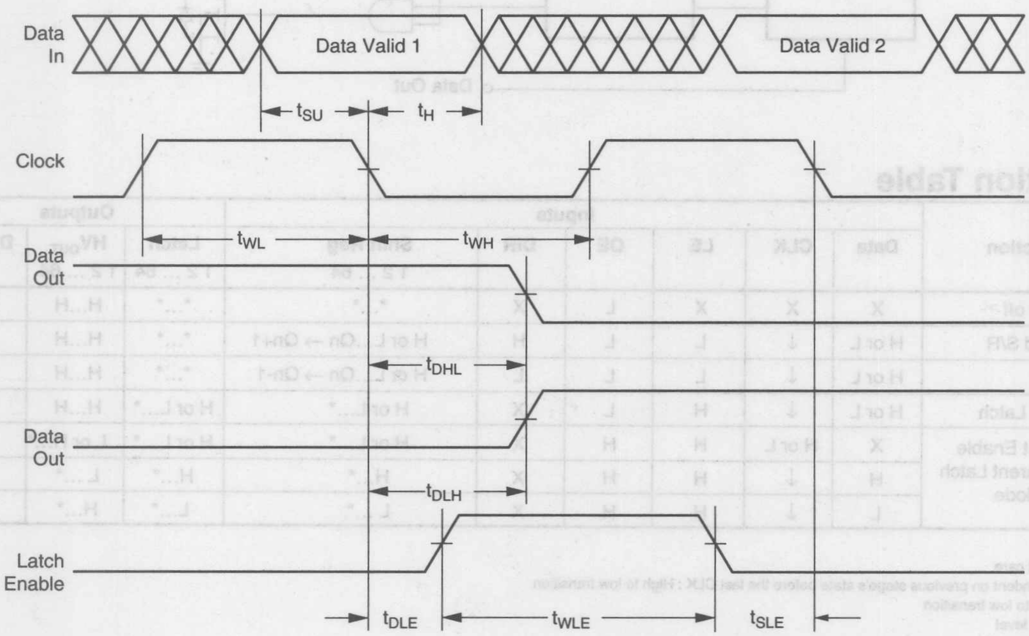
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

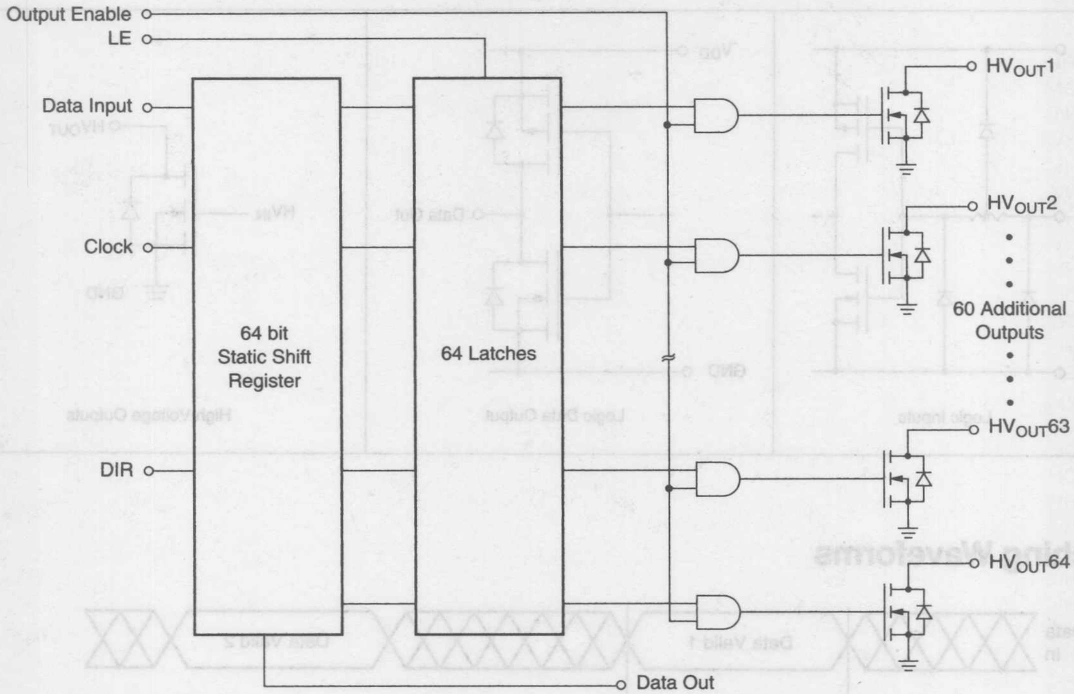
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs		
	Data	CLK	LE	OE	DIR	Shift Reg 1 2 … 64	Latch 1 2 … 64	HV_{OUT} 1 2 … 64	D_{OUT}
All off	X	X	X	L	X	*…*	*…*	H…H	*
Load S/R	H or L	↓	L	L	H	H or L…Qn → Qn+1	*…*	H…H	*
	H or L	↓	L	L	L	H or L…Qn → Qn-1	*…*	H…H	*
Load Latch	H or L	↓	H	L	X	H or L…*	H or L…*	H…H	*
Output Enable Transparent Latch Mode	X	H or L	H	H	X	H or L…*	H or L…*	L or H…*	*
	H	↓	H	H	X	H…*	H…*	L …*	*
	L	↓	H	H	X	L …*	L…*	H…*	*

Notes:
X = Don't care
* = Dependent on previous stage's state before the last CLK : High to low transition.
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

PG and DG Packages

HV31

Pin	Function	Pin	Function
1	GND	41	N/C
2	N/C	42	N/C
3	HV_{OUT} 59/6	43	HV_{OUT} 23/42
4	HV_{OUT} 60/5	44	HV_{OUT} 24/41
5	HV_{OUT} 61/4	45	HV_{OUT} 25/40
6	HV_{OUT} 62/3	46	HV_{OUT} 26/39
7	HV_{OUT} 63/2	47	HV_{OUT} 27/38
8	HV_{OUT} 64/1	48	HV_{OUT} 28/37
9	DIR	49	HV_{OUT} 29/36
10	Data Out	50	HV_{OUT} 30/35
11	CLK	51	HV_{OUT} 31/34
12	GND	52	HV_{OUT} 32/33
13	V_{DD}	53	HV_{OUT} 33/32
14	LE	54	HV_{OUT} 34/31
15	Data In	55	HV_{OUT} 35/30
16	OE	56	HV_{OUT} 36/29
17	HV_{OUT} 1/64	57	HV_{OUT} 37/28
18	HV_{OUT} 2/63	58	HV_{OUT} 38/27
19	HV_{OUT} 3/62	59	HV_{OUT} 39/26
20	HV_{OUT} 4/61	60	HV_{OUT} 40/25
21	HV_{OUT} 5/60	61	HV_{OUT} 41/24
22	HV_{OUT} 6/59	62	HV_{OUT} 42/23
23	N/C	63	N/C
24	HV_{OUT} GND	64	N/C
25	HV_{OUT} 7/58	65	HV_{OUT} 43/22
26	HV_{OUT} 8/57	66	HV_{OUT} 44/21
27	HV_{OUT} 9/56	67	HV_{OUT} 45/20
28	HV_{OUT} 10/55	68	HV_{OUT} 46/19
29	HV_{OUT} 11/54	69	HV_{OUT} 47/18
30	HV_{OUT} 12/53	70	HV_{OUT} 48/17
31	HV_{OUT} 13/52	71	HV_{OUT} 49/16
32	HV_{OUT} 14/51	72	HV_{OUT} 50/15
33	HV_{OUT} 15/50	73	HV_{OUT} 51/14
34	HV_{OUT} 16/49	74	HV_{OUT} 52/13
35	HV_{OUT} 17/48	75	HV_{OUT} 53/12
36	HV_{OUT} 18/47	76	HV_{OUT} 54/11
37	HV_{OUT} 19/46	77	HV_{OUT} 55/10
38	HV_{OUT} 20/45	78	HV_{OUT} 56/9
39	HV_{OUT} 21/44	79	HV_{OUT} 57/8
40	HV_{OUT} 22/43	80	HV_{OUT} 58/7

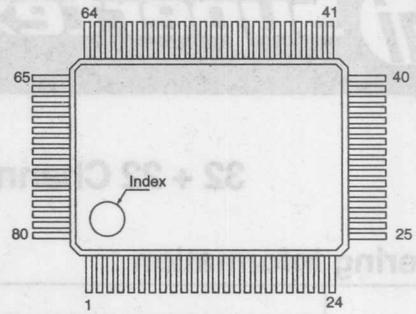
Note:

Pin designation DIR = H/L

Example: For DIR = H, Pin 3 is HV_{OUT} 59

For DIR = L, Pin 3 is HV_{OUT} 6

Package Outline



top view

80-pin Gullwing Package

Supertex inc.

HV33

Preliminary

32 + 22 Channel Matrix Printhead Driver

Ordering Information

Device	Package Options			
	68 J - Lead Ceramic Quad Flatpack	68 J - Lead Plastic Quad Flatpack	Die	68 J - Lead Ceramic Quad Flatpack (MIL-STD-883 Processed*)
HV33	HV3304DJ	HV3304PJ	HV3304X	RBHV3304DJ

* For Hi-Rel process flows, please refer to page 5-3 in the Databook

Features

- Separate data (32) and strobe (22) outputs
- Independant CLK and BLK functions
- 4MHz opertation (either clock)
- Latched data outputs
- 68-pin QFP
- Mil version available

Absolute Maximum Ratings

Supply voltage, V_{DD}		-0.5V to +7V
Supply voltage, V_{PD}		36V
Supply voltage, V_{PS}		36V
Logic input levels		-0.5V to V_{DD} + 0.5V
Continuous total power dissipation	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Ceramic	-40°C to +85°C
	Plastic	0°C to +70°C
Storage temperature range		-65°C to +150°C

General Description

The HV33 is dual serial-to-parallel converter chip originally designed for driving printheads. Its dual converters have independent clock inputs and output blanking logic permitting considerable flexibility in driving small matrix arrays with one device.

Electrical Characteristics (over recommended operating conditions unless noted)

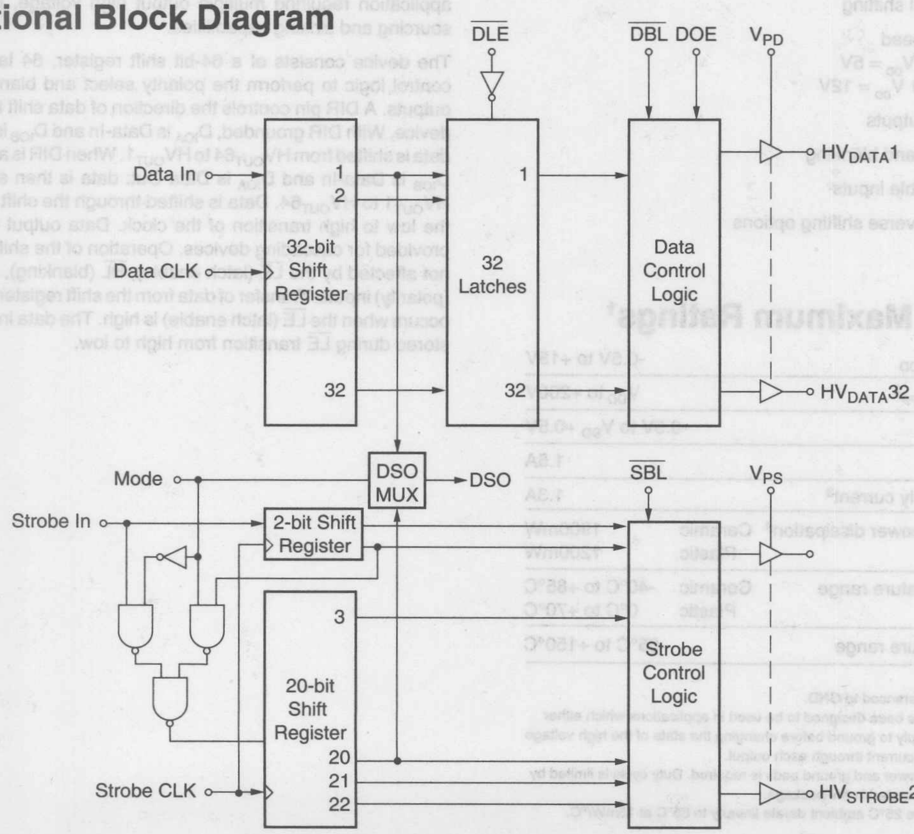
DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current			25	mA	f_{CLK} = 4MHz, f_{DATA} = 2MHz
I_{DDQ}	Quiescent V_{DD} Supply Current			0.25	mA	All V_{IN} = 0V
I_{PP}	High Voltage Supply Current			0.5	mA	Output High and Low
V_{OH}	High-Level Data Out			36	V	I_{OUT} = 4mA
I_{IH}	High-Level Input Current			10	µA	V_{IN} = High
I_{IL}	Low-Level Input Current	-10			µA	V_{IN} = 0V

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			4	MHz	
t_W	Clock Width High or Low	125			ns	
t_{SU}	Data Setup Time Before Clock Falls	50			ns	
t_H	Data Hold Time After Clock Falls	20			ns	
t_{DHVS}	Delay from -SBL to HV Strobe			2	µs	250 pF Load
t_{DHVD}	Delay from SCLK/DL to HV Date			2	µs	250 pF Load

Functional Block Diagram



Supertex inc.

HV34

64-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options			
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV34	180V	HV3418DG	HV3418PG	HV3418T	HV3418X

*For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- ☐ HVCMOS® technology
- ☐ Output voltages up to 180V
- ☐ Low power level shifting
- ☐ Shift register speed
  6MHz @ V_{DD} = 5V
  12MHz @ V_{DD} = 12V
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +15V
Supply voltage, V_{PP}[2]		V_{DD} to +200V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		1.5A
High voltage supply current[3]		1.3A
Continuous total power dissipation[4]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Ceramic	-40°C to +85°C
	Plastic	0°C to +70°C
Storage temperature range		-65°C to +150°C

Notes:

1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV34 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a printer driver for ink-jet applications. It can also be used in any application requiring multiple output high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, D_{IOA} is Data-In and D_{IOB} is Data-Out; data is shifted from $HV_{OUT}64$ to $HV_{OUT}1$. When DIR is at logic high, D_{IOB} is Data-In and D_{IOA} is Data-Out: data is then shifted from $HV_{OUT}1$ to $HV_{OUT}64$. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 12MHz, f_{DATA} = 12MHz, $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				200	µA	All V_{IN} = 0V or V_{DD}
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 180V All outputs high
					0.50	mA	V_{PP} = 180V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_{IL} = 0V
V_{OH}	High-Level Output	HV_{OUT}	155			V	V_{PP} = 180V, IHV_{OUT} = -5mA
		Data Out	V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			25	V	V_{PP} = 180V, IHV_{OUT} = +5mA
		Data Out			1.0	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} +1.5	V	I_{OL} = +5mA
					-1.5	V	I_{OL} = -5mA

AC Characteristics[1,2] (For V_{DD} = 12V: values in parentheses are for V_{DD} = 5V; V_{PP} = 180V, T_A = 25°C)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency				12(6)	MHz	
t_W	Clock Width High and Low	High	40(62)			ns	
		Low	35(42)			ns	
t_{SU}	Data Setup Time Before Clock Rises		25(35)			ns	
t_H	Data Hold Time After Clock Rises		10(30)			ns	
t_{WLE}	Width of Latch Enable Pulse		62(80)			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock		25(35)			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock		30(40)			ns	
t_{ON}, t_{OFF}	Time from Latch Enable to HV_{OUT}				1(1.5)	µs	C_L = 20pF
t_{DHL}	Delay Time Clock to Data High to Low				50(110)	ns	C_L = 20pF
t_{DLH}	Delay Time Clock to Data Low to High				75(160)	ns	C_L = 20pF
t_r, t_f	All Logic Inputs				5	ns	

Notes:
1. Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.
2. AC Characteristics are guaranteed only under V_{DD} = 12V and V_{DD} = 5V.

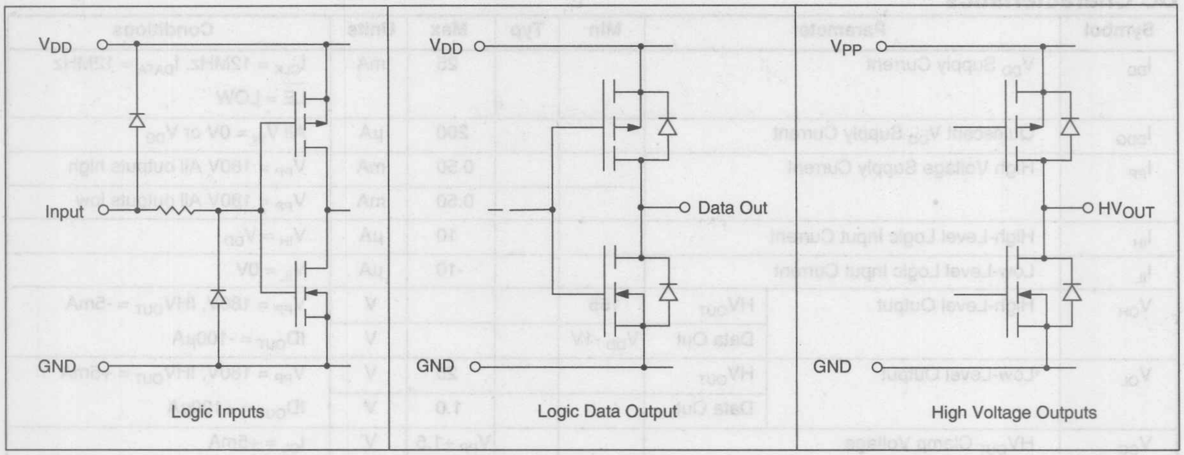
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage	V_{DD} = 5V	4.5	5.0	5.5	V
		V_{DD} =12V	10.8	12.0	13.2	V
V_{PP}	High voltage supply		60		180	V
V_{IH}	High-level input voltage		V_{DD} -0.9		V_{DD}	V
V_{IL}	Low-level input voltage		0		0.9	V
T_A	Operating free-air temperature		0		+70	°C

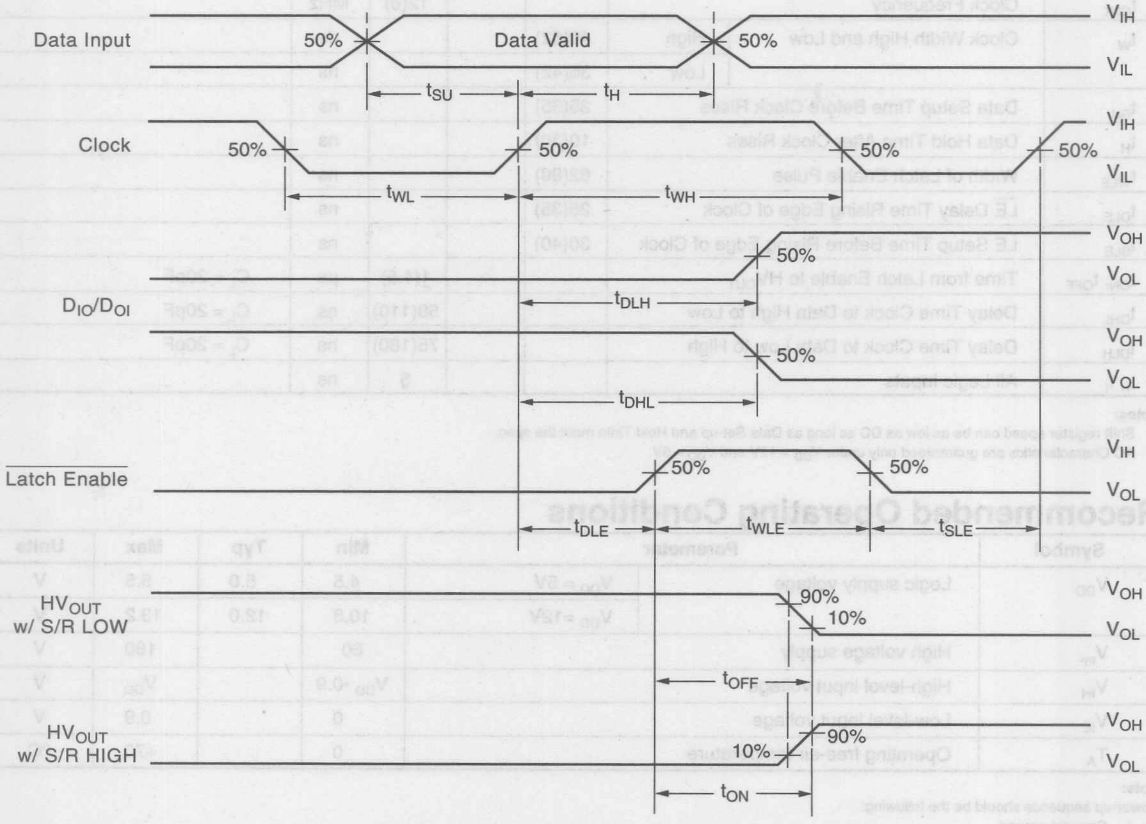
Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

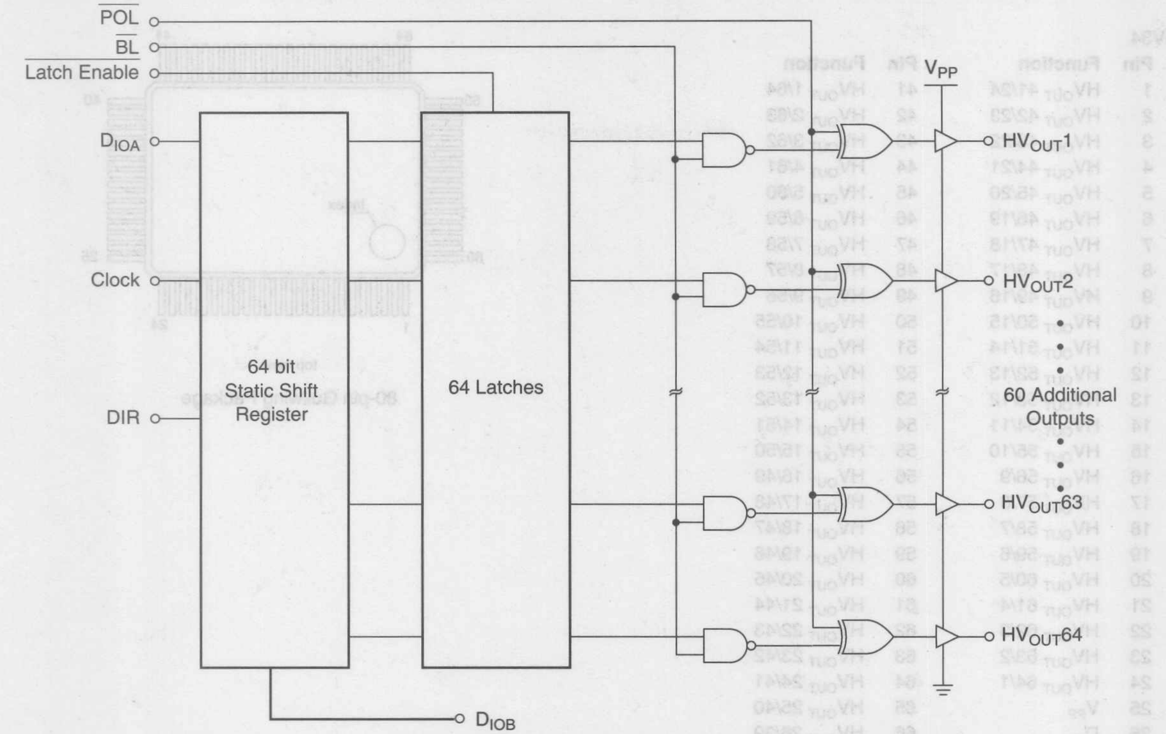
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1	Shift Reg 2…64	HV Outputs 1	HV Outputs 2…64	Data Out
All on	X	X	X	L	L	X	*	*…*	H	H…H	*
All off	X	X	X	L	H	X	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*…*	*	*…*	*
Load Latches	X	H or L	↓	H	H	X	*	*…*	*	*…*	*
	X	H or L	↓	H	L	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Transparent Latch mode	L	↑	H	H	H	X	L	*…*	L	*…*	*
	H	↑	H	H	H	X	H	*…*	H	*…*	*
I/O Relation	D_{IOA}	↑	X	X	X	L	$Q_n \rightarrow$	Q_{n-1}	—		D_{IOB}
	D_{IOB}	↑	X	X	X	H	$Q_n \rightarrow$	Q_{n+1}	—		D_{IOA}

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

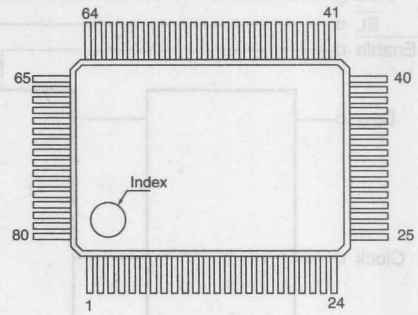
Pin Configurations

HV34

Pin	Function	Pin	Function
1	HV_{OUT} 41/24	41	HV_{OUT} 1/64
2	HV_{OUT} 42/23	42	HV_{OUT} 2/63
3	HV_{OUT} 43/22	43	HV_{OUT} 3/62
4	HV_{OUT} 44/21	44	HV_{OUT} 4/61
5	HV_{OUT} 45/20	45	HV_{OUT} 5/60
6	HV_{OUT} 46/19	46	HV_{OUT} 6/59
7	HV_{OUT} 47/18	47	HV_{OUT} 7/58
8	HV_{OUT} 48/17	48	HV_{OUT} 8/57
9	HV_{OUT} 49/16	49	HV_{OUT} 9/56
10	HV_{OUT} 50/15	50	HV_{OUT} 10/55
11	HV_{OUT} 51/14	51	HV_{OUT} 11/54
12	HV_{OUT} 52/13	52	HV_{OUT} 12/53
13	HV_{OUT} 53/12	53	HV_{OUT} 13/52
14	HV_{OUT} 54/11	54	HV_{OUT} 14/51
15	HV_{OUT} 55/10	55	HV_{OUT} 15/50
16	HV_{OUT} 56/9	56	HV_{OUT} 16/49
17	HV_{OUT} 57/8	57	HV_{OUT} 17/48
18	HV_{OUT} 58/7	58	HV_{OUT} 18/47
19	HV_{OUT} 59/6	59	HV_{OUT} 19/46
20	HV_{OUT} 60/5	60	HV_{OUT} 20/45
21	HV_{OUT} 61/4	61	HV_{OUT} 21/44
22	HV_{OUT} 62/3	62	HV_{OUT} 22/43
23	HV_{OUT} 63/2	63	HV_{OUT} 23/42
24	HV_{OUT} 64/1	64	HV_{OUT} 24/41
25	V_{PP}	65	HV_{OUT} 25/40
26	D_{IOA}	66	HV_{OUT} 26/39
27	N/C	67	HV_{OUT} 27/38
28	N/C	68	HV_{OUT} 28/37
29	$\overline{BL}$	69	HV_{OUT} 29/36
30	$\overline{POL}$	70	HV_{OUT} 30/35
31	V_{DD}	71	HV_{OUT} 31/34
32	DIR	72	HV_{OUT} 32/33
33	LGND	73	HV_{OUT} 33/32
34	OGND	74	HV_{OUT} 34/31
35	N/C	75	HV_{OUT} 35/30
36	N/C	76	HV_{OUT} 36/29
37	CLK	77	HV_{OUT} 37/28
38	$\overline{LE}$	78	HV_{OUT} 38/27
39	D_{IOB}	79	HV_{OUT} 39/26
40	V_{PP}	80	HV_{OUT} 40/25

Note:
Pin designation for DIR = H/L
Example: for DIR = H, Pin 1 is HV_{OUT}41
for DIR = L, Pin 1 is HV_{OUT}24

Package Outline



top view

80-pin Gullwing Package

Supertex inc.

HV35

Objective

275V, 64-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options			
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die
HV35	275V	HV3527DG	HV3527PG	HV3527T	HV3527X

*For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- ☐ HVCMOS® technology
- ☐ Output voltages up to 275V
- ☐ Low power level shifting
- ☐ Shift register speed 6MHz @ V_{DD} = 5V
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +6V
Supply voltage, V_{PP}[2]		V_{DD} to 300V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		1.5A
High voltage supply current[3]		1.3A
Continuous total power dissipation[4]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Ceramic	-40°C to +85°C
	Plastic	0°C to +70°C
Storage temperature range		-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV35 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a printer driver for electrostatic applications. It can also be used in any application requiring multiple output high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, D_{IOA} is Data-In and D_{IOB} is Data-Out; data is shifted from HV_{OUT}64 to HV_{OUT}1. When DIR is at logic high, D_{IOB} is Data-In and D_{IOA} is Data-Out: data is then shifted from HV_{OUT}1 to HV_{OUT}64. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

A bias pin is used to ensure that the device operates at full V_{PP} voltage.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 6MHz, f_{DATA} = 3MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				200	µA	All V_{IN} = 0V or V_{DD}
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 275V All outputs high
					0.50	mA	V_{PP} = 275V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	V_{IH} = V_{DD}
I_{IL}	Low-Level Logic Input Current				-10	µA	V_{IL} = 0V
V_{OH}	High-Level Output	HV_{OUT}	200			V	V_{PP} = 275V, IHV_{OUT} = -1mA
		Data Out	V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			10	V	IHV_{OUT} = 1mA, V_{DD} = 5V
		Data Out			1.0	V	ID_{OUT} = 100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} +1.5	V	I_{OL} = +5mA
					-1.5	V	I_{OL} = -5mA

AC Characteristics[1,2] (For V_{DD} = 5V; V_{PP} = 275V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			6	MHz	
t_W	Clock Width High and Low — High	62			ns	
	Low	42			ns	
t_{SU}	Data Setup Time Before Clock Rises	35			ns	
t_H	Data Hold Time After Clock Rises	30			ns	
t_{WLE}	Width of Latch Enable Pulse	80			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	35			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	40			ns	
t_{ON}, t_{OFF}	Time from Latch Enable to HV_{OUT}			1.5	µs	C_L = 20pF
t_{DHL}	Delay Time Clock to Data High to Low			80	ns	C_L = 20pF
t_{DLH}	Delay Time Clock to Data Low to High			80	ns	C_L = 20pF
t_r, t_f	All Logic Inputs			5	ns	

Notes:
1. Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.
2. AC Characteristics are guaranteed only under V_{DD} = 5V.

Recommended Operating Conditions

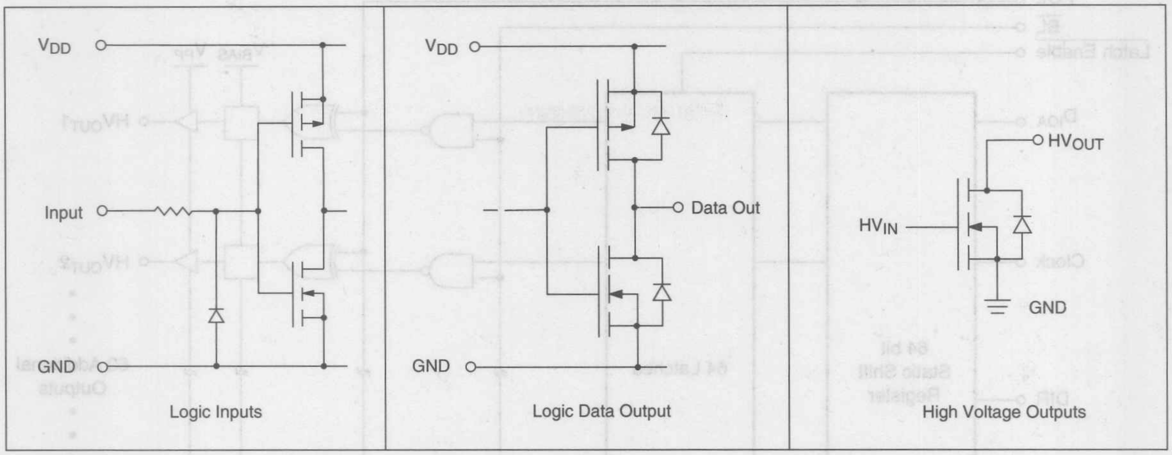
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V
V_{PP}	High voltage supply	60		275	V
V_{IH}	High-level input voltage	V_{DD} -0.9		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.9	V
T_A	Operating free-air temperature	0		+70	°C

Notes:

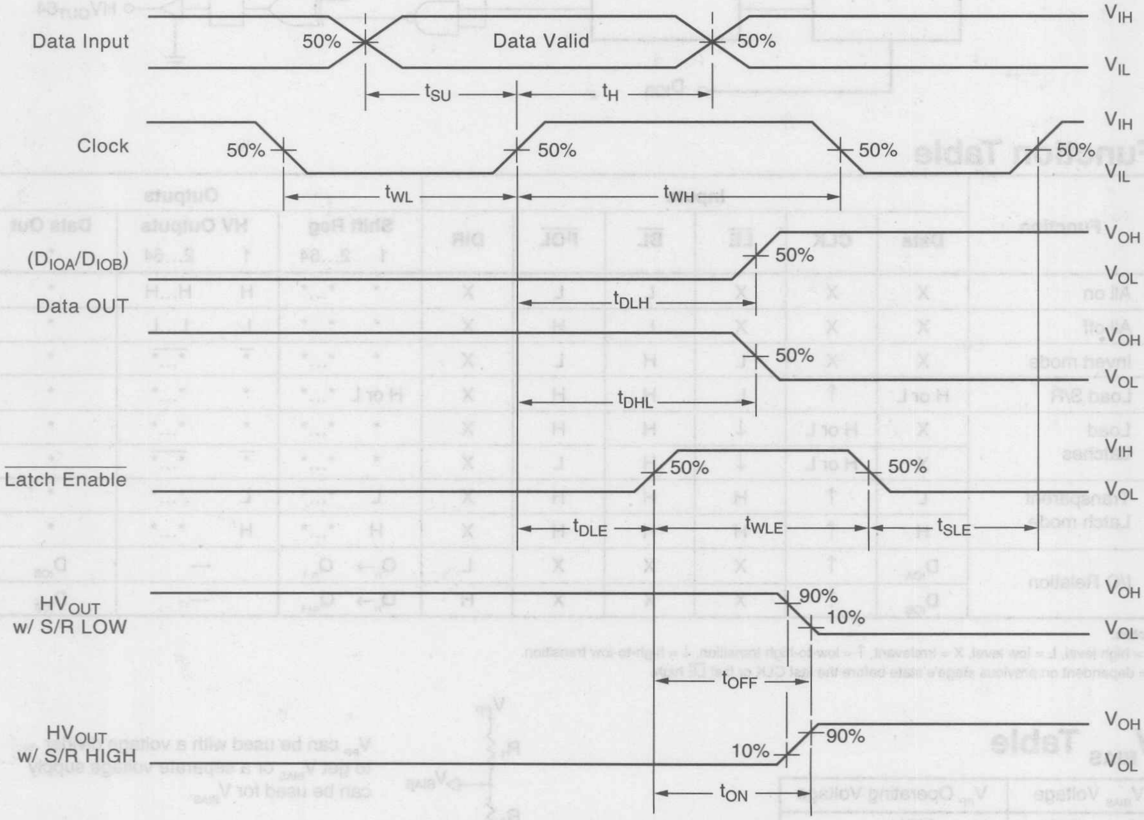
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

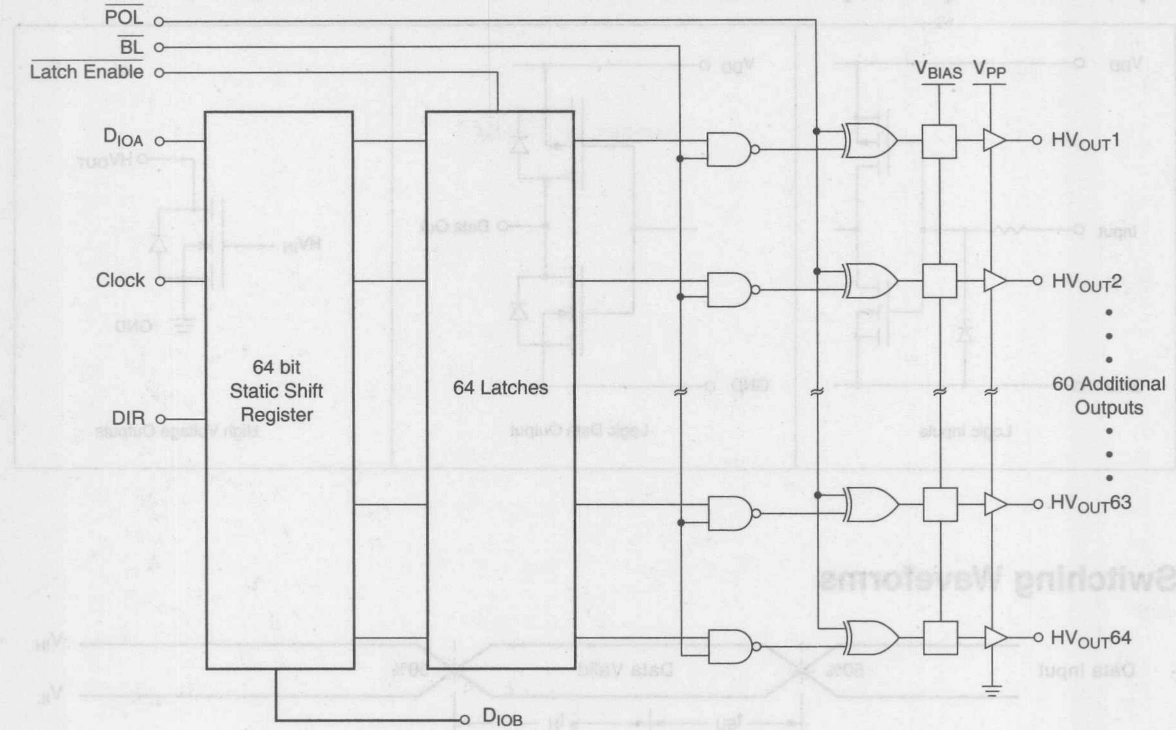
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



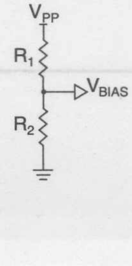
Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1	Shift Reg 2…64	HV Outputs 1	HV Outputs 2…64	Data Out *
All on	X	X	X	L	L	X	*	*…*	H	H…H	*
All off	X	X	X	L	H	X	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	X	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*…*	*	*…*	*
Load Latches	X	H or L	↓	H	H	X	*	*…*	*	*…*	*
	X	H or L	↓	H	L	X	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Transparent Latch mode	L	↑	H	H	H	X	L	*…*	L	*…*	*
	H	↑	H	H	H	X	H	*…*	H	*…*	*
I/O Relation	D_{IOA}	↑	X	X	X	L	$Q_n \rightarrow$	Q_{n-1}	—		D_{IOB}
	D_{IOB}	↑	X	X	X	H	$Q_n \rightarrow$	Q_{n+1}	—		D_{IOA}

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

V_{BIAS} Table

V_{BIAS} Voltage	V_{PP} Operating Voltage
$V_{BIAS} = 0V/V_{PP}$	$V_{PP} = 200V$
$V_{BIAS} = 80\pm5V$	$V_{PP} = 275V$



V_{PP} can be used with a voltage divider to get V_{BIAS} or a separate voltage supply can be used for V_{BIAS}.

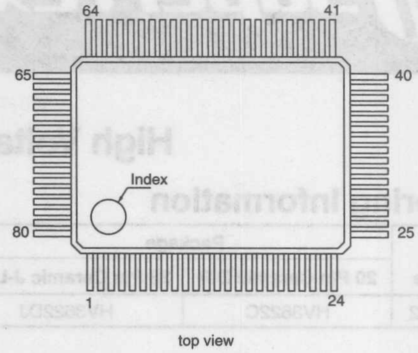
Pin Configurations

HV35

Pin	Function	Pin	Function
1	HV_{OUT} 41/24	41	HV_{OUT} 1/64
2	HV_{OUT} 42/23	42	HV_{OUT} 2/63
3	HV_{OUT} 43/22	43	HV_{OUT} 3/62
4	HV_{OUT} 44/21	44	HV_{OUT} 4/61
5	HV_{OUT} 45/20	45	HV_{OUT} 5/60
6	HV_{OUT} 46/19	46	HV_{OUT} 6/59
7	HV_{OUT} 47/18	47	HV_{OUT} 7/58
8	HV_{OUT} 48/17	48	HV_{OUT} 8/57
9	HV_{OUT} 49/16	49	HV_{OUT} 9/56
10	HV_{OUT} 50/15	50	HV_{OUT} 10/55
11	HV_{OUT} 51/14	51	HV_{OUT} 11/54
12	HV_{OUT} 52/13	52	HV_{OUT} 12/53
13	HV_{OUT} 53/12	53	HV_{OUT} 13/52
14	HV_{OUT} 54/11	54	HV_{OUT} 14/51
15	HV_{OUT} 55/10	55	HV_{OUT} 15/50
16	HV_{OUT} 56/9	56	HV_{OUT} 16/49
17	HV_{OUT} 57/8	57	HV_{OUT} 17/48
18	HV_{OUT} 58/7	58	HV_{OUT} 18/47
19	HV_{OUT} 59/6	59	HV_{OUT} 19/46
20	HV_{OUT} 60/5	60	HV_{OUT} 20/45
21	HV_{OUT} 61/4	61	HV_{OUT} 21/44
22	HV_{OUT} 62/3	62	HV_{OUT} 22/43
23	HV_{OUT} 63/2	63	HV_{OUT} 23/42
24	HV_{OUT} 64/1	64	HV_{OUT} 24/41
25	V_{PP}	65	HV_{OUT} 25/40
26	D_{IOA}	66	HV_{OUT} 26/39
27	N/C	67	HV_{OUT} 27/38
28	N/C	68	HV_{OUT} 28/37
29	$\overline{BL}$	69	HV_{OUT} 29/36
30	$\overline{POL}$	70	HV_{OUT} 30/35
31	V_{DD}	71	HV_{OUT} 31/34
32	DIR	72	HV_{OUT} 32/33
33	V_{BIAS}	73	HV_{OUT} 33/32
34	GND	74	HV_{OUT} 34/31
35	N/C	75	HV_{OUT} 35/30
36	N/C	76	HV_{OUT} 36/29
37	$\overline{CLK}$	77	HV_{OUT} 37/28
38	$\overline{LE}$	78	HV_{OUT} 38/27
39	D_{IOB}	79	HV_{OUT} 39/26
40	V_{PP}	80	HV_{OUT} 40/25

Note:
Pin designation for DIR = H/L
Example: for DIR = H, Pin 1 is HV_{OUT}41
for DIR = L, Pin 1 is HV_{OUT}24

Package Outline



80-pin Gullwing Package

High Voltage PIN Diode Driver

Ordering Information

Device	Package	
	20 Pin Ceramic DIP	28 Pin Ceramic J-Lead
HV3622	HV3622C	HV3622DJ

Features

- Processed with HVCMOS® technology
- 5V CMOS logic – low power dissipation
- DMOS output voltage up to 220V
- Low power level shifting – 5V to 220V
- Source current 10mA
- Output fault detection
- Latched data output

Absolute Maximum Ratings

Supply Voltage, V_{CC}	-0.5V to +7.0V
Logic Input Voltage	-0.3V to VCC + 0.3V
Supply Voltage V_{LL}	-5.0V
Supply Voltage V_{PP}	+230V
Max Power Dissipation	0.8W
Junction Temperature	+150 °C
Storage Temperature Range	-65 °C to +150 °C
Operating Temperature Range	-55 °C to +125 °C
Lead Soldering Temperature for 10 Seconds	+300 °C

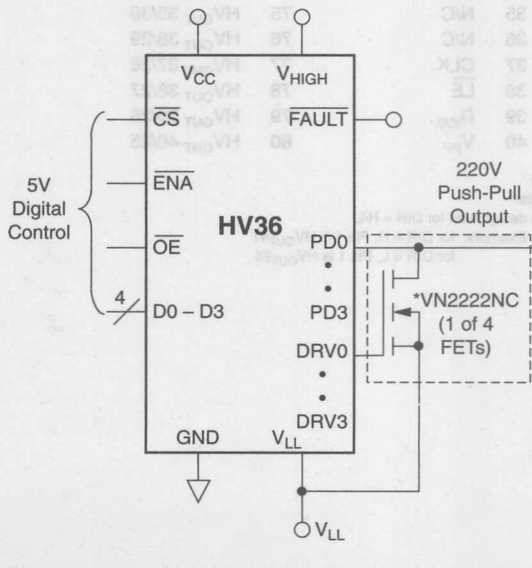
General Description

The HV3622 is a monolithic high-voltage quad-output driver that is designed to be used in conjunction with the Supertex VN2222NC,* a separate N-channel DMOS FET quad array, whose device characterics are briefly described below. Together, these devices perform a 220V push-pull function that is especially suited for driving PIN diodes in applications such as frequency-hopping radios, microwave communication systems and phased array radar.

Used as a microwave or RF switch, the HV3622 has 4 high-voltage P-channel outputs: PD_0, PD_1, PD_2 and PD_3. Additional controls are Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) functions. The HV3622 also has an output fault detection function that protects the outputs from damage by putting them into a high impedance state when a short is detected. The HV3622 provides 4 low-voltage outputs—DRV_0, DRV_1, DRV_2 and DRV_3—that drive the gates of the 4 N-channel FETs in the VN2222NC device. See the diagram below for an example of the push-pull output structure that these two devices provide.

For detailed electrical characteristics of the VN2222NC, please see the VN22C data sheet in Chapter 8. Currently, the HV3622 is only available in through-hole and surface-mount ceramic packages that are suitable for military applications, while the VN22C is offered in both ceramic quad and discrete packages. For commercial product availability, please consult the factory.

Push-Pull Configuration



* VN2222NC is an N-channel DMOS FET quad array recommended for use in conjunction with HV36 outputs to form four 220V push-pull outputs. Each of the four devices has a max $R_{DS(ON)}$ of 1.25Ω, min $I_{D(ON)}$ of 5.0 amps, and BV_{DSS} of 220V.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{CCQ}	Maximum Quiescent V_{CC} Supply Current		1.0	mA	V_{CC} = 5.5V All ouputs open
I_{LLQ}	Maximum Quiescent V_{LL} Supply Current		4.0	mA	V_{LL}= -3.5V $D_{RV(N)}$ high or low
I_{PPQ}	Maximum Quiescent V_{PP} Supply Current		100	µA	V_{PP} = 220V $P_{D(N)}$ high or low
I_{IH}	High-level logic current		10	µA	H = V_{CC}
I_{IL}	Low-level logic current		10	µA	L = 0V
V_{FH}	Minimum high-level logic output voltage (fault detect)	4.4		V	V_{CC} = 4.5V, I_{OH} = 20µA
V_{FL}	Maximum low-level logic output voltage (fault detect)		0.1	V	V_{CC} = 5.5V, I_{OL} =-20µA
V_{DH}	Minimum $P_{D(N)}$ high-level output voltage	198		V	V_{PP} = 203V, I_{OH}=10mA
V_{DH}	Minimum $P_{D(N)}$ high-level output voltage	92.5		V	V_{PP} = 100V, V_{DH} =10mA
V_{DH}	Minimum $D_{RV(N)}$ high-level output voltage	4		V	V_{CC} = 4.5V, I_{DH}=100µA
V_{DL}	Maximum $D_{RV(N)}$ low-output voltage		-2.3	V	V_{LL} = -2.5V, I_{DL} = -500µA
$V_{TH(min)}$	Minimum fault threshold for $P_{D(N)}$ output high	0.5 x V_{PP} fault		V	$P_{D(N)}$ = HIGH, $\overline{OE}$ = V_{CC}
$V_{TH(max)}$	Maximum fault threshold for $P_{D(N)}$ output high	0.85 x V_{PP} fault		V	$P_{D(N)}$ = HIGH, OE = V_{CC}
$V_{TL(min)}$	Minimum fault threshold for $P_{D(N)}$ output Hi-Z	$V_{(PDN)}$ = 0V		V	$P_{D(N)}$ = Hi-Z, $\overline{OE}$ = V_{CC}
$V_{TL(max)}$	Maximum fault thresholdfor $P_{D(N)}$ output Hi-Z		$V_{(PDN)}$ = 25	V	$P_{D(N)}$ = Hi-Z, $\overline{OE}$ = V_{CC}

AC Characteristics (over recommended operating conditions unless noted)

Symbol	Parameter	Min	Max	Units	Conditions
t_{WCS}	Minimum $\overline{CS}$ pulse to latch data	100		nSEC	V_{CC}= 4.5V, $\overline{ENA}$ = 0V
t_{WENA}	Minimum $\overline{ENA}$ pulse width to latch data	100		nSEC	V_{CC}= 4.5V, $\overline{CS}$ = 0V
t_{WOE}	$\overline{OE}$ pulse width	10	50	µS	V_{CC}= 4.5V, $\overline{OE}$ = 0V, V_{PP} = 220V $P_{D(N)}$ LOAD = 20K to GND
		16	50	µS	V_{PP} = 220V, $P_{D(N)}$ LOAD = 20K and 1500pF to GND
		40	50	µS	V_{PP} = 100V, $P_{D(N)}$ LOAD = 20K and 1500pF to GND
TT	Input transition rise and fall times	0	200	nSEC	V_{CC}= 4.5V
T_{SU1}	Minimum set-up time D_N and $\overline{CS}$ to $\overline{ENA}$	150		nSEC	V_{CC}= 4.5V
T_{SU2}	Minimum set-up time $\overline{ENA}$ to $\overline{OE}$ falling edge	150		nSEC	V_{CC}= 4.5V
TH	Minimum hold time	5		nSEC	V_{CC}= 4.5V
CIN	Maximum input capacitance		10	pF	Not tested, reference only
TO	$P_{D(N)}$ transition time from $\overline{OE}$ low to $P_{D(N)}$ high/low	1	15	µS	V_{PP} = 220V $P_{D(N)}$ output loaded by 20K ohms & 1500pF to GND
			40	µS	V_{PP} = 100V, $P_{D(N)}$ output loaded by 20K ohms & 1500pF to GND

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Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Logic Supply Voltage	4.5	5.5	V
V_{IN}	DC Logic Input Voltage	0	V_{CC}	V
V_{LL}	V_{LL} Supply Voltage	-3.5	-2.5	V
V_{PP}	V_{PP} Supply Voltage	100	220	V
$IP_{D(N)}H$	High-State Continuous $P_{D(N)}$ Source Current		10	mA
T_A	Ambient Operating Temp	-55	+125	°C
CL	$D_{RV(N)}$ Load Capacitance	0	0.006	µF

Notes:

1. V_{PP} rise time (dv/dt) should be less than 50V/µS.
2. Power-up sequence should be the following:
   - A) Connect ground;
   - B) Apply V_{PP};
   - C) Apply V_{DD};
   - D) Apply V_{LL};
   - E) Set all inputs to a known state. Power-down sequence should be the reverse of the above.

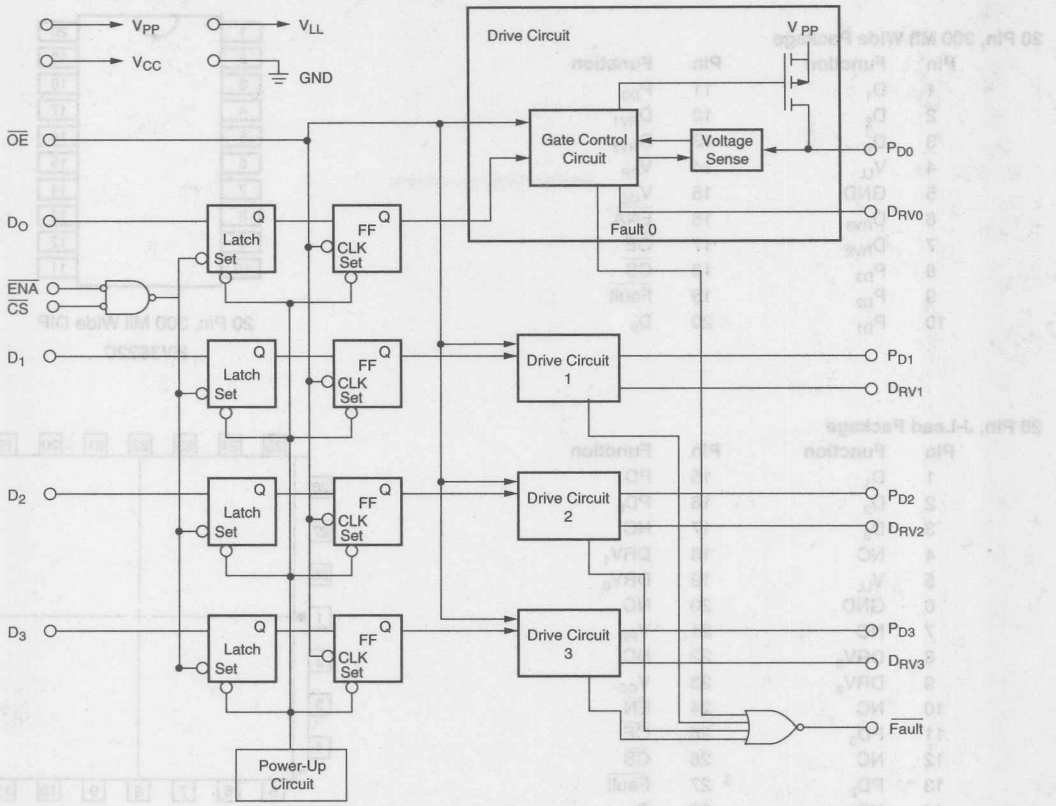
Function Table

Input					Output			
$\overline{CS}$	$\overline{ENA}$	$\overline{OE}$	Data $D_{(N)}$	V_{TH} Level[2]	Internal Latch Q(N)	$P_{D(N)}$	$D_{RV(N)}$	$\overline{\text{Fault}}$
H	X	H	X	Pass	Previous State	Previous State	Previous State	VFH
X	H	H	X	Pass	Previous State	Previous State	Previous State	VFH
L	L	H	H	Pass	Set	Previous State	Previous State	VFH
L	L	H	L	Pass	Reset	Previous State	Previous State	VFH
L	L	H>L	H	P/F	Set	VDH	VDL	VFH
L	L	H>L	L	P/F	Reset	HI-Z	VDH	VFH
H	X	H>L	X		Previous State			
				P/F	Set	VDH	VDL	VFH
				P/F	Reset	HI-Z	VDH	VFH
X	H	H>L	X		Previous State			
				Pass	Set	VDH	VDL	VFH
				Pass	Reset	HI-Z	VDH	VFH
X	X	H	X	Fail	—	HI-Z	VDL	VFL
(At Power Up)								
X	X	X	X	P/F	Set	VDH	VDL	VFH

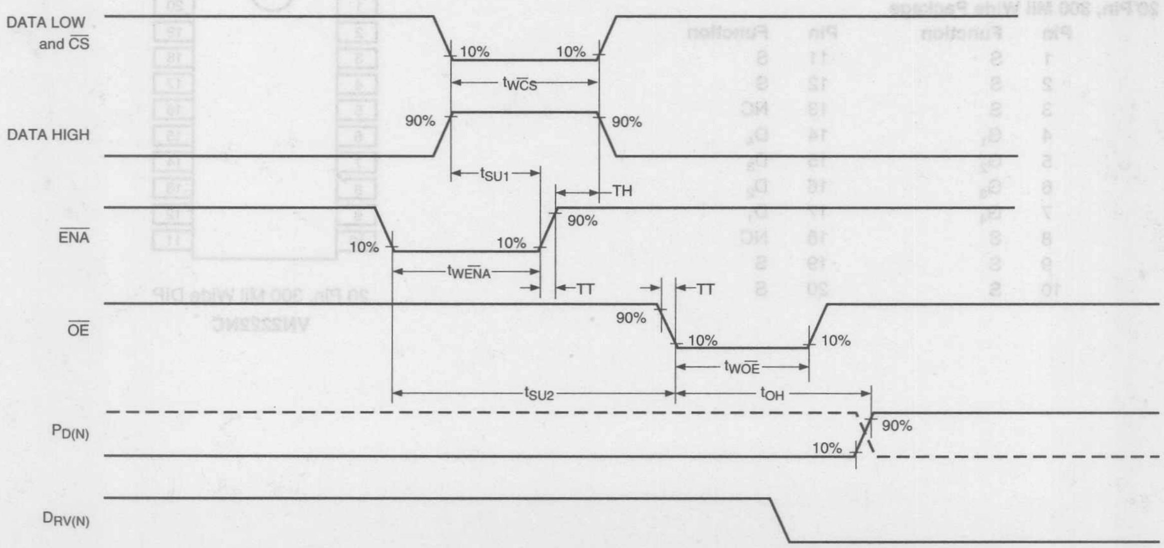
Notes:

1. X indicates "Don't Care" input state (L or H).
2. The output threshold is internally tested for each $P_{D(N)}$ output; the pass condition occurs when $\overline{OE}$ = H and:
   A) $P_{D(N)}$ driving high with output > $V_{TH\,(MAX)}$, or may occurs if $P_{D(N)}$ driving high and output > $V_{TH\,(MIN)}$ and < $V_{TL\,(MAX)}$.
   OR
   B) $P_{D(N)}$ driving Low with output < $V_{TH\,(MIN)}$, or may occur if $P_{D(N)}$ driving low and output < $V_{TH\,(MAX)}$ and < $V_{TL\,(MIN)}$.
   The fail condition occurs when $\overline{OE}$ = H and conditions for "pass" are not satisfied.
3. Fault output = V_{FL} indicates a fault has been detected in at least one of the $P_{D(N)}$ output loads when $\overline{OE}$ = H. All other outputs shall function normally when a fault condition has been detected for one of the outputs. The $\overline{\text{Fault}}$ output shall remain in the low state, regardless of the state of the output which initiated the fault status, until the next falling edge of $\overline{OE}$. Whenever $\overline{OE}$ = L, the $\overline{\text{Fault}}$ output is forced to V_{FH}, and the fault latch is reset. If the fault condition persists, the fault response repeats each time the $\overline{OE}$ input is set to H.
4. H>L indicates falling edge (H to L).
5. HI-Z indicates no current is sourced to output $P_{D(N)}$.
6. P/F indicates "Pass" or "Fail" fault threshold conditions.

Functional Block Diagram



Timing Diagram



Pin Configurations

20 Pin, 300 Mil Wide Package

Pin	Function	Pin	Function
1	D_1	11	P_{D0}
2	D_2	12	D_{RV1}
3	D_3	13	D_{RV2}
4	V_{LL}	14	V_{PP}
5	GND	15	V_{CC}
6	D_{RV3}	16	$\overline{ENA}$
7	D_{RV2}	17	$\overline{OE}$
8	P_{D3}	18	$\overline{CS}$
9	P_{D2}	19	$\overline{Fault}$
10	P_{D1}	20	D_0

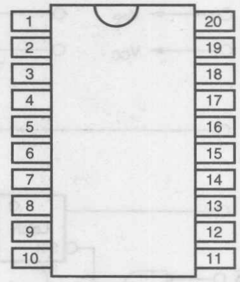
28 Pin, J-Lead Package

Pin	Function	Pin	Function
1	D_1	15	PD_1
2	D_2	16	PD_0
3	D_3	17	NC
4	NC	18	DRV_1
5	V_{LL}	19	DRV_0
6	GND	20	NC
7	NC	21	V_{PP}
8	DRV_3	22	NC
9	DRV_2	23	V_{CC}
10	NC	24	$\overline{EN}$
11	PD_3	25	$\overline{OE}$
12	NC	26	$\overline{CS}$
13	PD_2	27	$\overline{Fault}$
14	NC	28	D_0

20 Pin, 300 Mil Wide Package

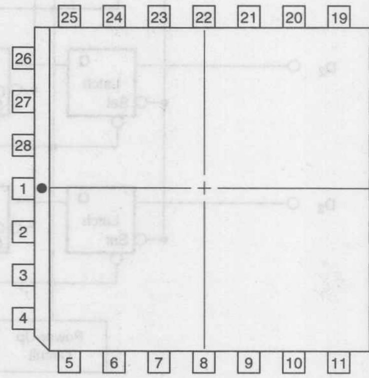
Pin	Function	Pin	Function
1	S	11	S
2	S	12	S
3	S	13	NC
4	G_1	14	D_4
5	G_2	15	D_3
6	G_3	16	D_2
7	G_4	17	D_1
8	S	18	NC
9	S	19	S
10	S	20	S

Package Outline



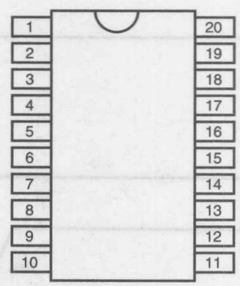
20 Pin, 300 Mil Wide DIP

HV3622C



28-pin J-Lead Package

HV3622DJ



20 Pin, 300 Mil Wide DIP

VN2222NC

Supertex inc.

Preliminary

32-Channel Gray-Shade Display Column Driver

Ordering Information

Device	Package Options			
	64-Lead 3-sided Plastic Gullwing	80-Lead Ceramic Gullwing	Die	80-Lead Ceramic Gullwing (MIL-STD-883 Processed*)
HV38	HV3806PG	HV3806DG	HV3806X	RBHV3806DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ 5V CMOS inputs
- ☐ Up to 60V modulation voltage
- ☐ Capable of 16 levels of gray shading
- ☐ 16MHz data throughput rate
- ☐ 32 Outputs per device (can be cascaded)
- ☐ Minimum 15 mA high-voltage output source/sink capability
- ☐ Pin-programmable shift direction (DIR)
- ☐ D/A conversion can be performed in as little as 3.2µs
- ☐ Diodes in output structure allow usage in energy recovery systems
- ☐ Integrated high-voltage CMOS technology
- ☐ Available in 3-sided 64-lead gullwing package or as dice

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7.5V
Supply voltage, V_{PP1}/V_{PP2}		-0.5V to +60V
Logic input levels[1]		-0.5 to V_{DD} + 0.5V
Ground current[2]		1.5A
Continuous total power dissipation[3]	Plastic	1200mW
	Ceramic	1500mW
Operating temperature range		-40°C to +85°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:

1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV38 is a 32-channel column driver IC designed for gray-shade display use. A bidirectional shift register working on both clock edges is used to index input data, in groups of 4, into a set of data latches. These are compared to the contents of a master binary counter. Each time the master counter begins to increment, a hold capacitor (C_H) on each channel is charged until the contents of the data latches is matched by that in the counter. Each channel's C_H thus is charged to an individual level, V_H, which is then transferred to the output by a source-follower structure that allows both sourcing and sinking of output current.

DIR is a shift-direction-select pin which has been provided to allow the user to interchange the shift register data input. When the DIR input is high, data is shifted in thru D1 to D4 in ascending order from $HV_{OUT}1$ to $HV_{OUT}32$. When the DIR input is low, data is shifted in descending order from $HV_{OUT}32$ to $HV_{OUT}1$.

In the HV38, the ramp generator circuitry (V_R) obtains its (low-current) bias from V_{PP1}. This allows the output bias, V_{PP2}, to be ramped down to zero when output current is not required, thus saving energy.

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Electrical Characteristics (at 25°C, unless otherwise specified)

Low-Voltage DC Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Units	Conditions
V_{DD}	Low-voltage supply	4.5	5.0	5.5	V	$f_{SC} = 8MHz$
I_{DD}	V_{DD} supply current (active)		6.0	10.0	mA	$f_{CC} = 6MHz$ $F_{DATA} = 8MHz$
I_{DDS}	V_{DD} supply current (standby)			100	µA	All $V_{IN} = 0V$, $V_{DD} = min$
V_{IH}	High-level input voltage	V_{DD} -1		V_{DD}	V	
V_{IL}	Low-level input voltage	0		1	V	
I_{IH}	High-level input current		1.0	50	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level input current		-1.0	-50	µA	$V_{IL} = 0V$
C_{IN}	Input capacitance (data, LC, SC, CC)			10	pF	$V_{IN} = 0V$, f = 1MHz
T_A	Operating free-air temperature	-40		85	°C	
V_{OH}	High-level output voltage	V_{DD} -1			V	$I_{OH} = -4mA$, $V_{DD} = min$
V_{OL}	Low-level output voltage			0.4	V	$I_{OL} = 4mA$, $V_{DD} = min$
I_{OH}	High-level output current			-4.0	mA	
I_{OL}	Low-level output current			4.0	mA	

Note 1. All typical values are at $V_{DD} = 5.0V$.

High-Voltage DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High-voltage supply	-0.3		60	V	
I_{PP}	V_{PP} supply current			100	µA	$V_{PP} = 60V$, outputs high or low, no load
V_R	Ramp voltage	0		V_{PP}-2	V	
I_{AOH} max	Maximum high-voltage analog output source current[1]			-15	mA	$V_{PP} = 60V$
I_{AOH}	High-voltage analog output source current[1]	-10			mA	$V_{PP} = 60V$ $V_R = 30V$, $V_{AO} = 25V$
		-100			µA	$V_{AO} = 28.75V$
I_{AOL} max	Maximum high-voltage analog output sink current[2]			15	mA	$V_{PP} = 60V$
I_{AOL}	High-voltage analog output sink current[2]	10			mA	$V_{PP} = 60V$ $V_R = 30V$, $V_{AO} = 25V$
		100			µA	$V_{AO} = 31.25V$

Notes:

1. Either by N-CH transistor or P-CH output diode.
2. Either by P-CH transistor or N-CH output diode.
3. Power-up sequence should be the following:
   1. Connect ground.
   2. Apply V_{DD}.
   3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
   4. Apply V_{PP}.

   Power-down sequence should be the reverse of the above.

Electrical Characteristics

AC Characteristics (V_{DD} = 5V, T_A = 25°C)

Logic Timing

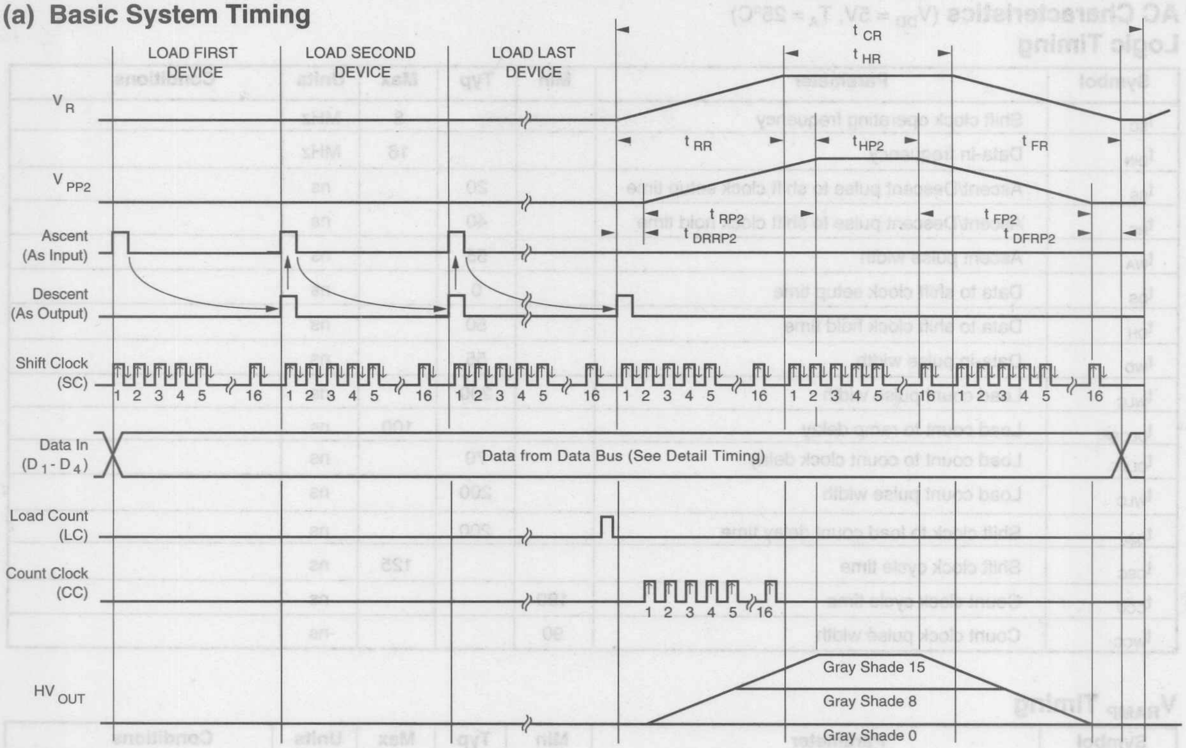
Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{SC}	Shift clock operating frequency			8	MHz	
f_{DIN}	Data-in frequency			16	MHz	
t_{SS}	Ascent/Descent pulse to shift clock setup time		20		ns	
t_{HS}	Ascent/Descent pulse to shift clock hold time		40		ns	
t_{WA}	Ascent pulse width		55		ns	
t_{DS}	Data to shift clock setup time		0		ns	
t_{DH}	Data to shift clock hold time		50		ns	
t_{WD}	Data-in pulse width		55		ns	
t_{WLC}	Load count pulse width		200		ns	
t_{DLCR}	Load count to ramp delay			100	ns	
t_{DLCC}	Load count to count clock delay		70		ns	
t_{WLC}	Load count pulse width		200		ns	
t_{DSL}	Shift clock to load count delay time		200		ns	
t_{CSC}	Shift clock cycle time			125	ns	
t_{CCC}	Count clock cycle time	190			ns	
t_{WCC}	Count clock pulse width	90			ns	

V_{RAMP} Timing

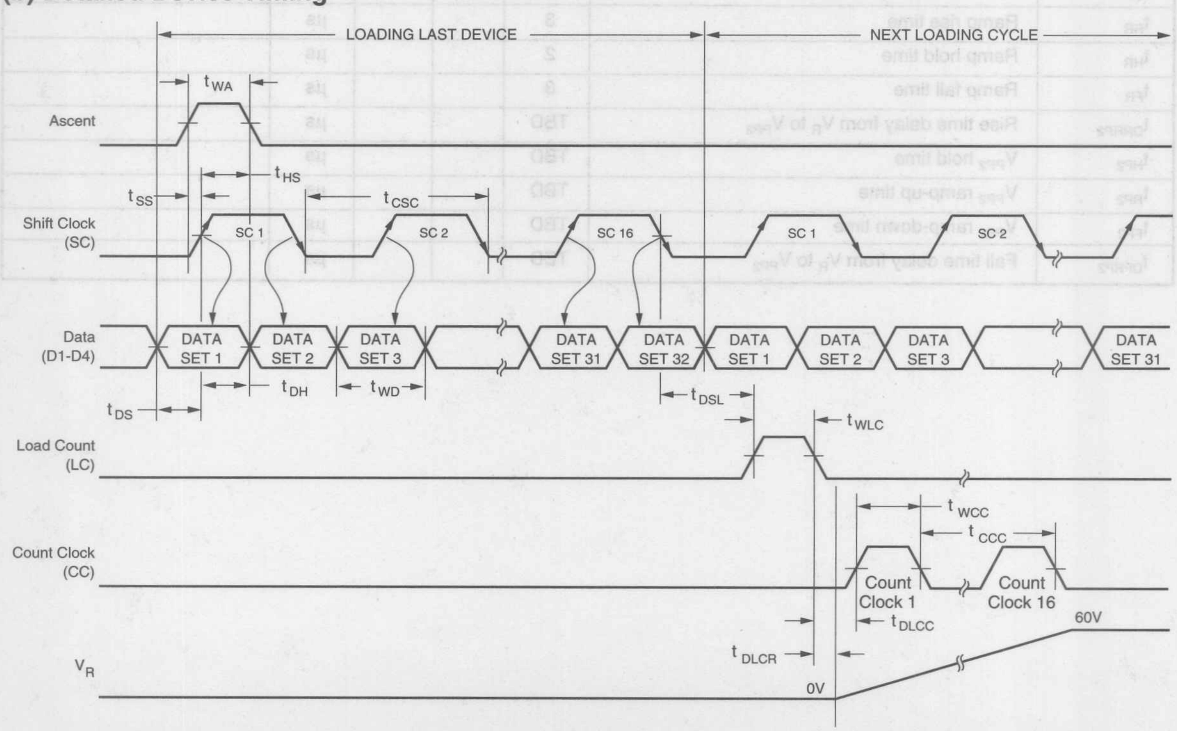
Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{CR}	Cycle time of ramp signal	8			µs	
t_{RR}	Ramp rise time	3			µs	
t_{HR}	Ramp hold time	2			µs	
t_{FR}	Ramp fall time	3			µs	
t_{DRRP2}	Rise time delay from V_R to V_{PP2}	TBD			µs	
t_{HP2}	V_{PP2} hold time	TBD			µs	
t_{RP2}	V_{PP2} ramp-up time	TBD			µs	
t_{FP2}	V_{PP2} ramp-down time	TBD			µs	
t_{DFRP2}	Fall time delay from V_R to V_{PP2}	TBD			µs	

Timing Diagrams

(a) Basic System Timing



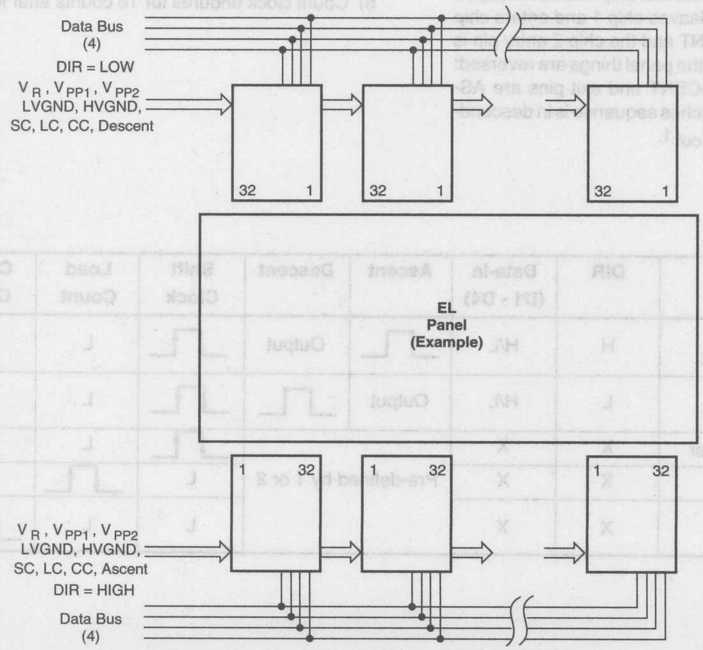
(b) Detailed Device Timing



Pin Definitions

Pin #	Name	Function
27-30	D1-D4	Inputs for binary-format parallel data
26	Shift clock	Triggers data on both rising and falling edges. This implies that the data rate is always twice the clock rate (data rate = 16MHz max if clock rate = 8MHz max)
22	Ascent	Input pin for the Ascent pulse (when DIR is high). Output pin for Descent pulse (when DIR is low).
43	Descent	Input pin for the Descent pulse (when DIR is low). Output pin for the Ascent pulse (when DIR is high).
40	Load Count	Input for a pulse whose rising edge causes data from the input latches to enter the comparator latches, and whose falling edge initiates the conversion of this binary data to an output level (D-to-A).
42	Count Clock	Input to the count clock generator whose increments are compared to the data in the comparator latches.
18,47	V_R	High-voltage ramp input for charging the output stage hold capacitors (C_H). This input can be linear or non-linear as desired.
32	DIR	When this pin is connected to V_{DD}, input data is shifted in ascending order, i.e. corresponding to $HV_{OUT}1$ to $HV_{OUT}32$. When connected to LVGND, input data is shifted in descending order, i.e. corresponding to $HV_{OUT}32$ to $HV_{OUT}1$.
31	LVGND	This is ground for the logic section. It may be connected to the HVGND pin, or kept separate in energy recovery circuits.
20,45	HVGND	This is ground for the high-voltage (output) section. It may be connected to the LVGND pin, or kept separate in energy recovery circuits.
19,46	$V_{PP}1$	This input biases the level translators and the P-channel transistors that charge the holding caps (C_H).
17,48	$V_{PP}2$	This input biases the output source followers. It can be set equal to $V_{PP}1$ or can be ramped (especially in energy recovery schemes).
1-16 49-64	$HV_{OUT}1$ - $HV_{OUT}32$	High-voltage source-follower outputs.
33	V_{DD}	Low-voltage logic power supply.

Typical EL Panel Connections



Theory of Operation

The HV38 has two primary functions:

1) Loading data from the data bus and,
2) Gray-shade conversion
(converting latched data to output voltages).

Since the device was developed initially for electroluminescent displays, the operation will be described in terms that pertain to that technology. As shown by the Typical EL Drive Scheme, several HV38 packages are mounted at the top and bottom of a display panel. Data exists on a 4-bit bus (adjacent PC board traces) at top and bottom. The D1 through D4 inputs of each chip take data from the bus when either an ASCENT or DESCENT pulse is present at the chip. These pulses therefore act as a combination CHIP SELECT and LOCATION STROBE. Because of the way the chip HV_{OUT} pins are sequenced, data on the bus at the bottom of the display panel will be entered into the left-most chip as $HV_{OUT}1$, $HV_{OUT}2$, etc. up to $HV_{OUT}32$. The ASCENT pulse will accomplish this with DIR = High.

Loading Data from Data Bus

Here is the full data-entry sequence:

1) The microcontroller puts data on the bus (4 bits)
2) To enter the data into the 32 sets of 4 latches on the first chip, the shift clock rises. This positive transition is combined with the ASCENT pulse (sometimes called a SEED BIT) and is generated only once to strobe the data into the first set of latches. (These latches eventually send data to the $HV_{OUT}1$). The data on the bus then changes, the shift clock falls, and this negative transition is combined with the ASCENT pulse, which is now propagated internally, to strobe the new data into the next set of 4 latches (which will end up as $HV_{OUT}2$). This internal ASCENT pulse therefore runs at twice the shift clock rate.
3) When the last set of 4 latches in the first chip has been loaded ($HV_{OUT}32$), the ASCENT pulse leaves chip 1 and enters chip 2. The exit pin is called DESCENT and the chip 2 entry pin is ASCENT. For chips at the top of the panel things are reversed: DIR is low, entry pins are DESCENT and exit pins are ASCENT, because the data-into-latches sequence is in descending order, $HV_{OUT}32$ down to $HV_{OUT}1$.
4) The buses may of course be separate, and data can be strobed in on an interleaved basis, etc., but those complications will be left to systems designers.

When data has been loaded into all 32 outputs of all chips (top and bottom of the display panel), the load count pin is pulsed. On its rising transition, all the data in the input latches is transferred to a like number of comparator latches, (thus leaving the data latches ready to receive new data during the following operations). After the transfer, the load count pin is brought low. This transition begins the events that convert the binary data into a gray-shade level.

Gray-shade Conversion

1) The COUNT CLOCK is started. This external signal is applied to the COUNT CLOCK pin, causing the counter on each chip to increment from binary 0000 to 1111 (0 to 15).
2) At the same time, the V_R voltage is applied to all chips, via charging transistors, causing the HOLD CAPACITORS (C_H) on each output to experience a rise in voltage.
3) If each set of comparator latches held binary 1111 (a count of 15), the V_R voltage would charge each C_H to the full value of V_R. The voltage followers on each output would thus present this level as a maximum-brightness output to the panel.
4) On the other hand, if the count in the comparator latches is less than maximum, when the COUNT CLOCK had incremented the master counter to a value that matched the latch value, that particular charging transistor would be cut off, leaving that C_H at some other value of voltage (gray-shade level).

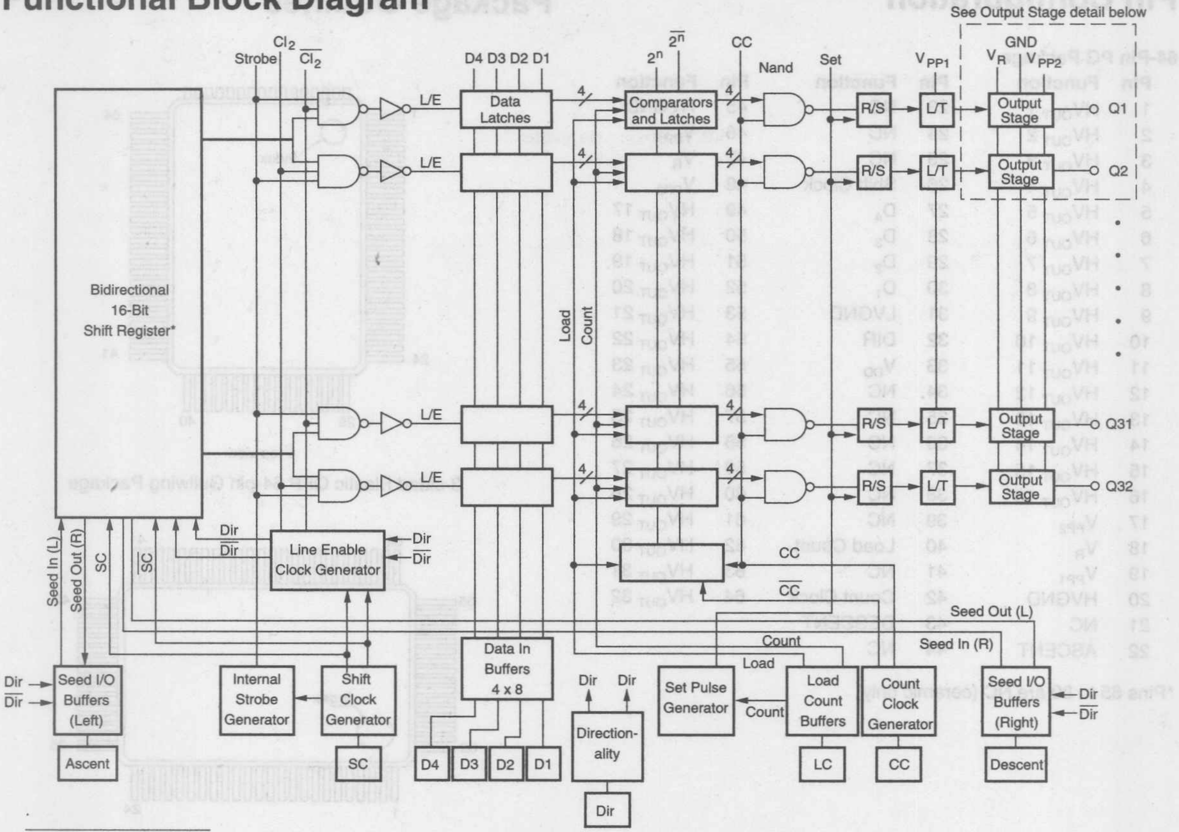
It should be clear that :

a) Data continues until all latches in all chips are loaded. The shift clock and the internal ASCENT/DESCENT pulses last for the same duration.
b) Count clock endures for 16 counts after load count goes low.

Function Table

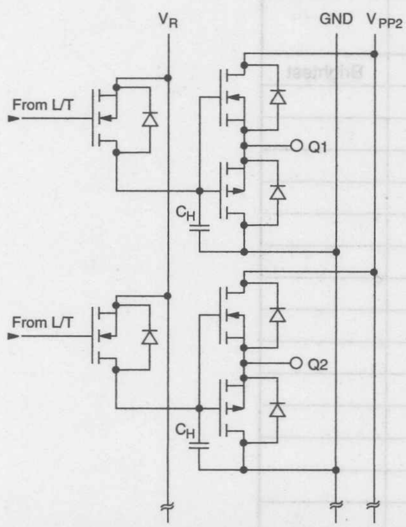
Sequence	Function	DIR	Data-In (D1 - D4)	Ascent	Descent	Shift Clock	Load Count	Count Clock	V_R
1	Shift Data from $HV_{OUT}1$ to 32	H	H/L		Output		L	L	L
2	Shift Data from $HV_{OUT}32$ to 1	L	H/L	Output			L	L	L
3	Load Shift Register	X	X				L	L	L
4	Load Counter	X	X	Pre-defined by 1 or 2		L		L	L
5	Counting/Voltage Conversion	X	X			L	L		Initiates V_{RAMP}

Functional Block Diagram



* Uses both clock edges.

Output Stage Detail



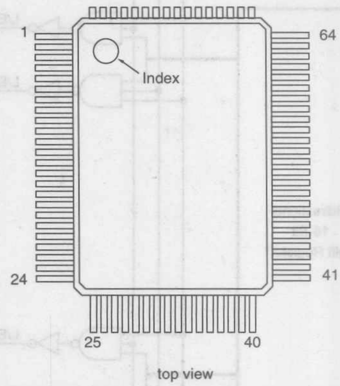
Pin Configuration

64-Pin PG Package

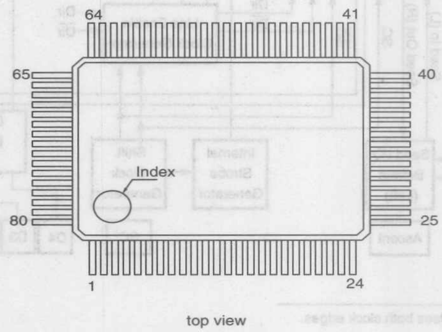
Pin	Function	Pin	Function	Pin	Function
1	HV_{OUT} 1	23	NC	45	HVGND
2	HV_{OUT} 2	24	NC	46	V_{PP1}
3	HV_{OUT} 3	25	NC	47	V_R
4	HV_{OUT} 4	26	Shift Clock	48	V_{PP2}
5	HV_{OUT} 5	27	D_4	49	HV_{OUT} 17
6	HV_{OUT} 6	28	D_3	50	HV_{OUT} 18
7	HV_{OUT} 7	29	D_2	51	HV_{OUT} 19
8	HV_{OUT} 8	30	D_1	52	HV_{OUT} 20
9	HV_{OUT} 9	31	LVGND	53	HV_{OUT} 21
10	HV_{OUT} 10	32	DIR	54	HV_{OUT} 22
11	HV_{OUT} 11	33	V_{DD}	55	HV_{OUT} 23
12	HV_{OUT} 12	34	NC	56	HV_{OUT} 24
13	HV_{OUT} 13	35	NC	57	HV_{OUT} 25
14	HV_{OUT} 14	36	NC	58	HV_{OUT} 26
15	HV_{OUT} 15	37	NC	59	HV_{OUT} 27
16	HV_{OUT} 16	38	NC	60	HV_{OUT} 28
17	V_{PP2}	39	NC	61	HV_{OUT} 29
18	V_R	40	Load Count	62	HV_{OUT} 30
19	V_{PP1}	41	NC	63	HV_{OUT} 31
20	HVGND	42	Count Clock	64	HV_{OUT} 32
21	NC	43	DESCENT		
22	ASCENT	44	NC		

*Pins 65 to 80 are NC (ceramic only)

Package Outlines



3-sided Plastic QFP 64-pin Gullwing Package



80-pin Gullwing Package
80-pin Ceramic Gullwing Package

Gray Shade Decoding Scheme

Brightest Shade No.	D4	D3	D2	D1	
15	1	1	1	1	Brightest
14	1	1	1	0	
13	1	1	0	1	
12	1	1	0	0	
11	1	0	1	1	
10	1	0	1	0	
9	1	0	0	1	
8	1	0	0	0	
7	0	1	1	1	
6	0	1	1	0	
5	0	1	0	1	
4	0	1	0	0	
3	0	0	1	1	
2	0	0	1	0	
1	0	0	0	1	
0	0	0	0	0	Dimmest

Supertex inc.

HV41
HV42

32-Channel Serial To Parallel Converter With P-Channel Open Drain Outputs

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV41	HV4122DJ	HV4122PJ	HV4122X	RBHV4122DJ
HV42	HV4222DJ	HV4222PJ	HV4222X	RBHV4222DJ

* For Hi-Rel process flows, please refer to page 5-3 in the Databook

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages to -225V
- ☐ Source current minimum 80mA
- ☐ Shift register speed 8MHz
- ☐ Strobe and enable inputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ 44-lead plastic and ceramic surface mount packages
- ☐ Hi-Rel processing available
- ☐ Can be used with the HV51 and HV52 to provide 200V push-pull operation

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		+0.5V to -15.5V
Off state output voltage[1]		+0.5V to -250V
Logic input levels[1]		+0.5V to V_{DD} - 0.5V
Ground current[2]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 85°C at 15mW/°C.

General Description

The HV41 and HV42 are low voltage serial to high voltage parallel converters wtih P-Channel open drain outputs.These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the logic high to low transition of the clock. The HV41 shifts in the counterclockwise direction when viewed from the top of the package and the HV42 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

For applications requiring active pull down as well as pull up, the HV41 and HV42 can be paired with the HV52 and HV51 devices, respectively.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics (voltages referenced to V_{SS})

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			-15	mA	f_{CLK} = 8 MHz F_{DATA} = 4 MHz
I_{DDQ}	Quiescent V_{DD} supply current			-100	µA	ALL V_{IN} = 0V
$I_{O(OFF)}$	Off state output current			-100	µA	All SWS parallel
I_{IH}	High-level logic input current			-1	µA	V_{IH} = -12V
I_{IL}	Low-level logic input current			+1	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} + 1.0V		V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}		-30.0	V	I_{HVout} = -80mA
		Data out		-1.0	V	I_{Dout} = -100µA
V_{OC}	HV_{OUT} clamp voltage			+1.5	V	I_{OL} = +80mA

AC Characteristics (@ V_{DD} = -12V, V_{SS} = 0V)

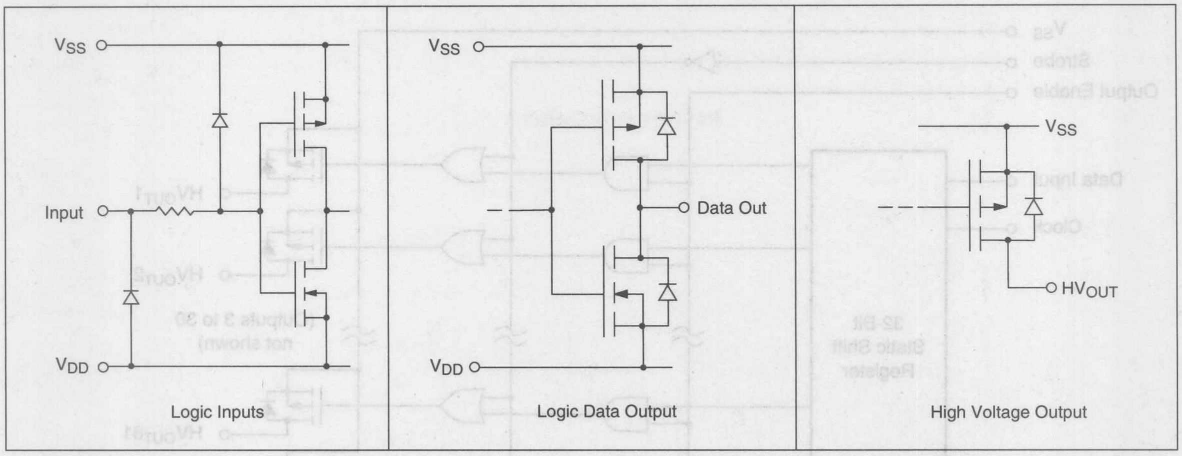
Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	50		ns	
t_H	Data hold time after clock rises	20		ns	
t_{ON}	Turn ON time, HV_{OUT} from enable		400	ns	R_L = 10K to -225V
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF

Recommended Operating Conditions

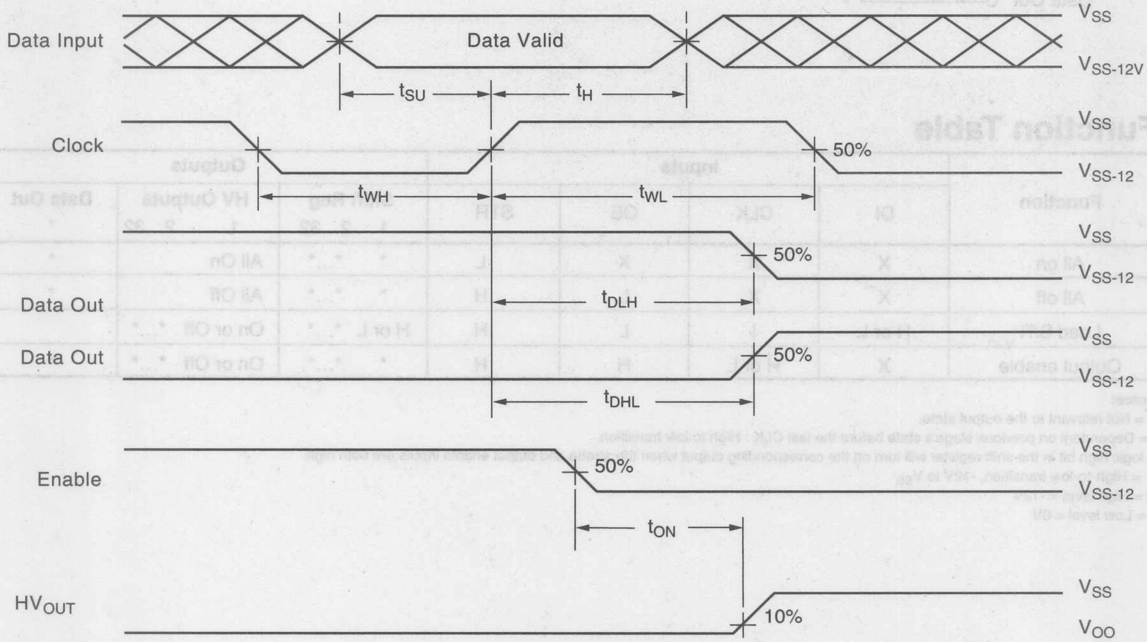
Symbol	Parameter		Min	Nom	Max	Units
V_{DD}	Logic supply voltage		-10.8	-12	-13.2	V
V_{OO}	Output off voltage		+0.3		-225	V
V_{IH}	High-level input voltage (LOGIC "1")		V_{DD} + 2V		V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")		0		-2.0	V
f_{CLK}	Clock frequency				8	MHz
T_A	Operating free-air temperature	Commercial	-40		+85	°C
		Military Hi-Rel (RB)	-55		+125	°C

Note : All voltages are referenced to V_{SS}.

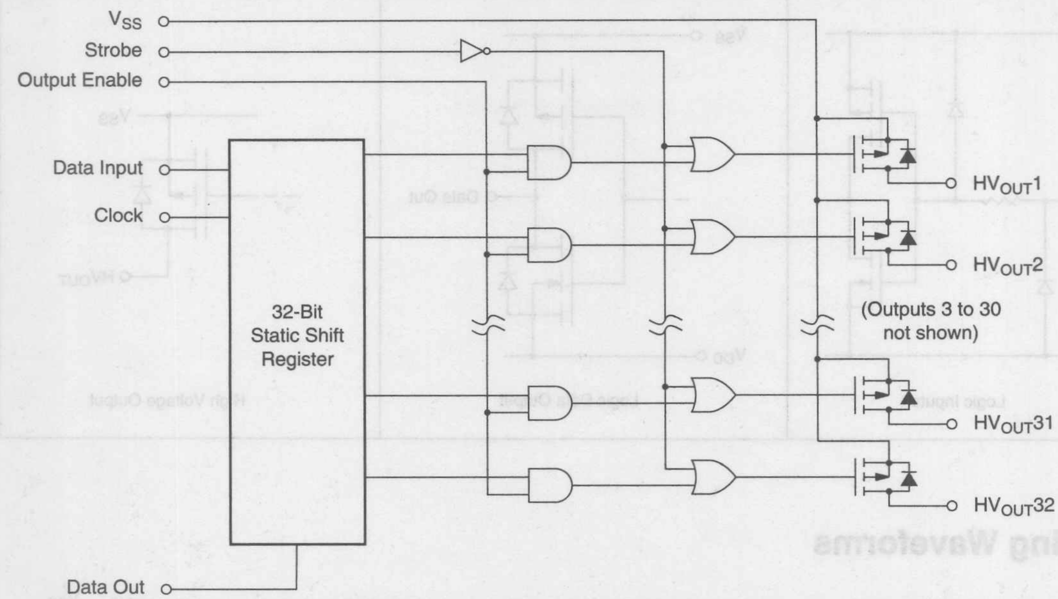
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs				
	DI	CLK	OE	STR	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out *
All on	X	X	X	L	*	*…*	All On		*
All off	X	X	L	H	*	*…*	All Off		*
Load S/R	H or L	↓	L	H	H or L	*…*	On or Off	*…*	
Output enable	X	H or L	H	H	*	*…*	On or Off	*…*	*

Notes:
X = Not relevant to the output state.
* = Dependent on previous stage's state before the last CLK : High to low transition.
A logic high bit in the shift register will turn on the corresponding output when the strobe and output enable inputs are both high.
↓ = High-to-low transition, -12V to V_{SS}
H = High level = -12V
L = Low level = 0V

Pin Configurations

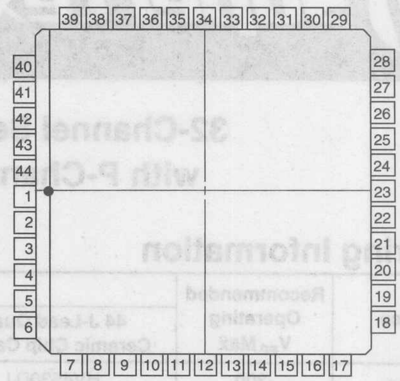
HV41
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	Output Enable
2	HV_{OUT} 18	24	Clock
3	HV_{OUT} 19	25	V_{SS}
4	HV_{OUT} 20	26	V_{DD}
5	HV_{OUT} 21	27	Strobe
6	HV_{OUT} 22	28	Data In
7	HV_{OUT} 23	29	HV_{OUT} 1
8	HV_{OUT} 24	30	HV_{OUT} 2
9	HV_{OUT} 25	31	HV_{OUT} 3
10	HV_{OUT} 26	32	HV_{OUT} 4
11	HV_{OUT} 27	33	HV_{OUT} 5
12	HV_{OUT} 28	34	HV_{OUT} 6
13	HV_{OUT} 29	35	HV_{OUT} 7
14	HV_{OUT} 30	36	HV_{OUT} 8
15	HV_{OUT} 31	37	HV_{OUT} 9
16	HV_{OUT} 32	38	HV_{OUT} 10
17	N/C	39	HV_{OUT} 11
18	Data Out	40	HV_{OUT} 12
19	N/C	41	HV_{OUT} 13
20	N/C	42	HV_{OUT} 14
21	N/C	43	HV_{OUT} 15
22	N/C	44	HV_{OUT} 16

HV42
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	Output Enable
2	HV_{OUT} 15	24	Clock
3	HV_{OUT} 14	25	V_{SS}
4	HV_{OUT} 13	26	V_{DD}
5	HV_{OUT} 12	27	Strobe
6	HV_{OUT} 11	28	Data In
7	HV_{OUT} 10	29	HVout 32
8	HV_{OUT} 9	30	HV_{OUT} 31
9	HV_{OUT} 8	31	HV_{OUT} 30
10	HV_{OUT} 7	32	HV_{OUT} 29
11	HV_{OUT} 6	33	HV_{OUT} 28
12	HV_{OUT} 5	34	HV_{OUT} 27
13	HV_{OUT} 4	35	HV_{OUT} 26
14	HV_{OUT} 3	36	HV_{OUT} 25
15	HV_{OUT} 2	37	HV_{OUT} 24
16	HV_{OUT} 1	38	HV_{OUT} 23
17	N/C	39	HV_{OUT} 22
18	Data Out	40	HV_{OUT} 21
19	N/C	41	HV_{OUT} 20
20	N/C	42	HV_{OUT} 19
21	N/C	43	HV_{OUT} 18
22	N/C	44	HV_{OUT} 17

Package Outline



top view

44-pin J-Lead Package

11

Supertex inc.

HV45
HV46

32-Channel Serial To Parallel Converter with P-Channel Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options			
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	44 Quad Plastic Gullwing	Die
HV45	-300	HV4530DJ	HV4530PJ	HV4530PG	HV4530X
	-220	HV4522DJ	HV4522PJ	HV4522PG	HV4522X
HV46	-300	HV4630DJ	HV4630PJ	HV4630PG	HV4630X
	-220	HV4622DJ	HV4622PJ	HV4622PG	HV4622X

Features

- Processed with HVCMOS Technology
- Output voltages to -300V
- Source current minimum 60 mA
- Shift register speed 8 MHz
- Polarity and blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- 44-lead plastic and ceramic surface mount packages
- Hi-Rel processing available
- Can be used with the HV55 and HV56 to provide 300V push pull operation

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		+0.5V to -16V
Off state output voltage	HV4530/HV4630	+0.5V to -315V
	HV4522/ HV4622	+0.5V to -220V
Logic input levels[1]		+0.5V to V_{DD} - 0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Ceramic	-40°C to +85°C
	Plastic	0°C to +70°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV45 and HV46 are low-voltage serial to high-voltage parallel converters with P-Channel open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register, 32 data latches, and control logic to perform polarity and blanking functions. Data is shifted through the shift register on the logic high-to-low transition of the clock. The HV45 shifts in the counterclockwise direction when viewed from the top of the package and the HV46 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. The data in the shift register is latched when the latch enable pin is brought to logic high and then returned to ground. If the latch enable pin is held high, the latch becomes transparent and the shift register data is directly reflected in the outputs.

For applications requiring active pull down as well as pull up, the HV45 and HV46 can be paired with the HV55 and HV56 devices, respectively.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			-15	mA	f_{CLK} = 8 MHz F_{DATA} = 4 MHz
I_{DDQ}	Quiescent V_{DD} supply current			-100	µA	$V_{IN} = V_{SS}$ or V_{DD}
$I_{O(OFF)}$	Off state output current			-100	µA	All SWS parallel
I_{IH}	High-level logic input current			-1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			+1	µA	$V_{IL} = V_{SS}$
V_{OH}	High-level output data out		V_{DD} + 1.0V		V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}		-30.0	V	I_{HVout} = -60mA
		Data out		-1.0	V	I_{Dout} = -100µA
V_{OC}	HV_{OUT} clamp voltage			+1.5	V	I_{OL} = +60mA

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	50		ns	
t_H	Data hold time after clock rises	20		ns	
t_{ON}	Turn ON time, HV_{OUT} from enable		400	ns	R_L = 10K to V_{OO} MAX
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		-10.8	-13.2	V
V_{OO}	Output off voltage	HV4530 and HV4630	+0.3	-300	V
		HV4522 and HV4622	+0.3	-220	V
V_{IH}	High-level input voltage (LOGIC "1")		V_{DD} + 2V	V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")		0	-2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	0	70	°C
		Military Hi-Rel (RB)	-55	+125	°C

Note 1: All voltages are referenced to V_{SS}.

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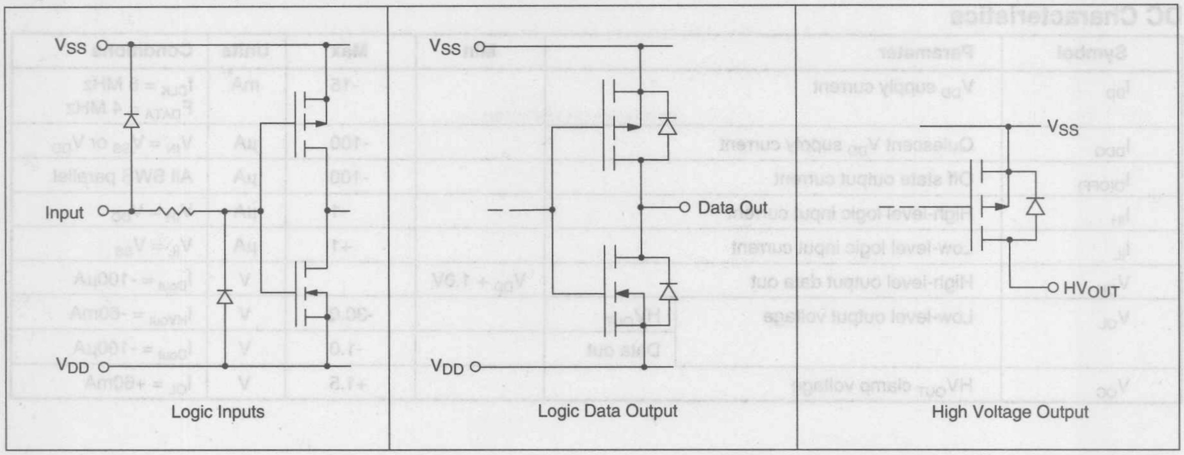
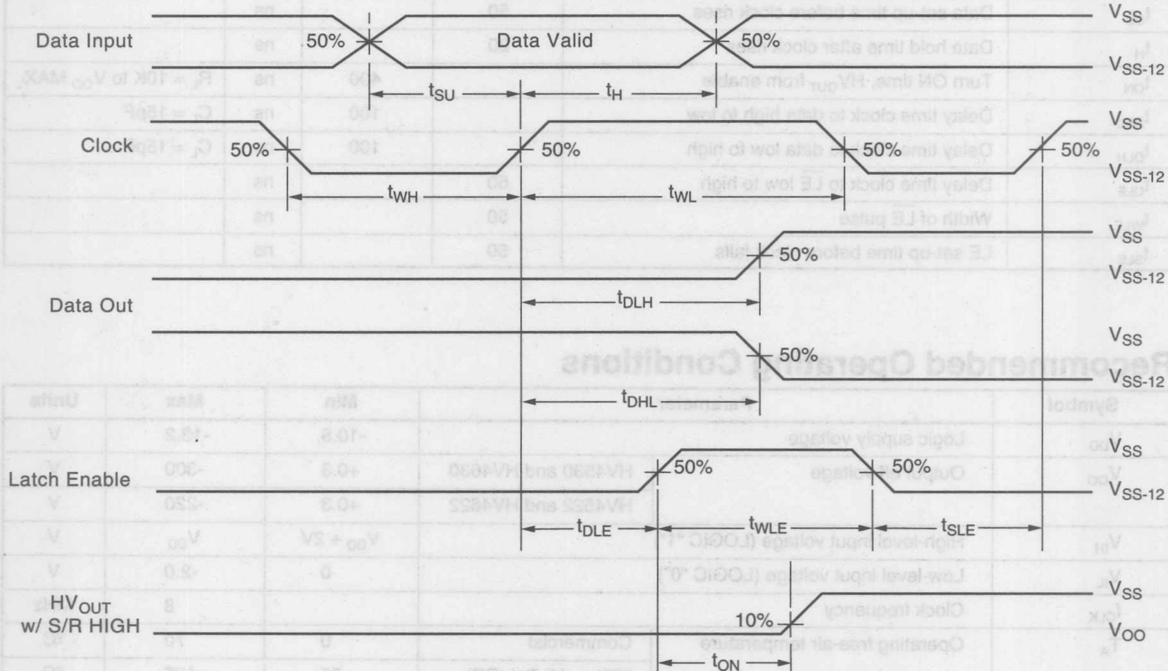
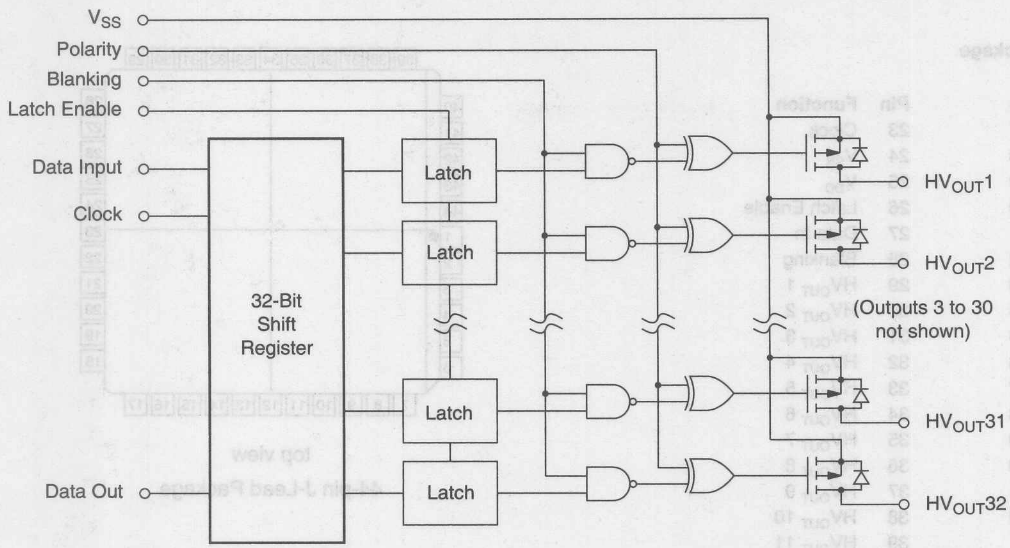
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out *
All on	X	X	X	L	L	*	*…*	H	H…H	*
All off	X	X	X	L	H	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*…*	*	*…*	*
Load latches	X	H or L	↑	H	H	*	*…*	*	*…*	*
	X	H or L	↑	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Transparent latch mode	L	↓	H	H	H	L	*…*	L	*…*	*
	H	↓	H	H	H	H	*…*	H	*…*	*

Notes:
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition, -12V to V_{SS}.
* = dependent on previous stage's state before the last CLK Ø or last LE high.

Pin Configurations

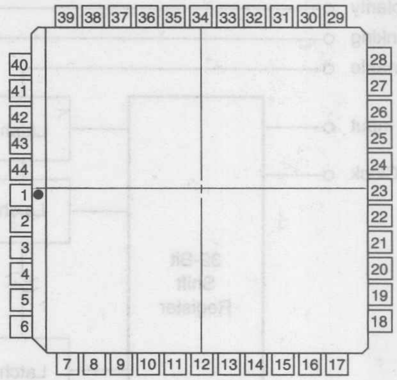
HV45
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	Clock
2	HV_{OUT} 18	24	V_{SS}
3	HV_{OUT} 19	25	V_{DD}
4	HV_{OUT} 20	26	Latch Enable
5	HV_{OUT} 21	27	Data In
6	HV_{OUT} 22	28	Blanking
7	HV_{OUT} 23	29	HV_{OUT} 1
8	HV_{OUT} 24	30	HV_{OUT} 2
9	HV_{OUT} 25	31	HV_{OUT} 3
10	HV_{OUT} 26	32	HV_{OUT} 4
11	HV_{OUT} 27	33	HV_{OUT} 5
12	HV_{OUT} 28	34	HV_{OUT} 6
13	HV_{OUT} 29	35	HV_{OUT} 7
14	HV_{OUT} 30	36	HV_{OUT} 8
15	HV_{OUT} 31	37	HV_{OUT} 9
16	HV_{OUT} 32	38	HV_{OUT} 10
17	N/C	39	HV_{OUT} 11
18	Data Out	40	HV_{OUT} 12
19	N/C	41	HV_{OUT} 13
20	N/C	42	HV_{OUT} 14
21	N/C	43	HV_{OUT} 15
22	Polarity	44	HV_{OUT} 16

HV46
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	Clock
2	HV_{OUT} 15	24	V_{SS}
3	HV_{OUT} 14	25	V_{DD}
4	HV_{OUT} 13	26	Latch Enable
5	HV_{OUT} 12	27	Data In
6	HV_{OUT} 11	28	Blanking
7	HV_{OUT} 10	29	HVout 32
8	HV_{OUT} 9	30	HV_{OUT} 31
9	HV_{OUT} 8	31	HV_{OUT} 30
10	HV_{OUT} 7	32	HV_{OUT} 29
11	HV_{OUT} 6	33	HV_{OUT} 28
12	HV_{OUT} 5	34	HV_{OUT} 27
13	HV_{OUT} 4	35	HV_{OUT} 26
14	HV_{OUT} 3	36	HV_{OUT} 25
15	HV_{OUT} 2	37	HV_{OUT} 24
16	HV_{OUT} 1	38	HV_{OUT} 23
17	N/C	39	HV_{OUT} 22
18	Data Out	40	HV_{OUT} 21
19	N/C	41	HV_{OUT} 20
20	N/C	42	HV_{OUT} 19
21	N/C	43	HV_{OUT} 18
22	Polarity	44	HV_{OUT} 17

Package Outline



top view
44-pin J-Lead Package

Pin Configurations

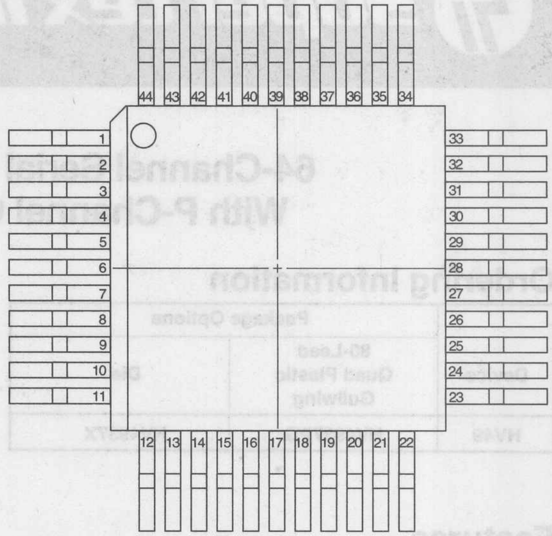
HV45
44-Pin Plastic Gullwing (QFP) Package

Pin	Function	Pin	Function
1	HV_{OUT} 12	23	Data Out
2	HV_{OUT} 13	24	N/C
3	HV_{OUT} 14	25	N/C
4	HV_{OUT} 15	26	N/C
5	HV_{OUT} 16	27	Polarity
6	HV_{OUT} 17	28	Clock
7	HV_{OUT} 18	29	V_{SS}
8	HV_{OUT} 19	30	V_{DD}
9	HV_{OUT} 20	31	Latch Enable
10	HV_{OUT} 21	32	Data In
11	HV_{OUT} 22	33	Blanking
12	HV_{OUT} 23	34	HV_{OUT} 1
13	HV_{OUT} 24	35	HV_{OUT} 2
14	HV_{OUT} 25	36	HV_{OUT} 3
15	HV_{OUT} 26	37	HV_{OUT} 4
16	HV_{OUT} 27	38	HV_{OUT} 5
17	HV_{OUT} 28	39	HV_{OUT} 6
18	HV_{OUT} 29	40	HV_{OUT} 7
19	HV_{OUT} 30	41	HV_{OUT} 8
20	HV_{OUT} 31	42	HV_{OUT} 9
21	HV_{OUT} 32	43	HV_{OUT} 10
22	N/C	44	HV_{OUT} 11

HV46
44-Pin Plastic Gullwing (QFP) Package

Pin	Function	Pin	Function
1	HV_{OUT} 21	23	Data Out
2	HV_{OUT} 20	24	N/C
3	HV_{OUT} 19	25	N/C
4	HV_{OUT} 18	26	N/C
5	HV_{OUT} 17	27	Polarity
6	HV_{OUT} 16	28	Clock
7	HV_{OUT} 15	29	V_{SS}
8	HV_{OUT} 14	30	V_{DD}
9	HV_{OUT} 13	31	Latch Enable
10	HV_{OUT} 12	32	Data In
11	HV_{OUT} 11	33	Blanking
12	HV_{OUT} 10	34	HV_{OUT} 32
13	HV_{OUT} 9	35	HV_{OUT} 31
14	HV_{OUT} 8	36	HV_{OUT} 30
15	HV_{OUT} 7	37	HV_{OUT} 29
16	HV_{OUT} 6	38	HV_{OUT} 28
17	HV_{OUT} 5	39	HV_{OUT} 27
18	HV_{OUT} 4	40	HV_{OUT} 26
19	HV_{OUT} 3	41	HV_{OUT} 25
20	HV_{OUT} 2	42	HV_{OUT} 24
21	HV_{OUT} 1	43	HV_{OUT} 23
22	N/C	44	HV_{OUT} 22

Package Outline



top view
44-pin PQFP Package

Preliminary

64-Channel Serial To Parallel Converter With P-Channel Open Drain Outputs

Ordering Information

Device	Package Options	
	80-Lead Quad Plastic Gullwing	Die
HV49	HV4937PG	HV4937X

Features

- ☐ HVCMOS® Technology
- ☐ Output voltages up to -375V
- ☐ Source current minimum 0.5mA
- ☐ Shift register speed 6 MHz
- ☐ Latched outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	+0.5V to -15V
Supply voltage, V_{PP}	+0.5V to -375V
Logic input levels	+0.5V to V_{DD} -0.5V
Ground current	0.75A
Continuous total power dissipation[2]	1200mW
Operating temperature range	0°C to +85°C
Storage temperature range	-65°C to +150°C

Notes:
1. All voltages are referenced to V_{SS}.
2. For operation above 25°C ambient derate linearly by 15mW/°C up to 85°C.

General Description

The HV49 is a low voltage serial to high voltage parallel converter with open drain outputs. It has been designed especially for use as a driver for electrostatic printers.

This device consists of a 64-bit shift register, 64 latches, latch enable (LE), and output enable (OE). Data is shifted through the shift register on the high to low transition of the clock. When the DIR pin is set high, the HV49 shifts in the counterclockwise direction when viewed from the top of the package. When the DIR pin is set low, the HV49 shifts in the clockwise direction. A serial data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE or the OE inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is stored when LE is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				-15	mA	f_{CLK} = 6MHz, f_{DATA} = 3MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				-250	µA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current at 25°C, per Switch				-100	nA	Output high, and at -375V
I_{IH}	High-Level Logic Input Current				-10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				+10	µA	V_I = 0V
V_{OH}	High-Level Data Out				V_{DD} +1	V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}	-10			V	IHV_{OUT} = -0.5mA
		Data Out	-1			V	ID_{OUT} = 100µA
V_{OC}	HV_{OUT} Clamp Voltage				-3.0	V	I_{OL} = 1mA
C_{HVO}	Output Capacitance per Channel				3	pF	V_{DS} = 100V

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			6	MHz	
t_W	Clock Width High or Low	83			ns	
t_{SU}	Data Setup Time Before Clock Falls	35			ns	
t_H	Data Hold Time After Clock Falls	15			ns	
t_{WLE}	Width of Latch Enable Pulse	83			ns	
t_{DLE}	$\overline{LE}$ Delay Time After Falling Edge of Clock	35			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Falling Edge of Clock	40			ns	
t_{DHL}	Clock Delay Time Data High to Low			160	ns	
t_{DLH}	Clock Delay Time Data Low to High			160	ns	

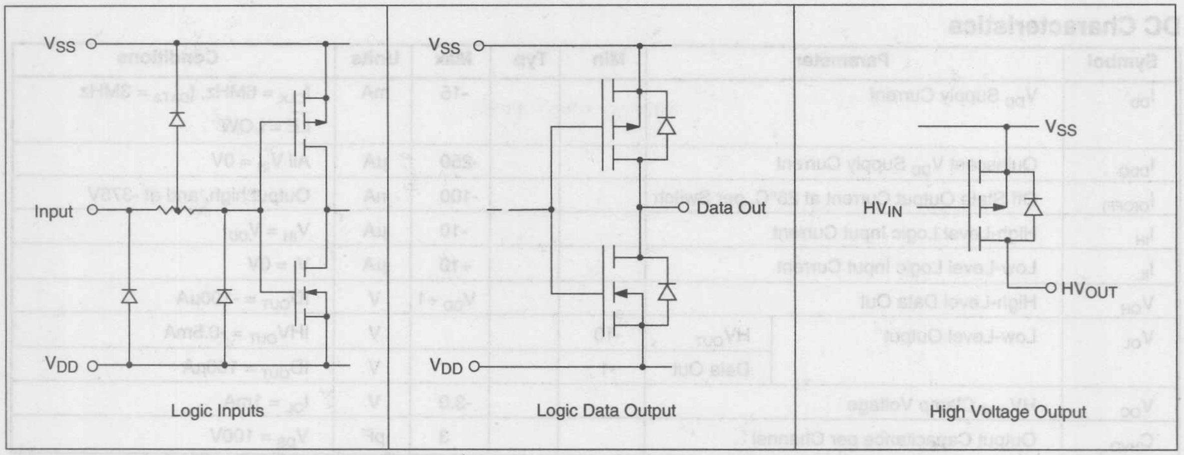
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	-10.8	-12	-13.2	V
V_{PP}	High voltage supply	-8.0		-375	V
V_{IH}	High-level input voltage	-3.5		V_{DD}	V
V_{IL}	Low-level input voltage	0		-0.8	V
T_A	Operating free-air temperature	0		+85	°C

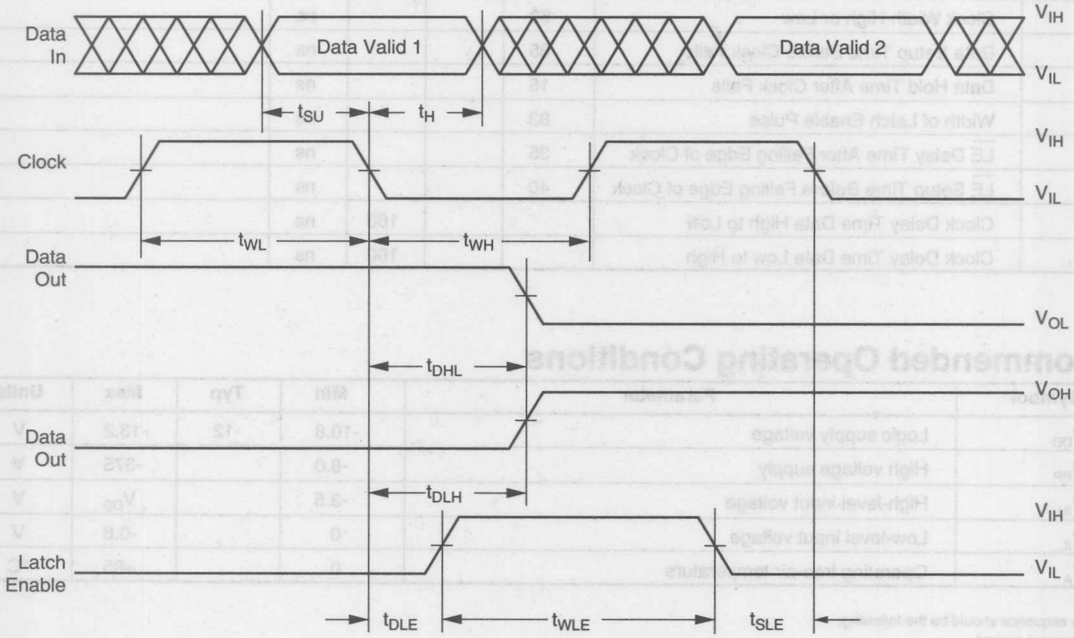
Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

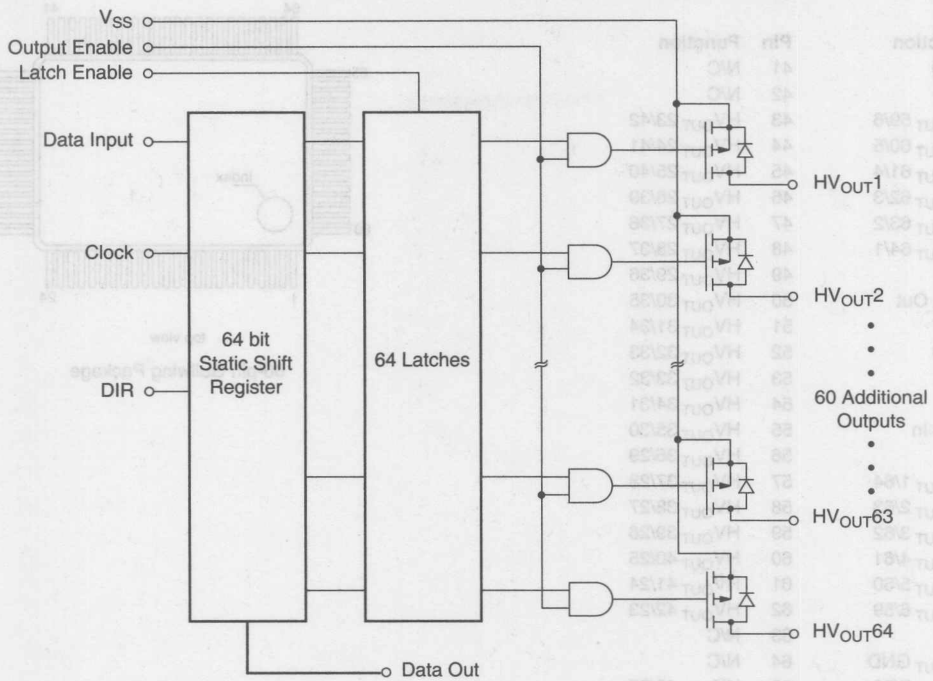
Input and Output Equivalent Circuit



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs		
	Data	CLK	LE	OE	DIR	Shift Reg 1 2 … 64	Latch 1 2 … 64	HV_{OUT} 1 2 … 64	D_{OUT}
All off	X	X	X	L	X	*…*	*…*	H…H	*
Load S/R	H or L	↓	L	L	H	H or L…Qn → Qn+1	*…*	H…H	*
	H or L	↓	L	L	L	H or L…Qn → Qn-1	*…*	H…H	*
Load Latch	H or L	↓	H	L	X	H or L…*	H or L…*	H…H	*
Output Enable Transparent Latch Mode	X	H or L	H	H	X	H or L…*	H or L…*	L or H…*	*
	H	↓	H	H	X	H…*	H…*	L…*	*
	L	↓	H	H	X	L…*	L…*	H…*	*

Notes:

X = Don't care
* = Dependent on previous stage's state before the last CLK : High to low transition.
↓ = -5V to V_{SS} transition
H = V_{PP}
L = GND

Pin Configurations

PG Package

HV49

Pin	Function	Pin	Function
1	GND	41	N/C
2	N/C	42	N/C
3	HV_{OUT} 59/6	43	HV_{OUT} 23/42
4	HV_{OUT} 60/5	44	HV_{OUT} 24/41
5	HV_{OUT} 61/4	45	HV_{OUT} 25/40
6	HV_{OUT} 62/3	46	HV_{OUT} 26/39
7	HV_{OUT} 63/2	47	HV_{OUT} 27/38
8	HV_{OUT} 64/1	48	HV_{OUT} 28/37
9	DIR	49	HV_{OUT} 29/36
10	Data Out	50	HV_{OUT} 30/35
11	CLK	51	HV_{OUT} 31/34
12	GND	52	HV_{OUT} 32/33
13	V_{DD}	53	HV_{OUT} 33/32
14	LE	54	HV_{OUT} 34/31
15	Data In	55	HV_{OUT} 35/30
16	OE	56	HV_{OUT} 36/29
17	HV_{OUT} 1/64	57	HV_{OUT} 37/28
18	HV_{OUT} 2/63	58	HV_{OUT} 38/27
19	HV_{OUT} 3/62	59	HV_{OUT} 39/26
20	HV_{OUT} 4/61	60	HV_{OUT} 40/25
21	HV_{OUT} 5/60	61	HV_{OUT} 41/24
22	HV_{OUT} 6/59	62	HV_{OUT} 42/23
23	N/C	63	N/C
24	HV_{OUT} GND	64	N/C
25	HV_{OUT} 7/58	65	HV_{OUT} 43/22
26	HV_{OUT} 8/57	66	HV_{OUT} 44/21
27	HV_{OUT} 9/56	67	HV_{OUT} 45/20
28	HV_{OUT} 10/55	68	HV_{OUT} 46/19
29	HV_{OUT} 11/54	69	HV_{OUT} 47/18
30	HV_{OUT} 12/53	70	HV_{OUT} 48/17
31	HV_{OUT} 13/52	71	HV_{OUT} 49/16
32	HV_{OUT} 14/51	72	HV_{OUT} 50/15
33	HV_{OUT} 15/50	73	HV_{OUT} 51/14
34	HV_{OUT} 16/49	74	HV_{OUT} 52/13
35	HV_{OUT} 17/48	75	HV_{OUT} 53/12
36	HV_{OUT} 18/47	76	HV_{OUT} 54/11
37	HV_{OUT} 19/46	77	HV_{OUT} 55/10
38	HV_{OUT} 20/45	78	HV_{OUT} 56/9
39	HV_{OUT} 21/44	79	HV_{OUT} 57/8
40	HV_{OUT} 22/43	80	HV_{OUT} 58/7

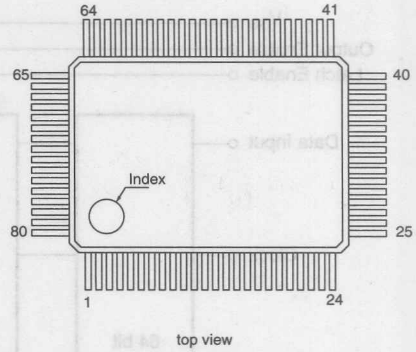
Note:

Pin designation DIR = H/L

Example: For DIR = H, Pin 3 is HV_{OUT} 59

For DIR = L, Pin 3 is HV_{OUT} 6

Package Outline



80-pin Gullwing Package

Supertex inc.

HV51
HV52

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Package Options				
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	44 Lead Quad Plastic Gullwing	Die	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV51	HV5122DJ	HV5122PJ	HV5122PG	HV5122X	RBHV5122DJ
HV52	HV5222DJ	HV5222PJ	HV5222PG	HV5222X	RBHV5222DJ

* For Hi-Rel process flows, please refer to perfer to page 5-3 in the Databook.

Features

- Processed with HVCMOS® technology
- Output voltages to 225V using a ramped supply voltage
- Sink current minimum 100mA
- Shift register speed 8MHz
- Strobe and enable inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- 44-lead ceramic surface mount package
- Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +15V
Output voltage, V_{PP}[2]		-0.5V to +250V
Logic input levels		-0.5V to V_{DD} + 0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55 to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV51 and HV52 are low voltage serial to high voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register and control logic to perform the Output Enable and All-ON functions. Data is shifted through the shift register on the high to low transition of the clock. The HV51 shifts in the counterclockwise direction when viewed from the top of the package and the HV52 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE (Output Enable) or the STR (Strobe) inputs.

The HV51 and HV52 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current				15	mA	f_{CLK} = 8MHz F_{DATA} = 4MHz
I_{DDQ}	Quiescent V_{DD} supply current				100	µA	All V_{IN} = 0V
$I_{O(OFF)}$	Off state output current				10	µA	All outputs high All SWS parallel
I_{IH}	High-level logic input current				1	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current				-1	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} - 1.0V			V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}			15.0	V	I_{HVout} = +100mA
		Data out			1.0	V	I_{Dout} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

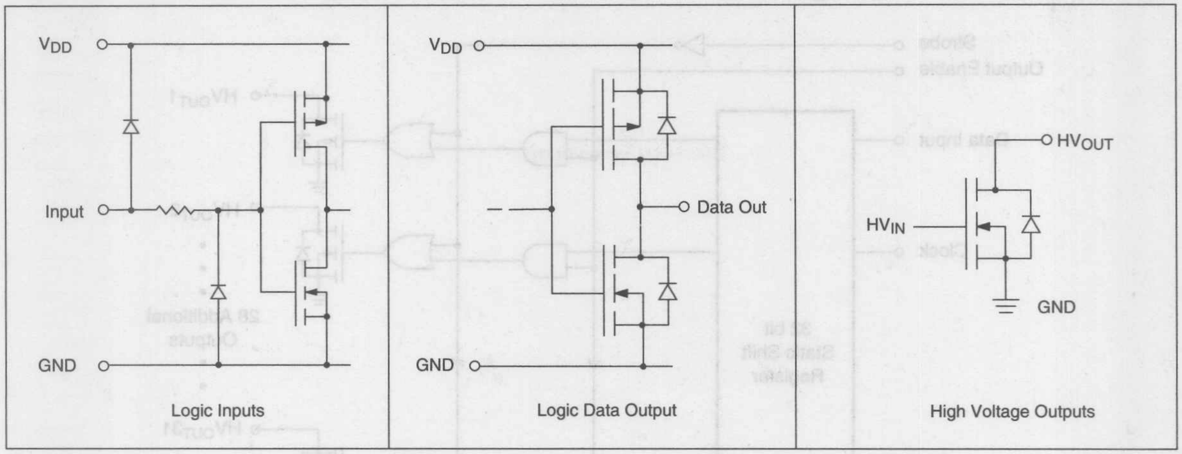
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency			8	MHz	
t_W	Clock width high or low	62			ns	
t_{SU}	Data set-up time before clock falls	25			ns	
t_H	Data hold time after clock falls	10			ns	
t_{ON}	Turn ON time, HV_{OUT} from enable			500	ns	R_L = 2KΩ to 200V
t_{DHL}	Delay time clock to data high to low			100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high			100	ns	C_L = 15pF

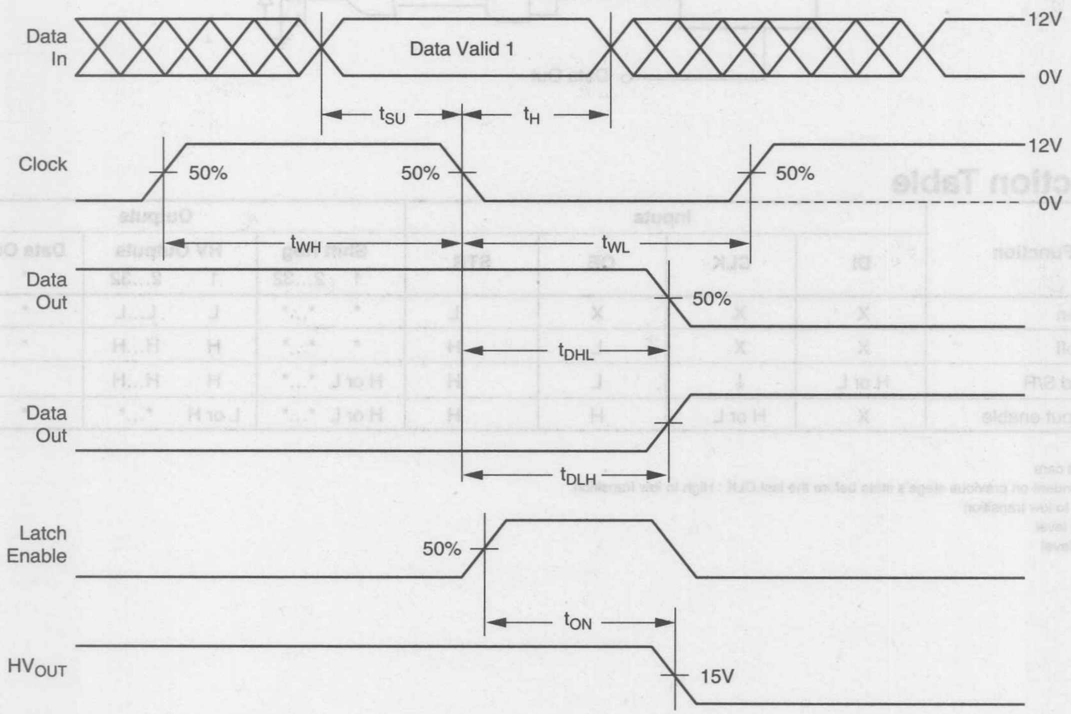
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply		8.0		225	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
f_{CLK}	Clock frequency				8	MHz
T_A	Operating free-air temperature	Commercial	-40		+85	°C
		Military Hi-Rel (RB)	-55		+125	°C

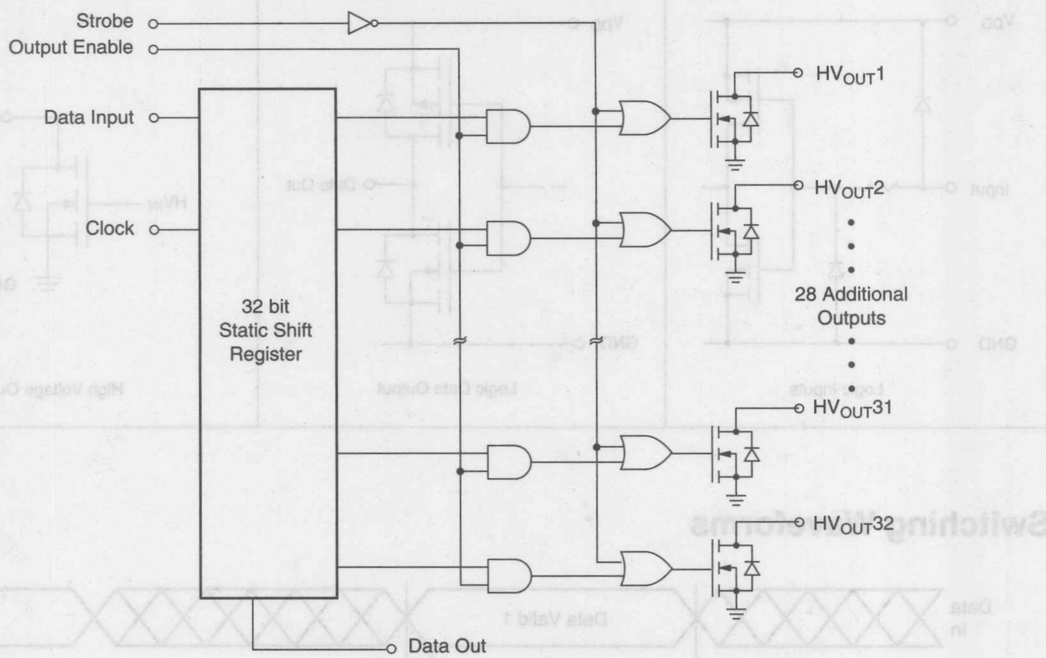
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Outputs		
	DI	CLK	OE	STR	Shift Reg 1 2…32	HV Outputs 1 2…32	Data Out
All on	X	X	X	L	* *…*	L L…L	*
All off	X	X	L	H	* *…*	H H…H	*
Load S/R	H or L	↓	L	H	H or L *…*	H H…H	
Output enable	X	H or L	H	H	H or L *…*	L or H *…*	*

Notes:
X = Don't care
* = Dependent on previous stage's state before the last CLK : High to low transition.
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

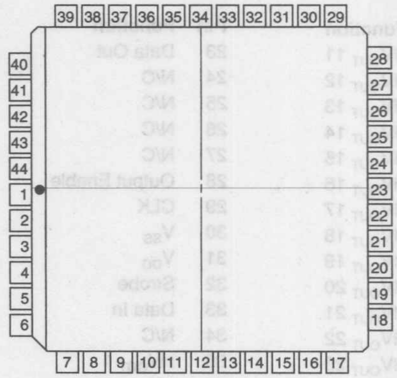
HV51
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	Output Enable
2	HV_{OUT} 17	24	Clock
3	HV_{OUT} 18	25	GND
4	HV_{OUT} 19	26	V_{DD}
5	HV_{OUT} 20	27	Stobe
6	HV_{OUT} 21	28	Data In
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	N/C	43	HV_{OUT} 14
22	NC	44	HV_{OUT} 15

HV52
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	Output Enable
2	HV_{OUT} 16	24	Clock
3	HV_{OUT} 15	25	GND
4	HV_{OUT} 14	26	V_{DD}
5	HV_{OUT} 13	27	Strobe
6	HV_{OUT} 12	28	Data In
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HVout 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	N/C	43	HV_{OUT} 19
22	N/C	44	HV_{OUT} 18

Package Outline



top view

44-pin J-Lead Package

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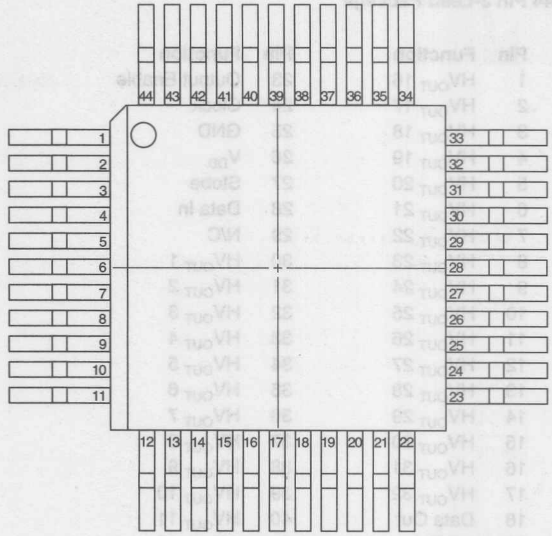
Pin Configurations

HV51
44-Pin Quad Plastic Package

Pin	Function	Pin	Function
1	HV_{OUT} 11	23	Data Out
2	HV_{OUT} 12	24	N/C
3	HV_{OUT} 13	25	N/C
4	HV_{OUT} 14	26	N/C
5	HV_{OUT} 15	27	N/C
6	HV_{OUT} 16	28	Output Enable
7	HV_{OUT} 17	29	CLK
8	HV_{OUT} 18	30	V_{SS}
9	HV_{OUT} 19	31	V_{DD}
10	HV_{OUT} 20	32	Strobe
11	HV_{OUT} 21	33	Data In
12	HV_{OUT} 22	34	N/C
13	HV_{OUT} 23	35	HV_{OUT} 1
14	HV_{OUT} 24	36	HV_{OUT} 2
15	HV_{OUT} 25	37	HV_{OUT} 3
16	HV_{OUT} 26	38	HV_{OUT} 4
17	HV_{OUT} 27	39	HV_{OUT} 5
18	HV_{OUT} 28	40	HV_{OUT} 6
19	HV_{OUT} 29	41	HV_{OUT} 7
20	HV_{OUT} 30	42	HV_{OUT} 8
21	HV_{OUT} 31	43	HV_{OUT} 9
22	HV_{OUT} 32	44	HV_{OUT} 10

Package Outline



top view

44-pin Quad Plastic Package

HV52
44-Pin Quad Plastic Package

Pin	Function	Pin	Function
1	HV_{OUT} 22	23	Data Out
2	HV_{OUT} 21	24	N/C
3	HV_{OUT} 20	25	N/C
4	HV_{OUT} 19	26	N/C
5	HV_{OUT} 18	27	N/C
6	HV_{OUT} 17	28	Output Enable
7	HV_{OUT} 16	29	CLK
8	HV_{OUT} 15	30	V_{SS}
9	HV_{OUT} 14	31	V_{DD}
10	HV_{OUT} 13	32	Strobe
11	HV_{OUT} 12	33	Data In
12	HV_{OUT} 11	34	N/C
13	HV_{OUT} 10	35	HV_{OUT} 32
14	HV_{OUT} 9	36	HV_{OUT} 31
15	HV_{OUT} 8	37	HV_{OUT} 30
16	HV_{OUT} 7	38	HV_{OUT} 29
17	HV_{OUT} 6	39	HV_{OUT} 28
18	HV_{OUT} 5	40	HV_{OUT} 27
19	HV_{OUT} 4	41	HV_{OUT} 26
20	HV_{OUT} 3	42	HV_{OUT} 25
21	HV_{OUT} 2	43	HV_{OUT} 24
22	HV_{OUT} 1	44	HV_{OUT} 23

HV53
HV54

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Package Options				
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	44 Lead Quad Plastic Gullwing	Die	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV53	HV5308DJ	HV5308PJ	HV5308PG	HV5308X	RBHV5308DJ
HV54	HV5408DJ	HV5408PJ	HV5408PG	HV5408X	RBHV5408DJ

* For Hi-Rel process flows, please refer to perfer to page 5-3 in the Databook.

Features

- ☐ Processed with HVCMOS® technology
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +16V
Supply voltage, V_{PP}		-0.5V to +80V
Logic input levels[2]		-0.5 to V_{DD} + 0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Ceramic Plastic	1500mW 1200mW
Operating temperature range	Commercial Military	-40°C to +85°C -55°C to 125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV53 and HV54 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. Q1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV54 shifts in the counterclockwise direction when viewed from the top of the package and the HV53 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

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Electrical Characteristics ($V_{PP} = 60V$, $V_{DD} = 12V$, $T_A = 25°C$)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PP}	V_{PP} Supply Current		0.5	mA	HVoutputs HIGH to LOW
I_{DDQ}	I_{DD} Supply Current (Quiescent)		100	μA	All inputs = V_{DD} or GND
I_{DD}	I_{DD} Supply Current (Operating)		15	mA	$V_{DD} = V_{DD}$ max, $f_{CLK} = 8$ MHz
V_{OH} (Data)	Shift Register Output Voltage	10.5		V	$I_O = 100μA$
V_{OL} (Data)	Shift Register Output Voltage		1	V	$I_O = 100μA$
I_{IH}	Current Leakage, any input		1	μA	$V_{IN} = V_{DD}$
I_{IL}	Current Leakage, any input		-1	μA	$V_{IN} = 0$
V_{OC}	HV Output Clamp Diode Voltage		-1.5	V	$I_{OL} = -100mA$
V_{OH}	HV Output when Sourcing	52		V	$I_{OH} = -20mA$, -40 to 85°C
V_{OL}	HV Output when Sinking		8	V	$I_{OL} = 20mA$, -40 to 85°C
V_{OH}	HV Output when Sourcing	52		V	$I_{OH} = -15mA$, -55 to 125°C
V_{OL}	HV Output when Sinking		8	V	$I_{OL} = 15mA$, -55 to 125°C

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock Frequency		8	MHz	
t_{WL} or t_{WH}	Clock width, HIGH or LOW	62		ns	
t_{SU}	Setup time before CLK rises	25		ns	
t_H	Hold time after CLK rises	10		ns	
t_{DLH} (Data)	Data Output Delay after L to H CLK		110	ns	$C_L = 15pF$
t_{DHL} (Data)	Data Output Delay after H to L CLK		110	ns	$C_L = 15pF$
t_{DLE}	LE Delay after L to H CLK	50		ns	
t_{WLE}	Width of LE Pulse	50		ns	
t_{SLE}	LE Setup Time before L to H CLK	50		ns	
t_{ON}	Delay from LE to HV_{OUT}, L to H		500	ns	
t_{OFF}	Delay from LE to HV_{OUT}, H to L		500	ns	

Recommended Operating Conditions

(over -40 to 85°C for commercial temperature range and -55°C to 125°C for military)

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic Voltage Supply	10.8	13.2	V
V_{PP}	High Voltage Supply	8.0	80	V
V_{IH}	Input HIGH Voltage	V_{DD}-2	V_{DD}	V
V_{IL}	Input LOW Voltage	0	2	V
f_{CLK}	Clock Frequency	0	8	MHz

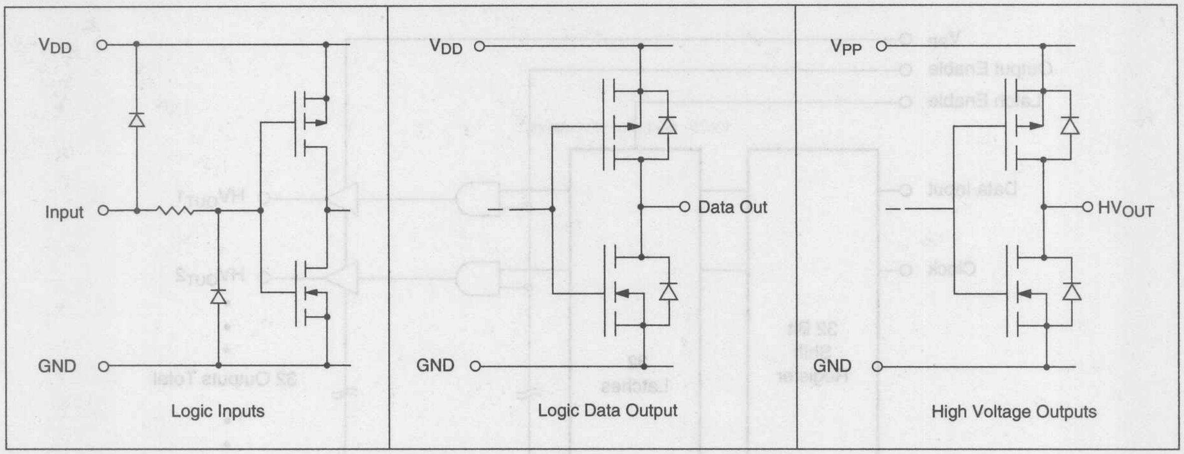
Note:

Power-up sequence should be the following:

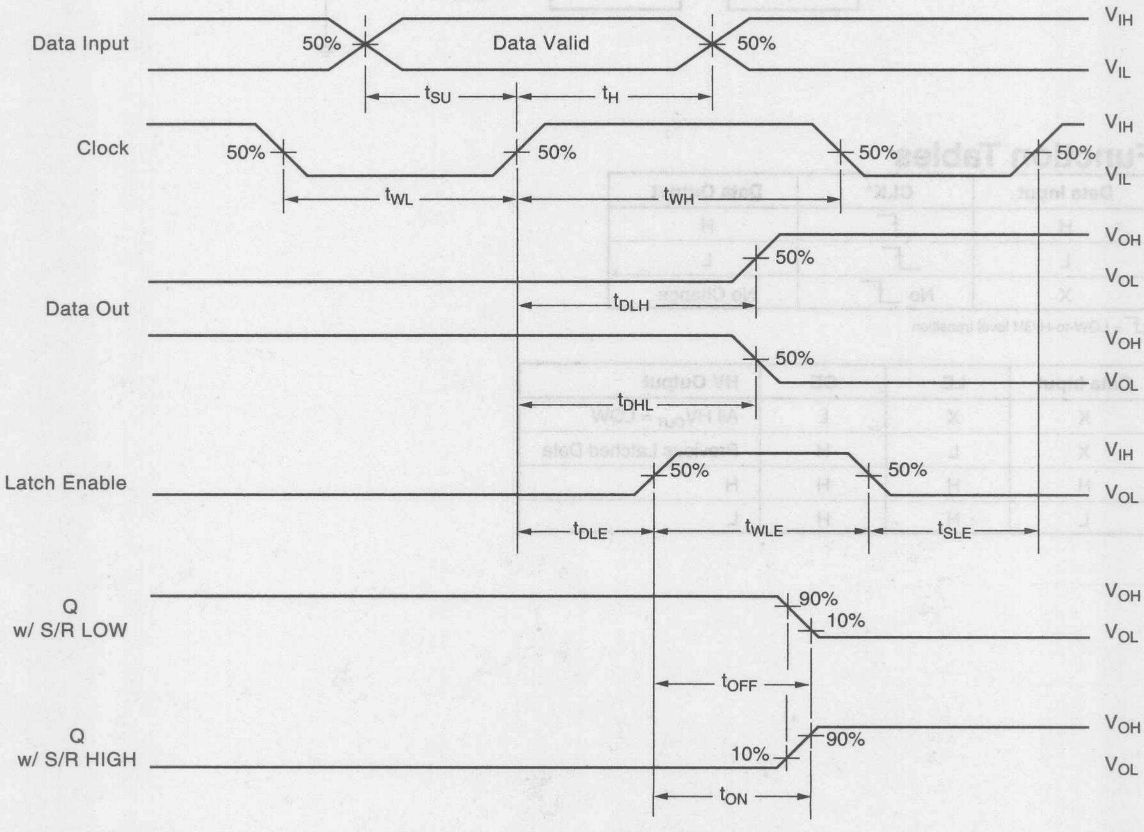
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

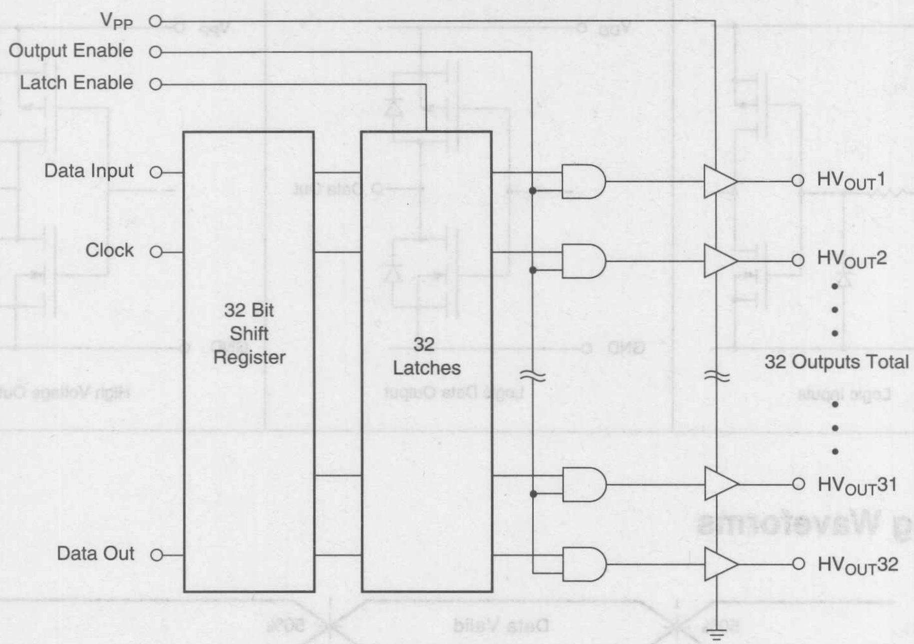
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Tables

Data Input	CLK*	Data Output
H	⌐	H
L	⌐	L
X	No ⌐	No Change

*⌐ = LOW-to-HIGH level transition

Data Input	LE	OE	HV Output
X	X	L	All HV_{OUT} = LOW
X	L	H	Previous Latched Data
H	H	H	H
L	H	H	L

Pin Configuration

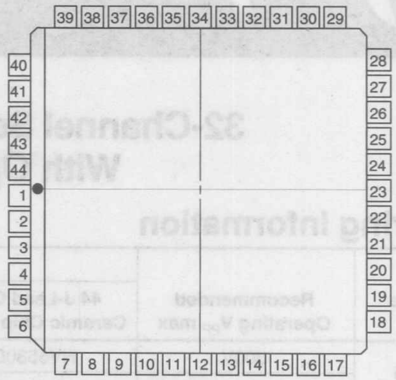
HV53
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Output Enable
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HV_{OUT} 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	N/C	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

HV54
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT}16	23	GND
2	HV_{OUT}17	24	V_{PP}
3	HV_{OUT}18	25	V_{DD}
4	HV_{OUT}19	26	Latch Enable
5	HV_{OUT}20	27	Data In
6	HV_{OUT}21	28	Output Enable
7	HV_{OUT}22	29	N/C
8	HV_{OUT}23	30	HV_{OUT}1
9	HV_{OUT}24	31	HV_{OUT}2
10	HV_{OUT}25	32	HV_{OUT}3
11	HV_{OUT}26	33	HV_{OUT}4
12	HV_{OUT}27	34	HV_{OUT}5
13	HV_{OUT}28	35	HV_{OUT}6
14	HV_{OUT}29	36	HV_{OUT}7
15	HV_{OUT}30	37	HV_{OUT}8
16	HV_{OUT}31	38	HV_{OUT}9
17	HV_{OUT}32	39	HV_{OUT}10
18	Data Out	40	HV_{OUT}11
19	N/C	41	HV_{OUT}12
20	N/C	42	HV_{OUT}13
21	N/C	43	HV_{OUT}14
22	Clock	44	HV_{OUT}15

Package Outline



top view

44-pin J-Lead Package

Supertex inc.

HV55
HV56

32-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options			
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	44 Lead Quad Plastic Gullwing	Dice
HV55	300V	HV5530DJ	HV5530PJ	HV5530PG	HV5530X
	220V	HV5522DJ	HV5522PJ	HV5522PG	HV5522X
HV56	300V	HV5630DJ	HV5630PJ	HV5630PG	HV5630X
	220V	HV5622DJ	HV5622PJ	HV5622PG	HV5622X

* For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- Processed with HVCMOS® technology
- Sink current minimum 100mA
- Shift register speed 8MHz
- Polarity and Blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to V_{PP} allows efficient power recovery
- 44-lead ceramic surface mount package
- Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +15V
Output voltage, V_{PP}[1]	HV5530/HV5630	-0.5V to +315V
	HV5522/HV5622	-0.5V to +220V
Logic input levels[1]		-0.5V to V_{DD} + 0.5V
Ground currrent[2]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Ceramic	-40°C to +85°C
	Plastic	0°C to +70°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV55 and HV56 are low-voltage serial to high-voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV55 shifts in the counterclockwise direction when viewed from the top of the package, and the HV56 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	f_{CLK} = 8MHz F_{DATA} = 4MHz
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	V_{IN} = 0V
$I_{O(OFF)}$	Off state output current			10	µA	All outputs high All SWS parallel
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} - 1.0V		V	I_{Dout} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}		15.0	V	I_{HVout} = +100mA
		Data out		1.0	V	I_{Dout} = +100µA
V_{OC}	HV_{OUT} clamp voltage			-1.5	V	I_{OL} = -100mA

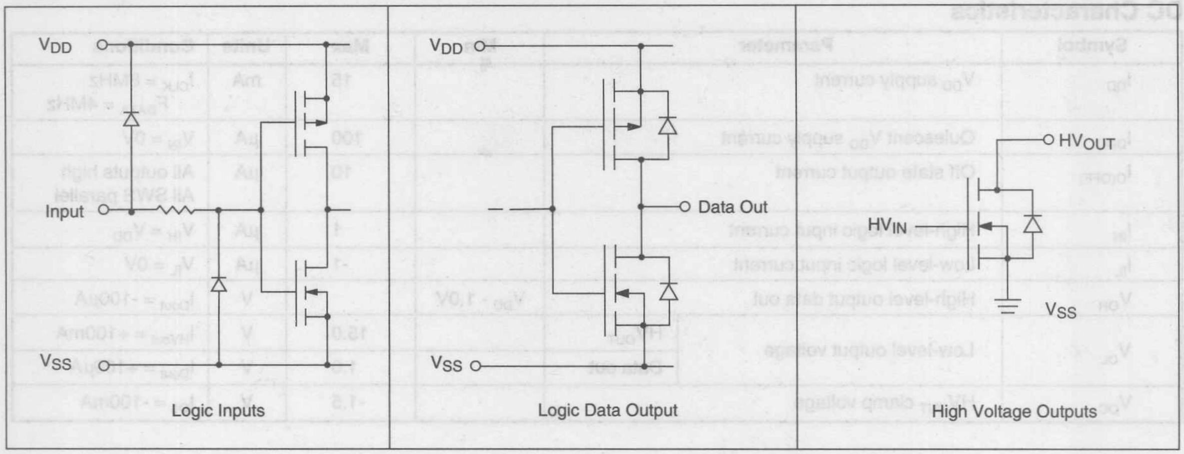
AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock falls	25		ns	
t_H	Data hold time after clock falls	10		ns	
t_{ON}	Turn on time, HV_{OUT} from enable		500	ns	R_L = 2KΩ to V_{PP} MAX
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

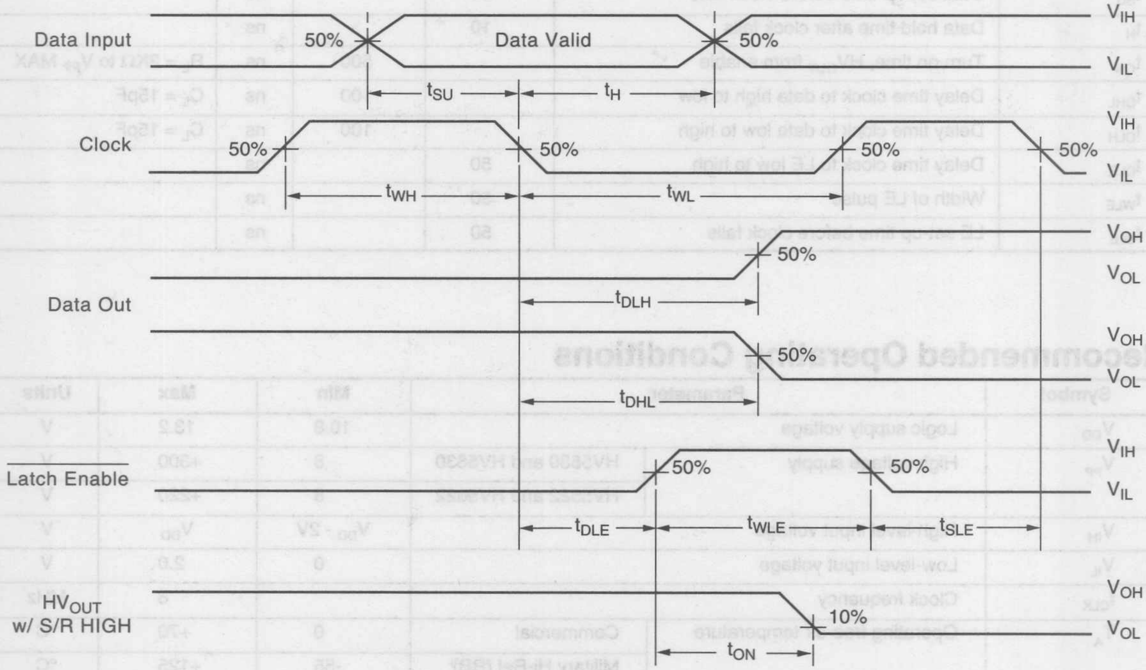
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply	HV5530 and HV5630	8	+300	V
		HV5522 and HV5622	8	+220	V
V_{IH}	High-level input voltage		V_{DD} - 2V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C

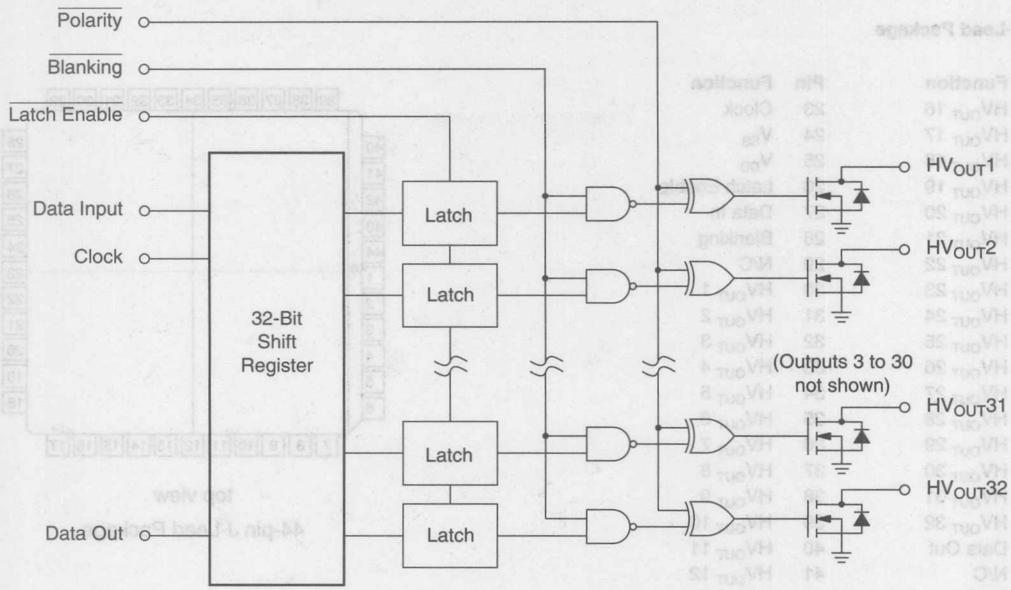
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out *
All on	X	X	X	L	L	*	*…*	On	On…On	*
All off	X	X	X	L	H	*	*…*	Off	Off…Off	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*…*	*	*…*	*
Load Latches	X	H or L	↑	H	H	*	*…*	*	*…*	*
	X	H or L	↑	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Transparent Latch mode	L	↓	H	H	H	L	*…*	Off	*…*	*
	H	↓	H	H	H	H	*…*	On	*…*	*

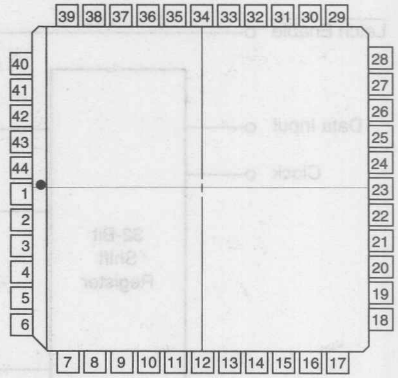
Notes:
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
* = dependent on previous stage's state before the last CLK ↓ or last LE high.

Pin Configurations

HV55
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	Clock
2	HV_{OUT} 17	24	V_{SS}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Blanking
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	N/C	43	HV_{OUT} 14
22	Polarity	44	HV_{OUT} 15

Package Outline



top view

44-pin J-Lead Package

HV56
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	Clock
2	HV_{OUT} 16	24	V_{SS}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Blanking
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HV_{OUT} 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	N/C	43	HV_{OUT} 19
22	Polarity	44	HV_{OUT} 18

Pin Configurations

HV55

44-Pin Quad Plastic Gullwing Package

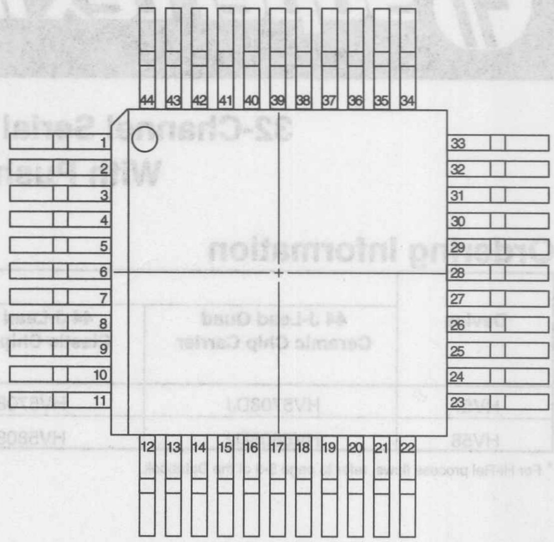
Pin	Function	Pin	Function
1	HV_{OUT} 11	23	Data Out
2	HV_{OUT} 12	24	N/C
3	HV_{OUT} 13	25	N/C
4	HV_{OUT} 14	26	N/C
5	HV_{OUT} 15	27	Polarity
6	HV_{OUT} 16	28	Clock
7	HV_{OUT} 17	29	V_{SS}
8	HV_{OUT} 18	30	V_{DD}
9	HV_{OUT} 19	31	Latch Enable
10	HV_{OUT} 20	32	Data In
11	HV_{OUT} 21	33	Blanking
12	HV_{OUT} 22	34	N/C
13	HV_{OUT} 23	35	HV_{OUT} 1
14	HV_{OUT} 24	36	HV_{OUT} 2
15	HV_{OUT} 25	37	HV_{OUT} 3
16	HV_{OUT} 26	38	HV_{OUT} 4
17	HV_{OUT} 27	39	HV_{OUT} 5
18	HV_{OUT} 28	40	HV_{OUT} 6
19	HV_{OUT} 29	41	HV_{OUT} 7
20	HV_{OUT} 30	42	HV_{OUT} 8
21	HV_{OUT} 31	43	HV_{OUT} 9
22	HV_{OUT} 32	44	HV_{OUT} 10

HV56

44-Pin Quad Plastic Gullwing Package

Pin	Function	Pin	Function
1	HV_{OUT} 22	23	Data Out
2	HV_{OUT} 21	24	N/C
3	HV_{OUT} 20	25	N/C
4	HV_{OUT} 19	26	N/C
5	HV_{OUT} 18	27	Polarity
6	HV_{OUT} 17	28	Clock
7	HV_{OUT} 16	29	V_{SS}
8	HV_{OUT} 15	30	V_{DD}
9	HV_{OUT} 14	31	Latch Enable
10	HV_{OUT} 13	32	Data In
11	HV_{OUT} 12	33	Blanking
12	HV_{OUT} 11	34	N/C
13	HV_{OUT} 10	35	HV_{OUT} 32
14	HV_{OUT} 9	36	HV_{OUT} 31
15	HV_{OUT} 8	37	HV_{OUT} 30
16	HV_{OUT} 7	38	HV_{OUT} 29
17	HV_{OUT} 6	39	HV_{OUT} 28
18	HV_{OUT} 5	40	HV_{OUT} 27
19	HV_{OUT} 4	41	HV_{OUT} 26
20	HV_{OUT} 3	42	HV_{OUT} 25
21	HV_{OUT} 2	43	HV_{OUT} 24
22	HV_{OUT} 1	44	HV_{OUT} 23

Package Outline



top view

44-pin Quad Plastic Gullwing Package

Supertex inc.

HV57
HV58

32-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	**44 J-Lead Quad Plastic Chip Carrier**	**Die in waffle pack**	**44 J-Lead Quad Ceramic Chip Carrier** (MIL-STD-883 Processed*)
HV57	HV5708DJ	HV5708PJ	HV5708X	RBHV5708DJ
HV58	HV5808DJ	HV5808PJ	HV5808X	RBHV5808DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery
- ☐ CMOS compatible inputs

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +15V
Output voltage, V_{PP}		-0.5V to +80V
Logic input levels[2]		-0.5V to V_{DD} +0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV57 and HV58 are low-voltage serial to high-voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays. The inputs are fully CMOS compatible.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV57 shifts data in the clockwise direction when viewed from the top of the package and the HV58 shifts in the counterclockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max $f_{CLK} = 8MHz$
I_{PP}	High voltage supply current			0.5	mA	Outputs high
				0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	HV_{OUT}	52		V	I_O= -20mA(-15mA*)
		Data out	10.5		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		8	V	I_O= 20mA(15mA*)
		Data out		1	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	$V_{IL} = 0V$

* Over Military temperature range

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	10		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	50		ns	

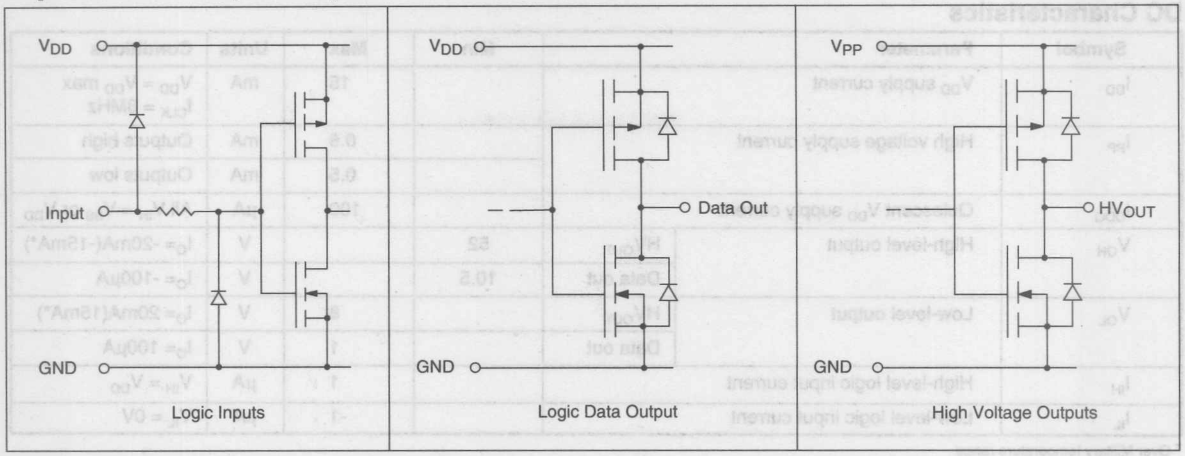
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	Output high voltage		8.0	75	V
V_{IH}	High-level input voltage		V_{DD} - 2V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8.0	MHz
T_A	Operating free-air temperature	Commercial	-4.0	+85	°C
		Military Hi-Rel (RB)	-55	+125	°C

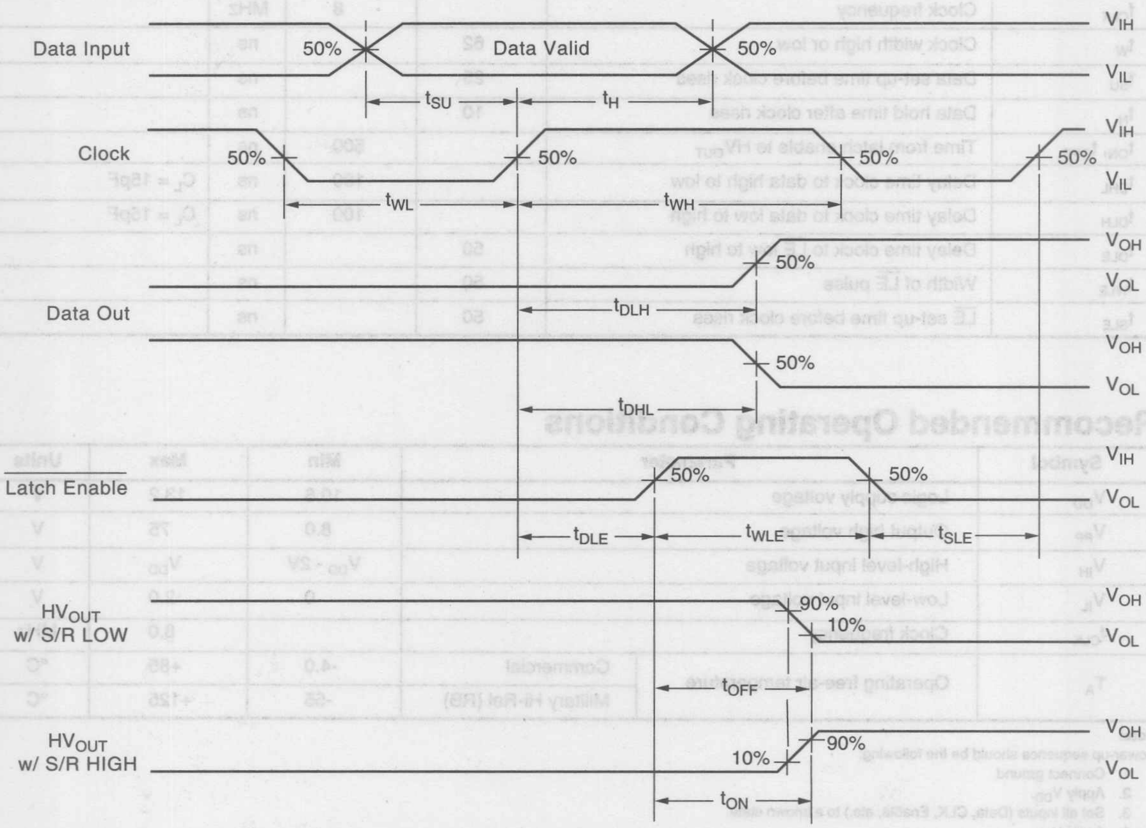
Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

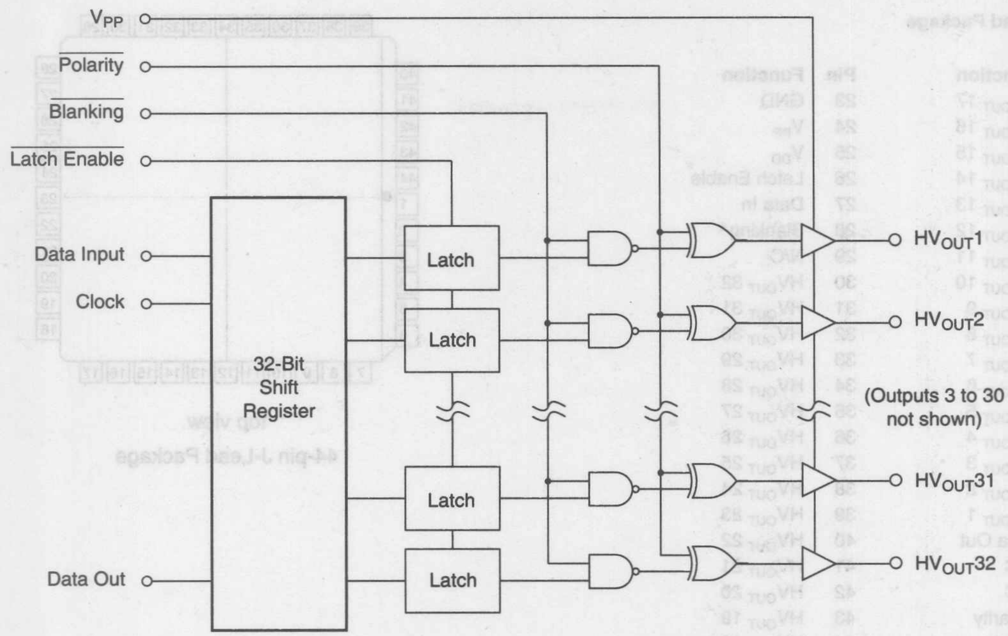
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out *
All on	X	X	X	L	L	*	*…*	H	H…H	*
All off	X	X	X	L	H	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*…*	*	*…*	*
Load latches	X	H or L	↑	H	H	*	*…*	*	*…*	*
	X	H or L	↑	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Transparent latch mode	L	↑	H	H	H	L	*…*	L	*…*	*
	H	↑	H	H	H	H	*…*	H	*…*	*

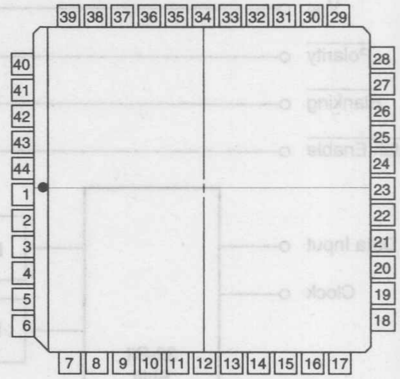
Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high,

Pin Configurations

HV57
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Blanking
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HV_{OUT} 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	Polarity	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

Package Outline



top view

44-pin J-Lead Package

HV58
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Blanking
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	Polarity	43	HVout 14
22	Clock	44	HVout 15

HV500

Supertex inc.

32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options						
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die	40-Pin Ceramic Dip (MIL-STD-883 Processed*)	44-Pin J-Lead Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV500	HV500D	HV500P	HV500DJ	HV500PJ	HV500X	RBHV500D	RBHV500DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS® Technology
- Output voltage of up to 100V
- CMOS push-pull output buffers
- Low-power level shifting
- Source/sink current minimum of 15mA
- Shift register speed 8MHz
- CMOS compatible inputs
- Output clamp diodes to V_{PP} and GND
- Direct replacement for the SN75500 and SN55500 series devices
- 44-lead plastic and ceramic surface mount packages available
- Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +15V
Supply voltage, V_{PP}[1]		-0.3V to +100V
Logic input levels[1]		-0.3V to V_{DD} + 0.3V
Ground currrent[2]		1.2A[3]
Continuous total power dissipation[4]	Ceramic Plastic	1850mW 1200mW
Operating temperature range	Commercial Military	-40°C to +85°C -55°C to 125°C
Storage temperature range		-65°C to +150°C

Notes:

1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. Consult factory for availability of 8.0A ground current version.
4. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

General Description

The HV500 is a monolithic low-voltage logic to high-voltage output 32-channel driver for AC plasma flat panel displays. It is manufactured using the HVCMOS process, providing the high output voltages and currents possible with DMOS structures and the low power dissipation of CMOS logic.

The HV500 is comprised of an 8-stage DMOS shift register, four groups of eight high-voltage output buffers, and logic to select which group of outputs will reflect the status of the data in the shift register and strobe functions. When the strobe input is high, all outputs are held low independent of any other logic input. When strobe is brought low, the group of outputs selected by the state of the select inputs reflects the data in the shift register, and all non-selected outputs are held low.

The high-voltage output buffers have level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	$I_{OH} = -1mA$[1]
			90		V	$I_{OH} = -15mA$[1]
		Serial out	9		V	$I_{OH} = -100µA$[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	$I_{OL} = 1mA$
				5	V	$I_{OL} = 15mA$
		Serial out		1	V	$I_{OL} = 100µA$[2]
V_{OK}	High voltage output			2.5	V	$I_{OK} = 20mA$[3]
	Clamp voltage			-2.5	V	$I_{OK} = -20mA$

Notes:
1. $V_{PP} = 100V$
2. $V_{DD} = 10.8V$
3. $V_{PP} = 0V$

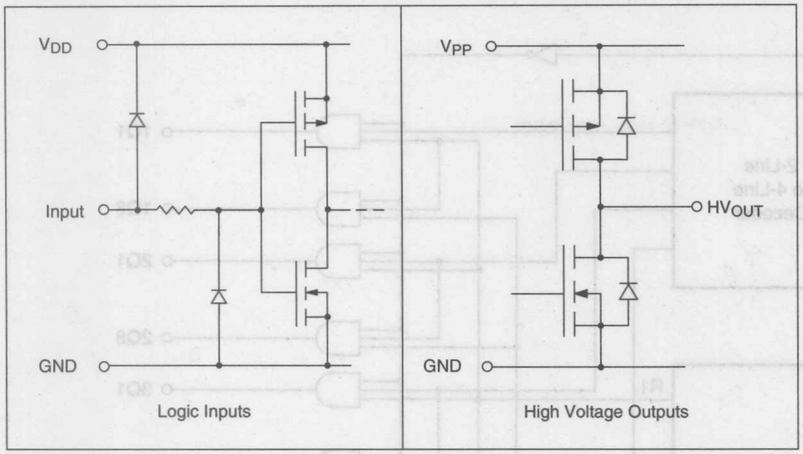
AC Characteristics ($V_{DD} = 12V$, $V_{PP} = 100V$, $T_C = 25°C$)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{DHL}	Delay time strobe to HV_{out} high to low			250	ns	$C_L = 30pF$
t_{DLH}	Delay time strobe to HV_{out} low to high			250	ns	$C_L = 30pF$
t_{SU}	Set-up time	Data in to clock ↑	20		ns	
		Select before strobe ↓	50		ns	
t_H	Hold time	Data after clock ↑	50		ns	
		Strobe high after clock ↑	50		ns	
		Select after strobe ↑	50		ns	
t_R	Rise time low to high HV_{out}			300	ns	$C_L = 30pF$
t_F	Fall time high to low HV_{out}			200	ns	$C_L = 30pF$

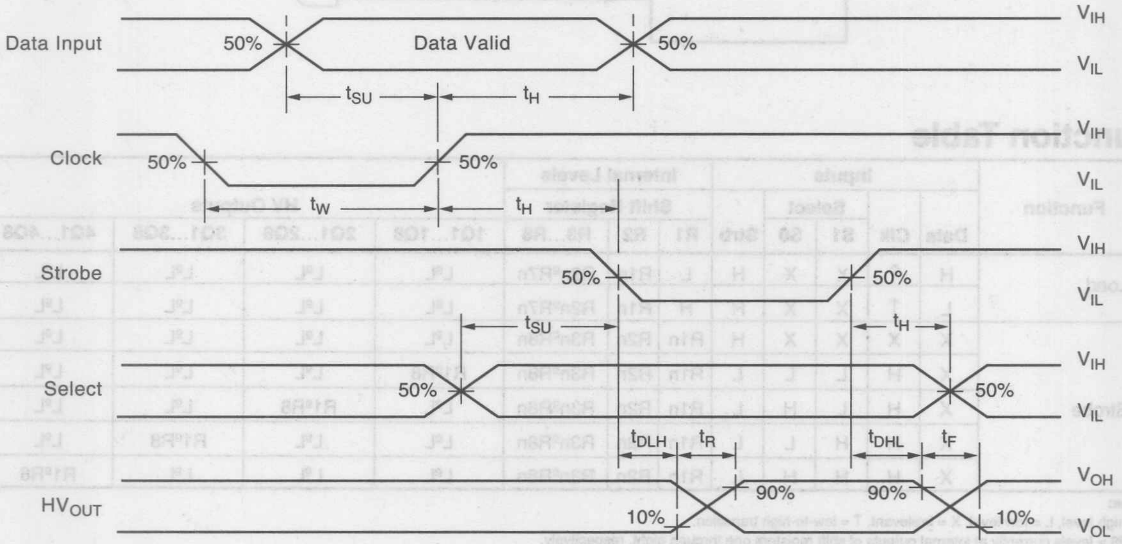
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		0	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+85	°C
		Military Hi-Rel (RB)	-55	+125	°C

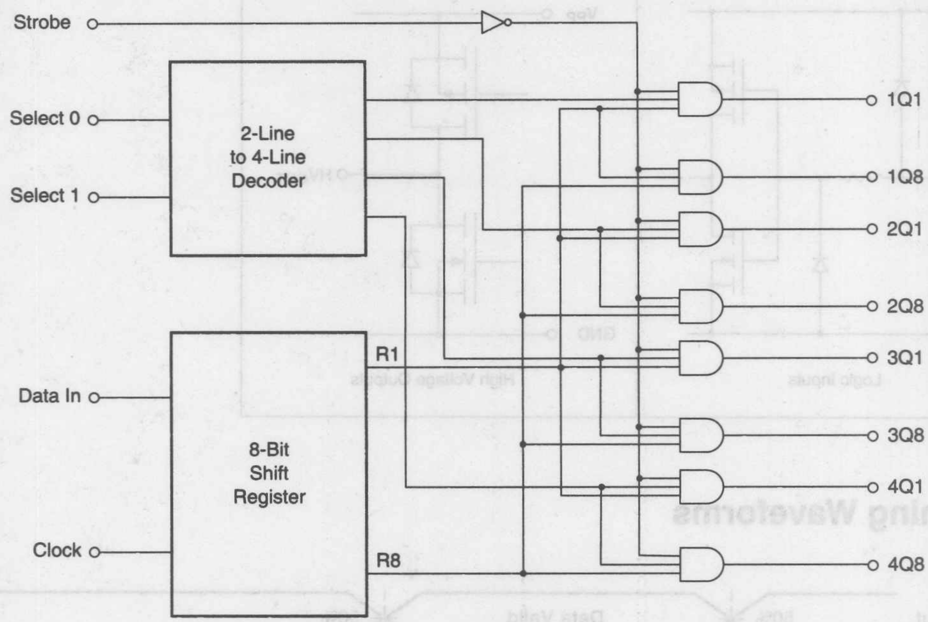
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Internal Levels			HV Outputs			
			Select			Shift Register						
	Data	Clk	S1	S0	Strb	R1	R2	R3…R8	1Q1…1Q8	2Q1…2Q8	3Q1…3Q8	4Q1…4Q8
Load	H	↑	X	X	H	L	R1n	R2nºR7n	LºL	LºL	LºL	LºL
	L	↑	X	X	H	H	R1n	R2nºR7n	LºL	LºL	LºL	LºL
Strobe	X	X	X	X	H	R1n	R2n	R3nºR8n	LºL	LºL	LºL	LºL
	X	H	L	L	L	R1n	R2n	R3nºR8n	R1ºR8	LºL	LºL	LºL
	X	H	L	H	L	R1n	R2n	R3nºR8n	LºL	R1ºR8	LºL	LºL
	X	H	H	L	L	R1n	R2n	R3nºR8n	LºL	LºL	R1ºR8	LºL
	X	H	H	H	L	R1n	R2n	R3nºR8n	LºL	LºL	LºL	R1ºR8

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1ºR8 = levels currently at internal outputs of shift registers one through eight, respectively.
R1nºR8n = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

Pin Configurations

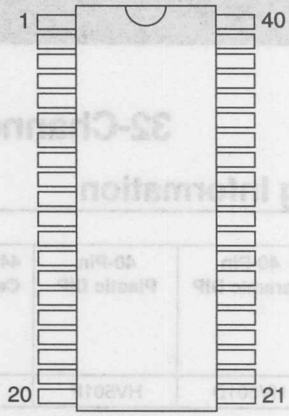
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Select 0	21	V_{PP}
2	Data In	22	3Q8
3	Clock	23	3Q7
4	1Q1	24	3Q6
5	1Q2	25	3Q5
6	1Q3	26	3Q4
7	1Q4	27	3Q3
8	1Q5	28	3Q2
9	1Q6	29	3Q1
10	1Q7	30	4Q8
11	1Q8	31	4Q7
12	2Q1	32	4Q6
13	2Q2	33	4Q5
14	2Q3	34	4Q4
15	2Q4	35	4Q3
16	2Q5	36	4Q2
17	2Q6	37	4Q1
18	2Q7	38	Strobe
19	2Q8	39	Select 1
20	GND	40	V_{DD}

44 Pin J-Lead

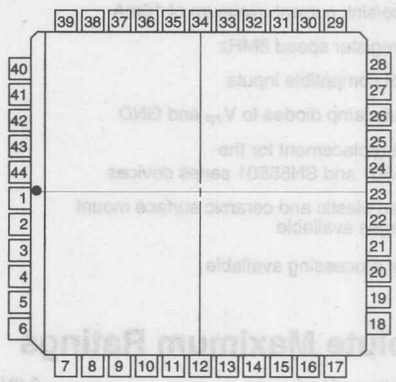
Pin	Function	Pin	Function
1	N/C	23	N/C
2	Select 0	24	V_{PP}
3	Data In	25	3Q8
4	Clock	26	3Q7
5	N/C	27	3Q6
6	1Q1	28	3Q5
7	1Q2	29	3Q4
8	1Q3	30	3Q3
9	1Q4	31	3Q2
10	1Q5	32	3Q1
11	1Q6	33	4Q8
12	1Q7	34	4Q7
13	1Q8	35	4Q6
14	2Q1	36	4Q5
15	2Q2	37	4Q4
16	2Q3	38	4Q3
17	2Q4	39	4Q2
18	2Q5	40	4Q1
19	2Q6	41	N/C
20	2Q7	42	Strobe
21	2Q8	43	Select 1
22	GND	44	V_{DD}

Package Outlines



top view

40-pin DIP



top view

44-pin J-Lead Package

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Supertex inc.

32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options						
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die	40-Pin Ceramic Dip (MIL-STD-883 Processed*)	44-Pin J-Lead Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV501	HV501D	HV501P	HV501DJ	HV501PJ	HV501X	RBHV501D	RBHV501DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ Processed with HVCMOS® Technology
- ☐ Output voltage of up to 100V
- ☐ DMOS push-pull output buffers
- ☐ Low-power level shifting
- ☐ Source/sink current minimum of 15mA
- ☐ Shift register speed 8MHz
- ☐ CMOS compatible inputs
- ☐ Output clamp diodes to V_{PP} and GND
- ☐ Direct replacement for the SN75501 and SN55501 series devices
- ☐ 44-lead plastic and ceramic surface mount packages available
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +15V
Supply voltage, V_{PP}[1]		-0.3V to +100V
Logic input levels[1]		-0.3V to V_{DD} + 0.3V
Ground currrent[2]		1.5A[3]
Continuous total power dissipation[4]	Ceramic	1850mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to 125°C
Storage temperature range		-65°C to +150°C

Notes:

1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. Consult factory for availability of 8.0A ground current version.
4. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

General Description

The HV501 is a 32-channel low-voltage serial to high-voltage parallel converter designed for use in matrix-addressable display applications. It is manufactured with the HVCMOS technology for enhanced ruggedness and performance. This device is a direct replacement for the SN75501 family of devices.

These devices are comprised of a 32-bit shift register with a serial data out, strobe and sustain control logic, and level shifters with high-voltage DMOS output buffers. When the strobe and sustain outputs are held high the outputs are held high. Data can then be clocked into the shift register without changing the state of the outputs. When the strobe input is brought low with the sustain input remaining high, the outputs will change state to reflect the status of the data in each output's corresponding shift register bit. A logic "1" in the shift register will cause the corresponding output to pull up to V_{PP}, and a logic "0" will cause the output to pull to GND. The sustain input is used to bring all the outputs low. When the sustain input is low, all outputs are low, independent of any other control input.

The high-voltage output buffers have low power level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	$I_{OH} = -1mA$[1]
			90		V	$I_{OH} = -15mA$[1]
		Data out	9		V	$I_{OH} = -100µA$[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	$I_{OL} = 1mA$
				5	V	$I_{OL} = 15mA$
		Data out		1	V	$I_{OL} = 100µA$[2]
V_{OK}	High voltage output			2.5	V	$I_{OK} = 20mA$[3]
	Clamp voltage			-2.5	V	$I_{OK} = -20mA$[3]

Notes:
1. $V_{PP} = 100V$
2. $V_{DD} = 10.8V$
3. $V_{PP} = 0V$

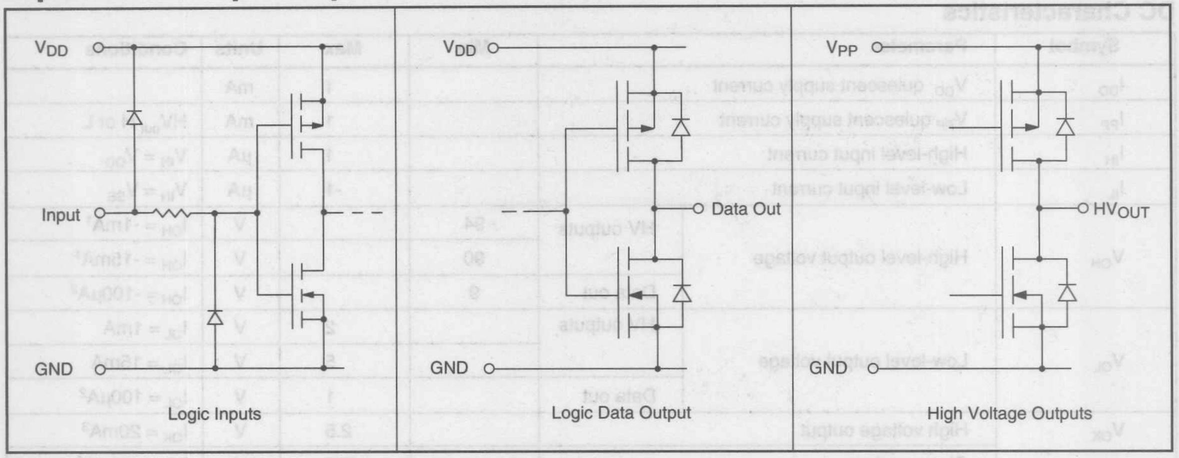
AC Characteristics ($V_{DD} = 12V$, $V_{PP} = 80V$)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{SU}	Data input set-up time before CLK		20		ns	
t_H	Data input hold time after CLK		50		ns	
t_{DHL}	Delay time High to low Level outputs	Strobe to HV_{OUT}		250	ns	$C_L = 30pF$
		Sustain to HV_{OUT}		250	ns	$C_L = 30pF$
		Serial out		147	ns	$C_L = 30pF$
t_{DLH}	Delay time Low to high Level outputs	Strobe to HV_{OUT}		450	ns	$C_L = 30pF$
		Sustain to HV_{OUT}		450	ns	$C_L = 30pF$
		Serial out		147	ns	$C_L = 30pF$
t_R	Rise time low to high HV_{OUT}			300	ns	$C_L = 30pF$
t_F	Fall time high to low HV_{OUT}			200	ns	$C_L = 30pF$

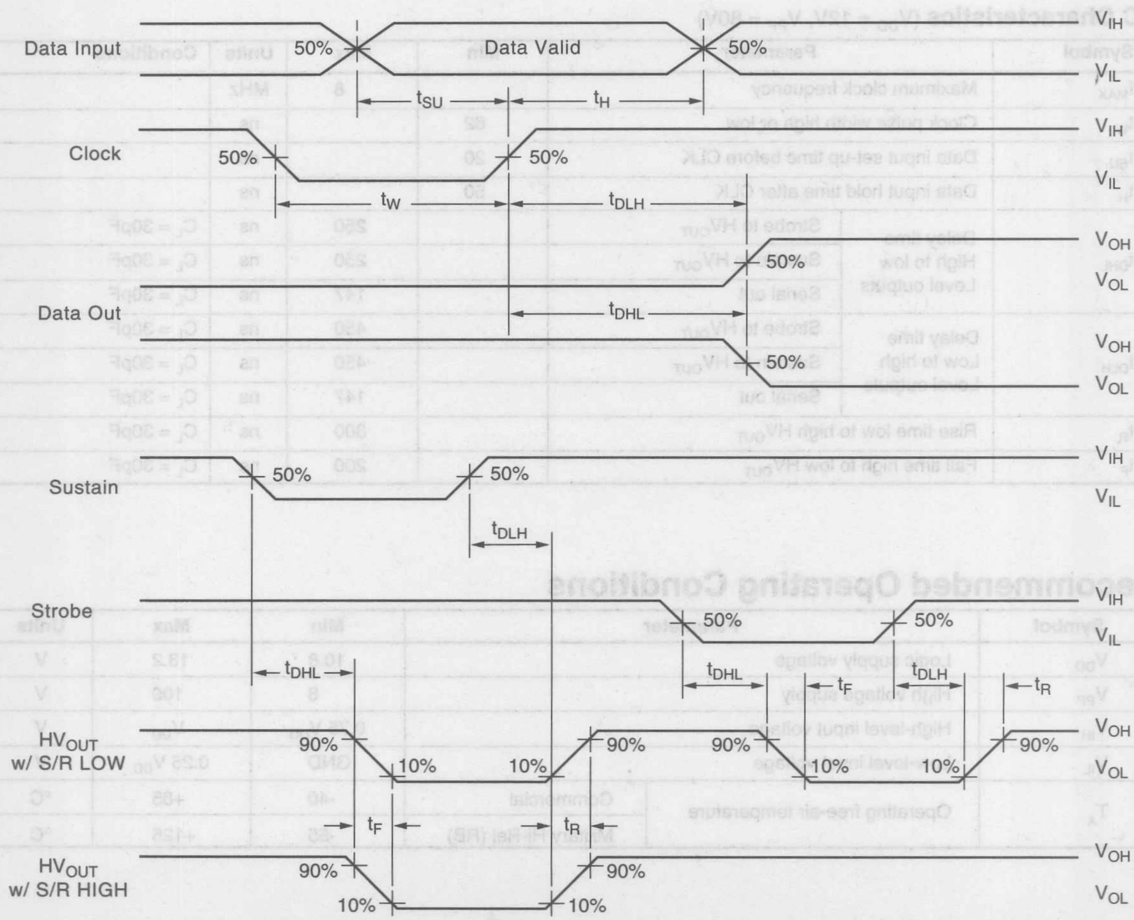
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		8	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+85	°C
		Military Hi-Rel (RB)	-55	+125	°C

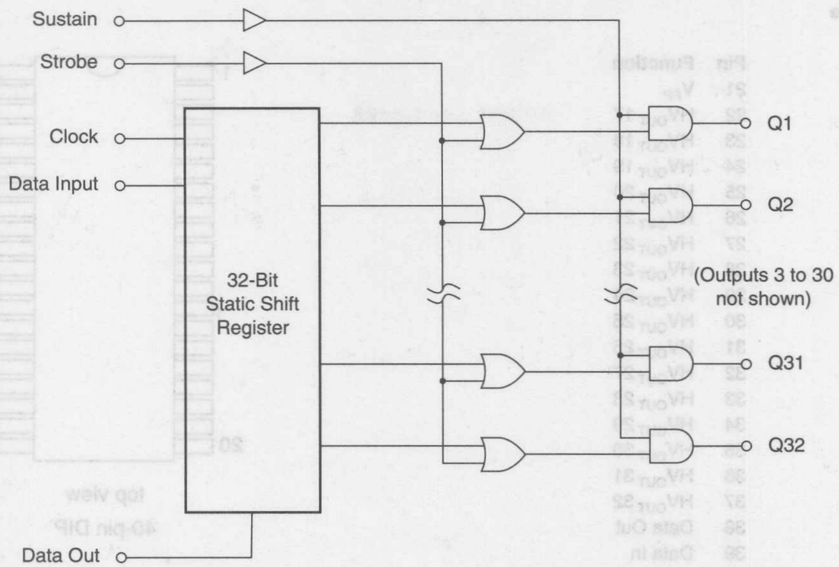
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs				Shift Register			HV Outputs		
	Data	Clock	Strobe	Sustain	R1	R2	R3…R32	1	2	3…32
Load	H	↑	H	H	H	R1n	R2n…R31n	H	H	H…H
	L	↑	H	H	L	R1n	R2n…R31n	H	H	H…H
Strobe	X	X	H	H	R1n	R2n	R3n…R32n	H	H	H…H
	X	H	L	H	R1n	R2n	R3n…R32n	R1	R2	R3…R32
Sustain	X	X	X	L	R1n	R2n	R3n…R32n	L	L	L…L

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1…R32 = levels currently at internal outputs of shift registers one through 32, respectively.
R1n…R32n = levels at shift-register outputs R1 through R32, respectively, before the most recent ↑ transition of the clock input.

Pin Configurations

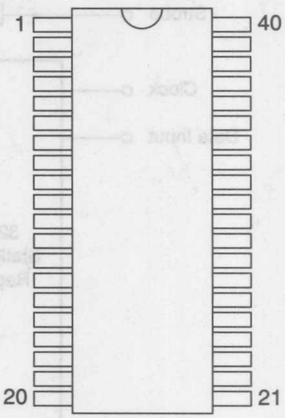
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Clock	21	V_{PP}
2	Sustain	22	HV_{OUT} 17
3	Strobe	23	HV_{OUT} 18
4	HV_{OUT} 1	24	HV_{OUT} 19
5	HV_{OUT} 2	25	HV_{OUT} 20
6	HV_{OUT} 3	26	HV_{OUT} 21
7	HV_{OUT} 4	27	HV_{OUT} 22
8	HV_{OUT} 5	28	HV_{OUT} 23
9	HV_{OUT} 6	29	HV_{OUT} 24
10	HV_{OUT} 7	30	HV_{OUT} 25
11	HV_{OUT} 8	31	HV_{OUT} 26
12	HV_{OUT} 9	32	HV_{OUT} 27
13	HV_{OUT} 10	33	HV_{OUT} 28
14	HV_{OUT} 11	34	HV_{OUT} 29
15	HV_{OUT} 12	35	HV_{OUT} 30
16	HV_{OUT} 13	36	HV_{OUT} 31
17	HV_{OUT} 14	37	HV_{OUT} 32
18	HV_{OUT} 15	38	Data Out
19	HV_{OUT} 16	39	Data In
20	GND	40	V_{DD}

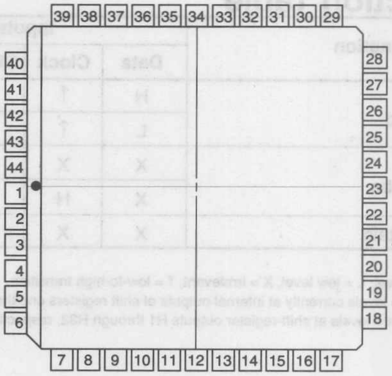
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	N/C	23	N/C
2	Clock	24	V_{PP}
3	Sustain	25	HV_{OUT} 17
4	Strobe	26	HV_{OUT} 18
5	N/C	27	HV_{OUT} 19
6	HV_{OUT} 1	28	HV_{OUT} 20
7	HV_{OUT} 2	29	HV_{OUT} 21
8	HV_{OUT} 3	30	HV_{OUT} 22
9	HV_{OUT} 4	31	HV_{OUT} 23
10	HV_{OUT} 5	32	HV_{OUT} 24
11	HV_{OUT} 6	33	HV_{OUT} 25
12	HV_{OUT} 7	34	HV_{OUT} 26
13	HV_{OUT} 8	35	HV_{OUT} 27
14	HV_{OUT} 9	36	HV_{OUT} 28
15	HV_{OUT} 10	37	HV_{OUT} 29
16	HV_{OUT} 11	38	HV_{OUT} 30
17	HV_{OUT} 12	39	HV_{OUT} 31
18	HV_{OUT} 13	40	HV_{OUT} 32
19	HV_{OUT} 14	41	N/C
20	HV_{OUT} 15	42	Data Out
21	HV_{OUT} 16	43	Data In
22	GND	44	V_{DD}

Package Outlines



top view
40-pin DIP



top view
44-pin J-Lead Package

Supertex inc.

32-Channel Vacuum-Fluorescent Display Driver

Ordering Information

Device	Package Options	
	40 Pin Dual-In-Line	44 Pin J-lead
HV518	HV518P	HV518PJ

Features

- ☐ 32 output lines
- ☐ 90V output swing
- ☐ Active pull-down
- ☐ Latches on all outputs
- ☐ Up to 6MHz @ V_{DD} = 5V
- ☐ -40°C to +85°C operation

General Description

The HV518 is designed for vacuum fluorescent or DC plasma applications, where it can serve as a segment, digit or matrix display driver. Each device has 32 outputs, 32 latches and a 32 bit cascadable shift register.

Serial data enters the shift register on the LOW-to-HIGH transition of the clock input. With latch enable (LE) HIGH, parallel data is transferred to the output buffers through a 32-bit latch. When LE is low the data is stored in the latch. When STROBE is LOW, all outputs are enabled; if STROBE is HIGH, all outputs are LOW.

Absolute Maximum Ratings

Supply voltage, V_{DD} [1]		-0.5V to +6.0V
Supply voltage, V_{PP} [1]		-0.5V to +90V
Logic input levels		-0.5V to V_{DD} +0.5V
Continuous total power dissipation [2,3]	Plastic	1200mW
Operating temperature range		-40°C to +85°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly at 13.2mW/°C for the dual-in-line package and 13.6mW/°C for the flat package.

Electrical Characteristics

(over recommended ranges of operating free-air temperature and V_{DD}. Unless otherwise noted, V_{PP} = 80V)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	Supply current				10	mA	V_{DD} = 5V, f_{CH} = 6.0 MHz
I_{PP}	Supply current				12	mA	Output high, T_A = -40°C
				7	10	mA	Output high, T_A = 0 to +85°C
					500	µA	Outputs low
V_{OH}	High-level output voltage	HVoutput	70.0			V	I_{OH}= -25mA
		Serial output	4.5	4.9	5	V	V_{DD} = 5V, I_{OH} = -20µA
V_{OL}	Low-level output	HVoutput			5	V	I_{OL}= 1mA
		Serial output		0.06	0.8	V	I_{OL} =20µA
I_{IH}	High-level logic input current			0.1	1	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current			-0.1	-1	µA	V_{IL} = 0V

Note: The total number of ON outputs times the duty cycle must not exceed the allowable package power dispation.

Switching Characteristics (V_{PP} = 80V, C_L = 50 pF, T_A = 25°C, unless otherwise noted)

Symbol	Parameter			Min	Max	Unit	Conditions
t_d	Delay time, Clock to data output		V_{DD} = 4.5V		600	ns	CL =15 pF See Figure 4
t_{DHL}	Delay time, high-to-low-level,	from latch enable	V_{DD} = 4.5V		1.5	µs	See Figure 5
	HVoutput	from strobe			1		See Figure 6
t_{DLH}	Delay time, low-to-high-level	from latch enable	V_{DD} = 4.5V		1.5	µs	See Figure 5
	HVoutput	from strobe			1		See Figure 6
t_{THL}	Transition time, high-to-low-level, HVoutput		V_{DD} = 4.5V		3	µs	See Figure 6
t_{TLH}	Transition time, low-to-high-level, HVoutput		V_{DD} = 4.5V		2.5	µs	See Figure 6

Recommended Operating Conditions (T_A = 25°C, unless otherwise noted)

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic voltage supply		4.5	5.5	V
V_{PP}	High voltage supply		8	80	V
V_{IH}	High-level input voltage (See Fig.1.)	V_{DD} = 4.5V	3.5		V
V_{IL}	Low-level input voltage (See Fig. 1.)	V_{DD} = 4.5V		1	V
I_{OH}	High-level output current		-25		mA
I_{OL}	Low-level output current			2	mA
f_{CLK}	Clock frequency (see Figure 2)	V_{DD} = 4.5V		6.0	MHz
$t_{w(CKH)}$	Pulse duration , clock high	V_{DD} = 4.5V	83		ns
$t_{w(CKL)}$	Pulse duration , clock low	V_{DD} = 4.5V	83		ns
t_{su}	Setup time, data before clock	V_{DD} = 4.5V	75		ns
t_h	Hold time, data after clock	V_{DD} = 4.5V	75		ns
T_A	Operating free-air temperature		-40	85	°C

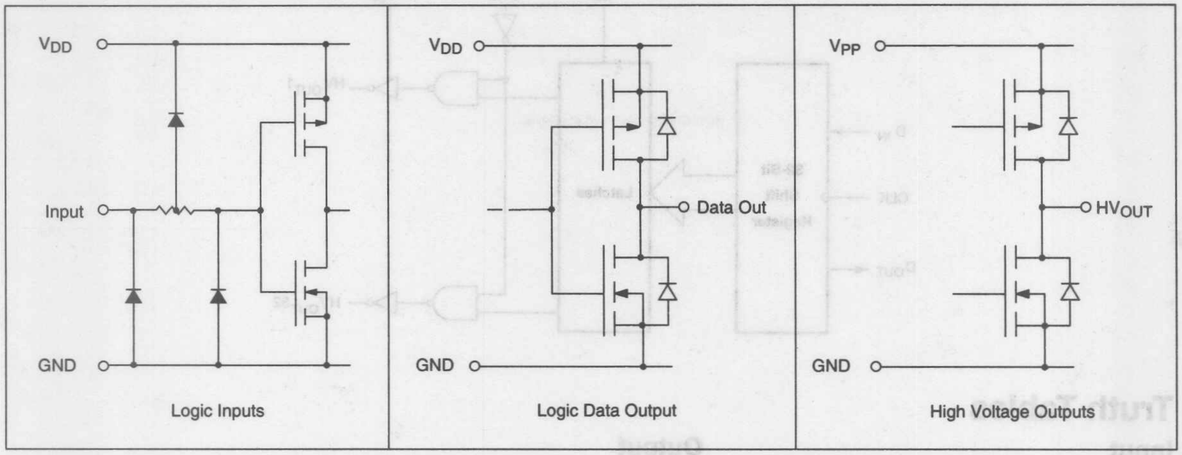
Note:

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply $_{VPP}$.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



Parameter Measurement Information

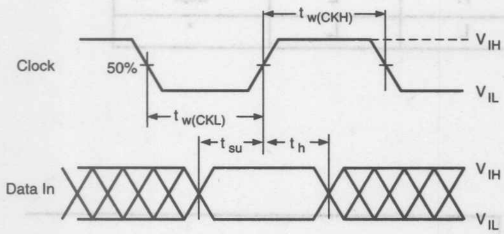


Figure 3: Input Timing Voltage Waveforms

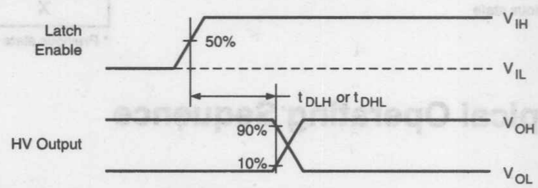


Figure 5

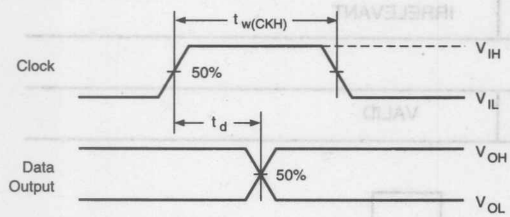


Figure 4

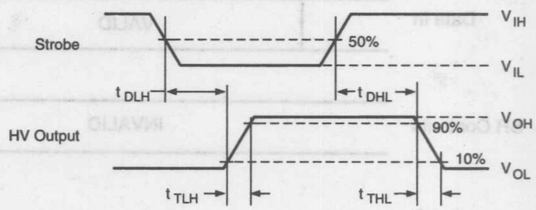
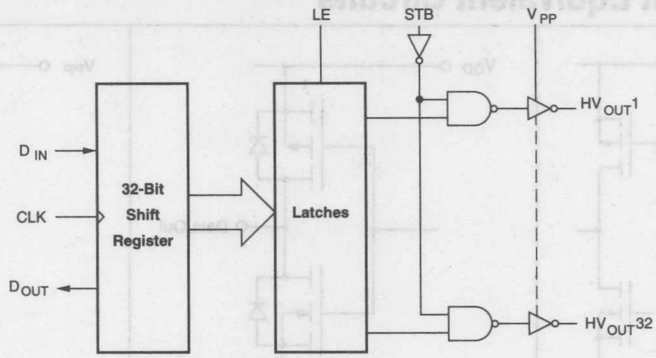


Figure 6: Switching-Time Voltage Waveforms

Note: For testing purposes, all input pulses have maximum rise and fall times of 30 nsec.

Logic Diagram



Truth Tables

Input

Data In	CLK	Data Out
H		H
L		L
X	No Change	*

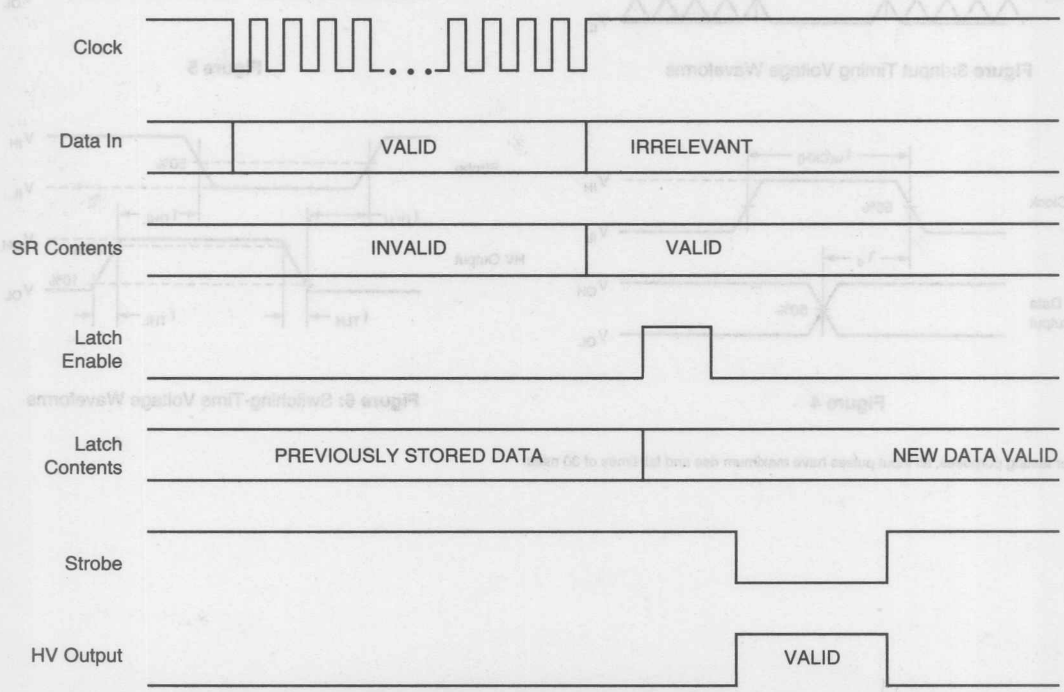
* Previous state

Output

Data In	LE	STB	HV Outputs
X	X	H	All Low
H	H	L	High
L	H	L	Low
X	L	L	*

* Previous state

Typical Operating Sequence



Pin Configurations

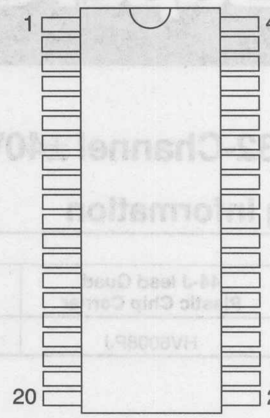
40 Pin Dual-In-Line Package

Pin	Function	Pin	Function
1	V_{PP}	21	Clock
2	Serial Out	22	LE
3	HV_{OUT} 32	23	HV_{OUT} 16
4	HV_{OUT} 31	24	HV_{OUT} 15
5	HV_{OUT} 30	25	HV_{OUT} 14
6	HV_{OUT} 29	26	HV_{OUT} 13
7	HV_{OUT} 28	27	HV_{OUT} 12
8	HV_{OUT} 27	28	HV_{OUT} 11
9	HV_{OUT} 26	29	HV_{OUT} 10
10	HV_{OUT} 25	30	HV_{OUT} 9
11	HV_{OUT} 24	31	HV_{OUT} 8
12	HV_{OUT} 23	32	HV_{OUT} 7
13	HV_{OUT} 22	33	HV_{OUT} 6
14	HV_{OUT} 21	34	HV_{OUT} 5
15	HV_{OUT} 20	35	HV_{OUT} 4
16	HV_{OUT} 19	36	HV_{OUT} 3
17	HV_{OUT} 18	37	HV_{OUT} 2
18	HV_{OUT} 17	38	HV_{OUT} 1
19	Strobe	39	Data In
20	GND	40	V_{DD}

44 Pin J-Lead Package

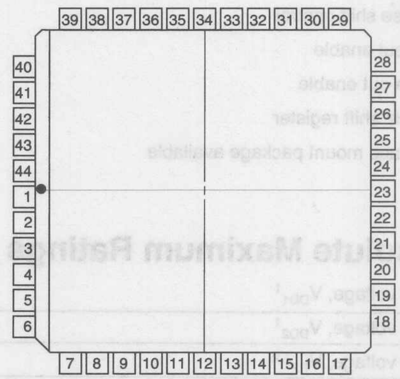
Pin	Function	Pin	Function
1	V_{PP}	23	Clock
2	Serial Out	24	LE
3	HV_{OUT} 32	25	HV_{OUT} 16
4	HV_{OUT} 31	26	HV_{OUT} 15
5	HV_{OUT} 30	27	HV_{OUT} 14
6	NC	28	NC
7	HV_{OUT} 29	29	NC
8	HV_{OUT} 28	30	HV_{OUT} 13
9	HV_{OUT} 27	31	HV_{OUT} 12
10	HV_{OUT} 26	32	HV_{OUT} 11
11	HV_{OUT} 25	33	HV_{OUT} 10
12	HV_{OUT} 24	34	HV_{OUT} 9
13	HV_{OUT} 23	35	HV_{OUT} 8
14	HV_{OUT} 22	36	HV_{OUT} 7
15	HV_{OUT} 21	37	HV_{OUT} 6
16	HV_{OUT} 20	38	HV_{OUT} 5
17	HV_{OUT} 19	39	HV_{OUT} 4
18	NC	40	HV_{OUT} 3
19	HV_{OUT} 18	41	HV_{OUT} 2
20	HV_{OUT} 17	42	HV_{OUT} 1
21	Strobe	43	Data In
22	GND	44	V_{DD}

Package Outline



top view

40-pin DIP



top view

44-pin J-Lead Package

Preliminary

32-Channel ±40V Liquid Crystal Display Row Driver

Ordering Information

Device	Package Options			
	44-J lead Quad Plastic Chip Carrier	44 -J Lead Quad Ceramic Chip Carrier	44-Lead Quad Plastic Gullwing	Die
HV6008	HV6008PJ	HV6008DJ	HV6008PG	HV6008X

Features

- ☐ Symmetrical ± 40V output swing
- ☐ Active return to GND
- ☐ 15mA peak source/sink/GND current per channel
- ☐ +5V control logic
- ☐ Special shift register with clear
- ☐ Phase shift control
- ☐ Output enable
- ☐ Data out enable
- ☐ 1MHz shift register
- ☐ Surface mount package available

Absolute Maximum Ratings

Supply voltage, V_{DD1} [1]	-6V
Supply voltage, V_{DD2} [1]	+6V
Supply voltage, V_{PP} [1,2]	+42V
Supply voltage, V_{NN} [1,2]	-42V
Logic input levels	V_{DD1} - 0.3V to V_{DD2} + 0.3V
Ground currrent[2]	700mA
Continuous total power dissipation[3]	1W
Operating temperature range	0°C to 70°C
Storage temperature range	-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 85°C at 15mW/°C.

General Description

The HV60 is a 32-channel liquid crystal display driver with 3-state DMOS outputs. Each output can be set to +40V, -40V, or GND. A symmetric waveform can be applied to a capacitive load using the phase shift feature of the HV60.

The HV60 consists of a 32-bit shift register with Clear, Enable, and Phase Shift logic, and 32 high voltage output buffers. With the Enable pin held low, all outputs are placed in the return to zero (GND) state. When Enable is high, each output reflects the data in its shift register bit. All outputs with a logic "0" in their shift register will be in the return to zero state. Outputs with a logic "1" in their shift register will reflect the state of the phase shift pin. These outputs will be switched to V_{PP} when phase shift is high and V_{NN} when phase shift is logic "0".

Additional functions provided are Shift Register Clear and Data Out. All bits of the shift register are changed to logic "0" when Clear is pulled low. With Clear at a logic "1", normal shift register operation proceeds. The data output reflects the status of the 32nd shift register stage.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
$I_{DD1,2}$	V_{DD} supply current	V_{DD1}			500	μA	$V_I = 4V$, $V_{DD1} = -6V$
		V_{DD2}					$V_I = 4V$, $V_{DD2} = +6V$
V_{IH}	Logic input high		+2		V_{DD2}	V	$V_{DD1} = -4.5V$,
V_{IL}	Logic input low		V_{DD1}		-2	V	$V_{DD2} = +4.5V$
V_{OH}	Logic output high		+2			V	$V_{DD1} = -4.5V$ $V_{DD2} = +4.5V$
V_{OL}	Logic output low				-2	V	$I_{OH} = -15μA$ $I_{OL} = 250μA$
I_{IH}	High-level logic input current				+3	μA	$V_I = V_{DD}$, $V_{DD1,2}$ = max
I_{IL}	Low-level logic input current				-50	μA	$V_I = 0V$, $V_{DD1,2}$ = max
I_{PP}	High voltage supply current				+1	mA	Static, no load
I_{NN}	High voltage supply current				-1	mA	Static, no load
V_{OH}	Output voltage high		+39			V	V_{PP}, $V_{NN} = \pm40$
V_{CL}	Output voltage clamp		-20		+20	mV	$I_{output} = 0.0$
V_{OL}	Output voltage low				-39	V	
Z_{OH}	Output switch impedence high			1000			
Z_{CL}	Output switch impedance clamp			500		Ω	V_{PP}, $V_{NN} = \pm40$
Z_{OL}	Output switch impedance low			700			$I_O = \pm15mA$
I_O	DC output current	Output H or L			5	mA	1 output only
		Data out H or L			150	μA	

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{WH}	Width of high clock phase		TBD			
t_{WL}	Width of low clock phase		TBD			
t_{SU}	Data set-up time before clock rises		TBD			
t_H	Data hold time after clock rises	0			ns	
	Phase shift duty cycle		50		%	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD1}	Logic supply voltage	-4		-6	V
V_{DD2}	Logic supply voltage	+4		+6	V
V_{PP}	High voltage supply	+10		+40	V
V_{NN}	High voltage supply	-10		-40	V
V_{IH}	High-level input voltage	+2V		V_{DD2}	V
V_{IL}	Low-level input voltage	-2V		V_{DD1}	V
$I_{O\,Pk.}$	Peak output current (any state)			±80	mA
T_A	Operating free-air temperature	0		+70	°C
f_{DIN}	Input data rate			1	MHz
f_{PS}	Phase shift rate			20	KHz

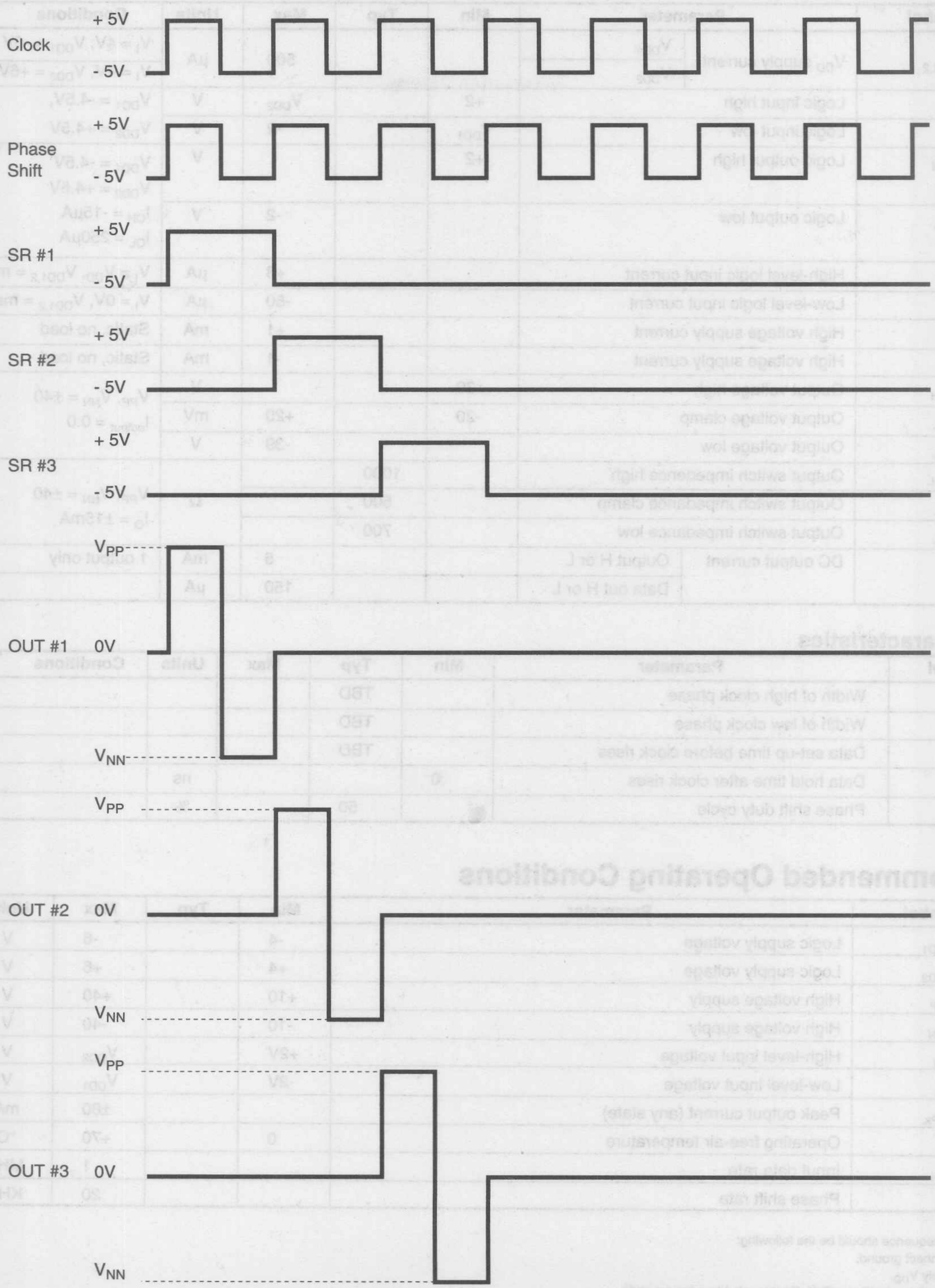
Note:

Power-up sequence should be the following:

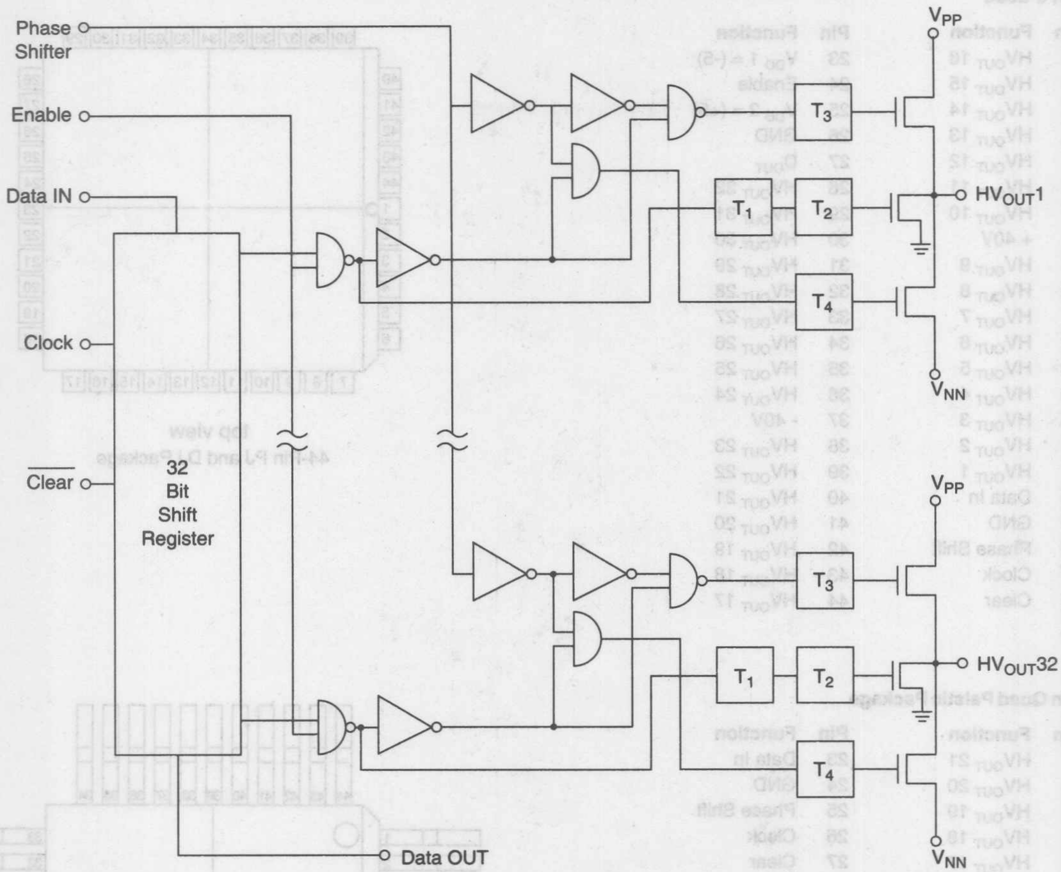
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply $_{VPP}$.

Power-down sequence should be the reverse of the above.

Switching Waveform



Functional Block Diagram



Function Table

Function	Inputs: Data In	CLK	CLR	Enable	Phase Shift	Outputs: Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out
CLR Reg	X	X	H	X	X	ALL L		ALL GND		L
All output GND	X	X	X	L	X	*	*…*	ALL GND		*
Load S/R	H or L	↓	L	L	X	H or L	*…*	ALL GND		*
Output State	X	H or L	L	H	X	L	L…L	GND	GND…GND	*
					H	H	H…H	V_{PP}	$V_{PP}…V_{PP}$	*
					L	H	H…H	V_{NN}	$V_{NN}…V_{NN}$	*

Notes:

X = Irrelevant
* = Dependent on previous stage's state before the last CLK
↓ = High to low transition
H = High level
L = Low level

Pin Configurations

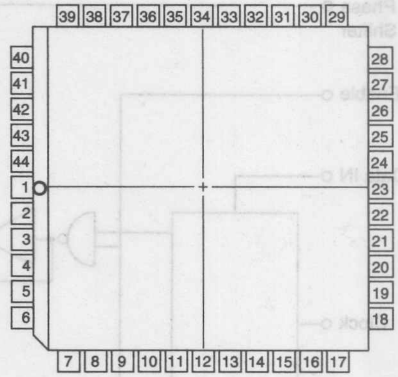
44-Pin J-Lead

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	V_{DD} 1 = (-5)
2	HV_{OUT} 15	24	Enable
3	HV_{OUT} 14	25	V_{DD} 2 = (+5)
4	HV_{OUT} 13	26	GND
5	HV_{OUT} 12	27	D_{OUT}
6	HV_{OUT} 11	28	HV_{OUT} 32
7	HV_{OUT} 10	29	HV_{OUT} 31
8	+ 40V	30	HV_{OUT} 30
9	HV_{OUT} 9	31	HV_{OUT} 29
10	HV_{OUT} 8	32	HV_{OUT} 28
11	HV_{OUT} 7	33	HV_{OUT} 27
12	HV_{OUT} 6	34	HV_{OUT} 26
13	HV_{OUT} 5	35	HV_{OUT} 25
14	HV_{OUT} 4	36	HV_{OUT} 24
15	HV_{OUT} 3	37	- 40V
16	HV_{OUT} 2	38	HV_{OUT} 23
17	HV_{OUT} 1	39	HV_{OUT} 22
18	Data In	40	HV_{OUT} 21
19	GND	41	HV_{OUT} 20
20	Phase Shift	42	HV_{OUT} 19
21	Clock	43	HV_{OUT} 18
22	Clear	44	HV_{OUT} 17

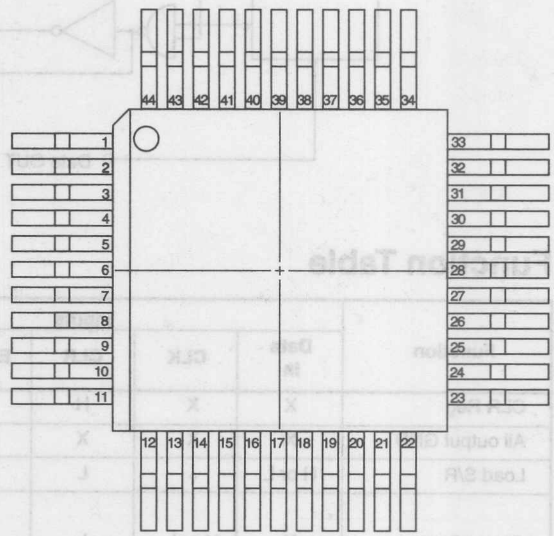
44-Pin Quad Palstic Package

Pin	Function	Pin	Function
1	HV_{OUT} 21	23	Data In
2	HV_{OUT} 20	24	GND
3	HV_{OUT} 19	25	Phase Shift
4	HV_{OUT} 18	26	Clock
5	HV_{OUT} 17	27	Clear
6	HV_{OUT} 16	28	-5V
7	HV_{OUT} 15	29	Enable
8	HV_{OUT} 14	30	+5V
9	HV_{OUT} 13	31	GND
10	HV_{OUT} 12	32	Data Out
11	HV_{OUT} 11	33	HV_{OUT} 32
12	HV_{OUT} 10	34	HV_{OUT} 31
13	V_{PP}	35	HV_{OUT} 30
14	HV_{OUT} 9	36	HV_{OUT} 29
15	HV_{OUT} 8	37	HV_{OUT} 28
16	HV_{OUT} 7	38	HV_{OUT} 27
17	HV_{OUT} 6	39	HV_{OUT} 26
18	HV_{OUT} 5	40	HV_{OUT} 25
19	HV_{OUT} 4	41	HV_{OUT} 24
20	HV_{OUT} 3	42	V_{NN}
21	HV_{OUT} 2	43	HV_{OUT} 23
22	HV_{OUT} 1	44	HV_{OUT} 22

Package Outlines



top view
44-Pin PJ and DJ Package



top view
44-pin Quad Plastic Package

Supertex inc.

32-Channel LCD Driver with Separate Backplane Output

Ordering Information

Device	Package Options	
	44 J-Lead Quad Plastic Chip Carrier	Dice in waffle pack
HV65	HV6506PJ	HV6506X

Features

- ☐ Processed with HVCMOS® technology
- ☐ 32 push-pull CMOS output up to 60V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 5mA
- ☐ Shift register speed 5MHz
- ☐ Latched data outputs
- ☐ Bidirectional shift register (DIR)
- ☐ Backplane output

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]	-0.5V to +7.0V
Output voltage, V_{PP}	-0.5V to +80V
Logic input levels[2]	-0.5V to V_{DD} + 0.5V
Ground currrent[3]	1.5A
Continuous total power dissipation[4]	1500mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +125°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to V_{SS}.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV65 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver circuit for LCD displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities. The inputs are fully CMOS compatible.

The device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select of the outputs. HVout1 is connected to the first stage of the shift register through the polarity logic. Data is shifted through the shift register on the logic low to high transition of the clock. A DIR pin causes data shifting counter-clockwise when grounded and clockwise when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable) or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored after LE transition from high to low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics (V_{DD} = 5V, V_{PP} = 60V, V_{SS} = GND)

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 5MHz
I_{PP}	High voltage supply current			0.5	mA	Outputs high
				0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	Q	52		V	I_O= 5mA, V_{PP} = 60V
		Data out	4.6		V	I_O= -100µA
V_{OL}	Low-level output	Q		8	V	I_O= 5mA, V_{PP} = 60V
		Data out		0.4	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			1	µA	V_{IL} = 0V
V_{OLBP}	Low-level output voltage, backplane			8	V	I_O = 40mA
V_{OHBP}	High-level output viltage, backplane		48		V	I_O = -40mA

AC Characteristics (V_{DD} = 5V, V_{PP} = 60V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		5	MHz	
t_W	Clock width high or low	100		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	50		ns	
t_{ON}, t_{OFF}	Time from latch enable or POL to HV_{OUT}		500	ns	C_L = 30pF
t_{ON}, t_{OFF}	Time from POL to BP output		500	ns	C_L = 30pF
t_{DHL}	Delay time clock to data high to low		200	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		200	ns	C_L = 15pF
t_{DLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	100		ns	
t_{SLE}	LE set-up time before clock rises	50		ns	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output off voltage	0	60	V
V_{IH}	High-level input voltage	3.5	V_{DD}	V
V_{IL}	Low-level input voltage	0	0.8	V
f_{CLK}	Clock frequency		5	MHz
T_A	Operating free-air temperature	-40	+85	°C
I_{OD}	Allowable current through output diodes		200	mA

Note:

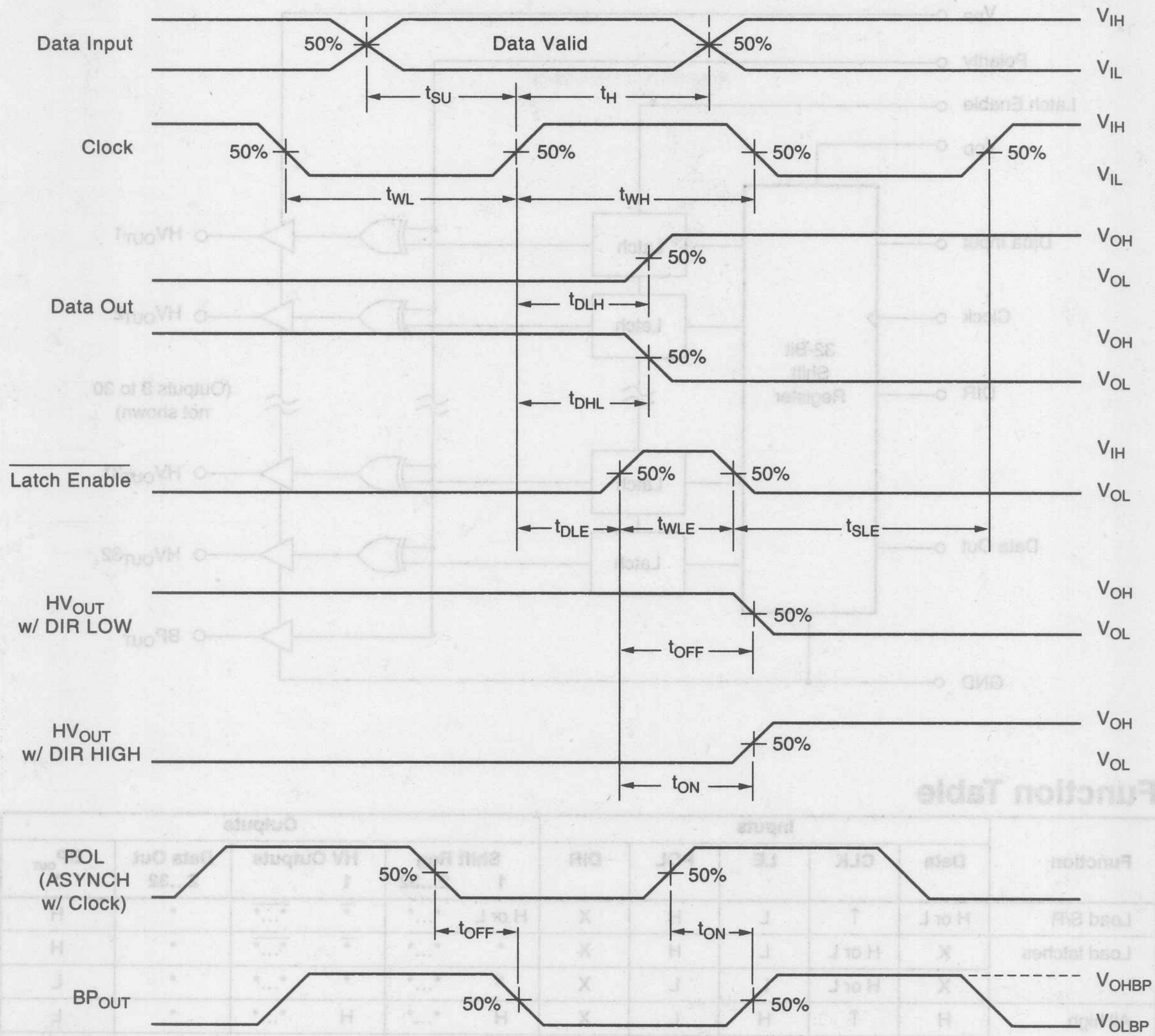
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

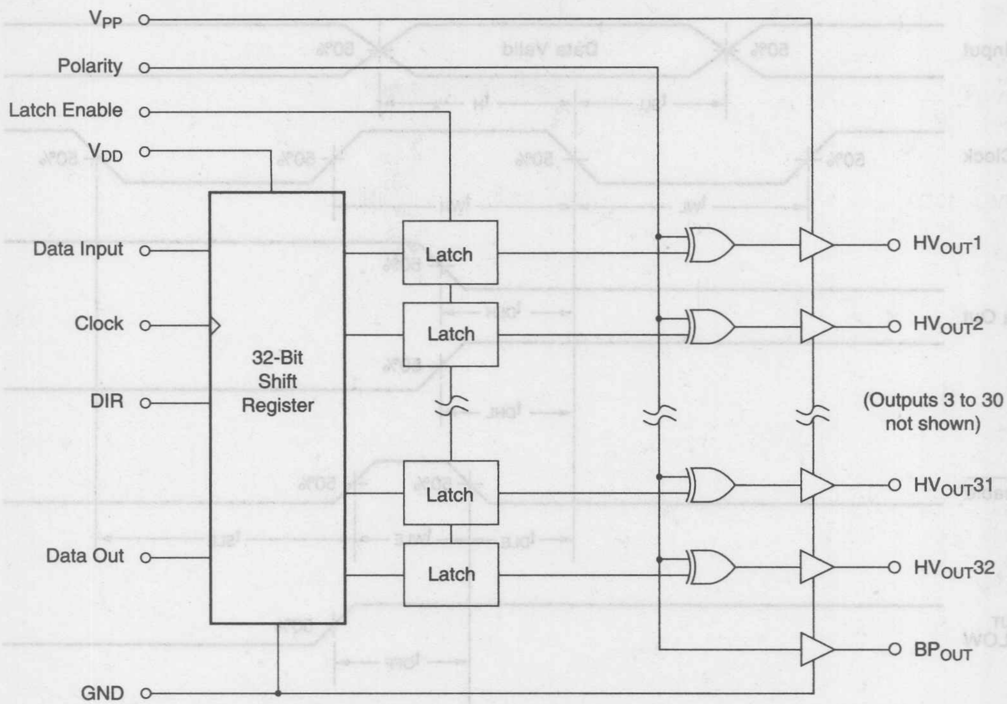
Power-down sequence should be the reverse of the above.

5. The V_{PP} should not drop below 0V during operation.

Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs					
	Data	CLK	LE	POL	DIR	Shift Reg 1	2…32	HV Outputs 1	2…32	Data Out	BP_{OUT}
Load S/R	H or L	↑	L	H	X	H or L	*…*	$\overline{*}$	$\overline{*…*}$	*	H
Load latches	X	H or L	L	H	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*	H
	X	H or L	L	L	X	*	*…*	*	*…*	*	L
All high	H	↑	H	L	X	H	*…*	H	*…*	*	L
	L	↑	H	H	X	L	*…*	H	*…*	*	H
All low	H	↑	H	H	X	H	*…*	H	*…*	*	H
	L	↑	H	L	X	L	*…*	H	*…*	*	L
Transparent Mode	L	↑	H	H	X	L	*…*	H	*…*	*	H
	H	↑	H	H	X	H	*…*	H	*…*	*	H
	L	↑	H	L	X	L	*…*	H	*…*	*	L
	H	↑	H	L	X	H	*…*	H	*…*	*	L
R/L Shift	X	↑	X	X	H	Qn → Qn+1		*	*…*	Q32	
	X	↑	X	X	L	Qn → Qn-1		*	*…*	Q1	

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last LE high.

Pin Configuration

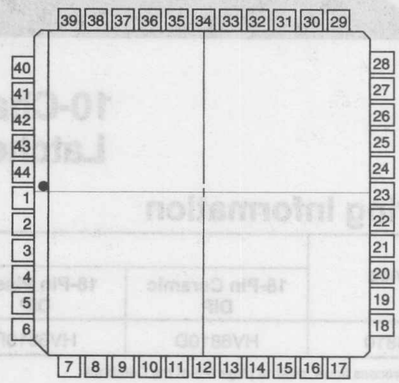
HV65
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17/16	23	LE
2	HV_{OUT} 16/17	24	V_{DD}
3	HV_{OUT} 15/18	25	Clock
4	HV_{OUT} 14/19	26	DIR
5	HV_{OUT} 13/20	27	Data In
6	HV_{OUT} 12/21	28	V_{PP}
7	HV_{OUT} 11/22	29	BP Out
8	HV_{OUT} 10/23	30	HV_{OUT} 32/1
9	HV_{OUT} 9/24	31	HV_{OUT} 31/2
10	HV_{OUT} 8/25	32	HV_{OUT} 30/3
11	HV_{OUT} 7/26	33	HV_{OUT} 29/4
12	HV_{OUT} 6/27	34	HV_{OUT} 28/5
13	HV_{OUT} 5/28	35	HV_{OUT} 27/6
14	HV_{OUT} 4/29	36	HV_{OUT} 26/7
15	HV_{OUT} 3/30	37	HV_{OUT} 25/8
16	HV_{OUT} 2/31	38	HV_{OUT} 24/9
17	HV_{OUT} 1/32	39	HV_{OUT} 23/10
18	Data Out	40	HV_{OUT} 22/11
19	GND	41	HV_{OUT} 21/12
20	N/C	42	HV_{OUT} 20/13
21	N/C	43	HV_{OUT} 19/14
22	POL	44	HV_{OUT} 18/15

Note:

1. Pin designation for DIR = L/H
   Example: for DIR = L Pin 1 is HV_{OUT} 17
   for DIR = H Pin 1 is HV_{OUT} 16
2. Blanking function is optional, BL pin can be left open when not used.

Package Outline



top view

44-pin J-Lead Package

Supertex inc.

HV6810

10-Channel Serial-Input Latched Display Driver

Ordering Information

Device	Package Options				
	18-Pin Ceramic DIP	18-Pin Plastic DIP	20-Pin Small Outline Package	20-Pin Plastic Chip Carrier	18-Pin Ceramic DIP (MIL-STD-883 Processed*)
HV6810	HV6810D	HV6810P	HV6810WG	HV6810PJ	RBHV6810D

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ High output voltage 80V
- ☐ High speed 5MHz @ $5V_{DD}$
- ☐ Low power $I_{BB} \leq 0.1mA$ (All high)
- ☐ Active pull down 100µA min
- ☐ Output source current 25mA
- ☐ Each device drives 10 lines
- ☐ High-speed serially-shifted data input
- ☐ 5V CMOS-compatible inputs
- ☐ Latches on all driver outputs
- ☐ Pin-compatible improved replacement for UCN5810A and TL4810A, TL4810B

General Description

The HV6810 is a monolithic integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large displays.

A 10-bit data word is serially loaded into the shift register on the positive-going transition of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and is latched when the latch enable is low. When the blanking input is high, all outputs are low.

Outputs are structures formed by double-diffused MOS (DMOS) transistors with output voltage ratings of 80 volts and 60 milliampere source-current capability. All inputs are compatible with CMOS levels.

Absolute Maximum Ratings[1]

Logic supply voltage, V_{DD}[2]		7.5V
Driver supply voltage, V_{BB}		90V
Output voltage		90V
Input voltage		-0.3V to V_{DD} + 0.3V
Continuous total power dissipation at 25°C free-air temperature [3]	Ceramic	1500mW
	Plastic	875mW
Operating Temperature Range	CommerClal	-40 to +85°C
	Military	-55 to +125°C

Notes:
1. Over operating free-air temperature.
2. All voltages are referenced to V_{SS}.
3. For operation above 25°C free-air temperature the derating factor is 7.0mW/°C.

Electrical Characteristics

DC Characteristics (V_{DD} = 5V ±10%, V_{BB} = 60V, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
V_{OH}	High-level output voltage	Q outputs	57.5	58		V	I_{OH} = 25mA
		Serial output	4	4.5		V	V_{DD} = 4.5V, I_{OH} = -100µA
V_{OL}	Low-level output voltage	Q outputs		0.15	1	V	I_{OH} = 100µA, Blanking input at V_{DD}
		Serial output		0.05	0.1	V	V_{DD} = 4.5V, I_{OL} = 100µA
I_{OL}	Low-level Q output current (pull-down current)		60	80		µA	T_A = Max, V_{OL} = 0.7V
$I_{O(OFF)}$	Off-state output current			-1	-15	µA	V_O = 0, Blanking input T_A = Max at V_{DD}
I_H	High-level input current				1	µA	V_I = V_{DD}
I_{DD}	Supply current from V_{DD} (standby)			10	50	µA	All inputs at 0V, one Q output high
				10	50	µA	All inputs at 0V, all Q outputs low
I_{BB}	Supply current from V_{BB}			0.05	0.1	mA	All outputs low, all Q outputs open
				0.05	0.1	mA	All outputs high, all Q outputs open

* All typical values are at T_A = 25°C, except for I_O.

AC Characteristics (Timing requirements over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$t_{W(CKH)}$	Pulse duration, clock high	100			ns	
$t_{W(LEH)}$	Pulse duration, latch enable high	100			ns	
$t_{SU(D)}$	Setup time, data before clock	50			ns	
$t_{H(D)}$	Setup time, data after clock	50			ns	
$t_{CKH-LEH}$	Delay time, clock to latch enable high	50			ns	
t_{pd}*	Propagation delay time, latch enable to output		0.3		µs	

* Switching characteristics, V_{BB} = 60V, T_A = 25°C.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{DD}	Supply voltage		4.5		5.5	V
V_{BB}	Supply voltage		20		80	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage (for V_{DD} = 5V)		3.5		5.3	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
I_{OH}	Continuous high-level Q output current		-25			mA
T_A	Operating free-air temperature	CommerCIal	-40		+85	°C
		Military	-55		+125	

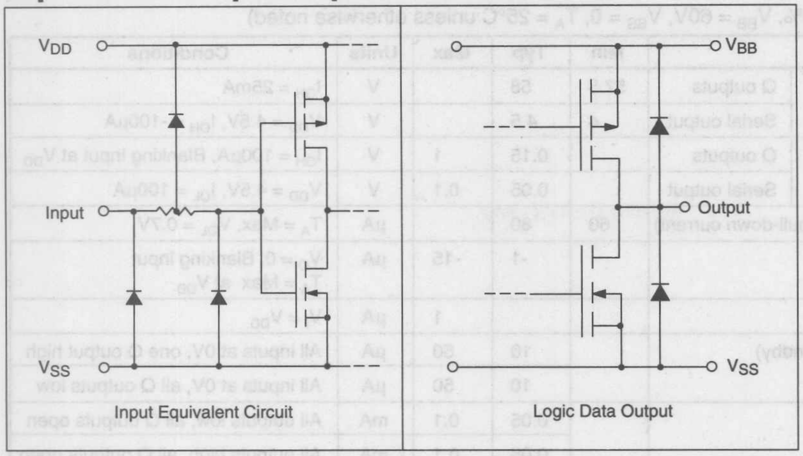
Note:

Power-up sequence should be the following:

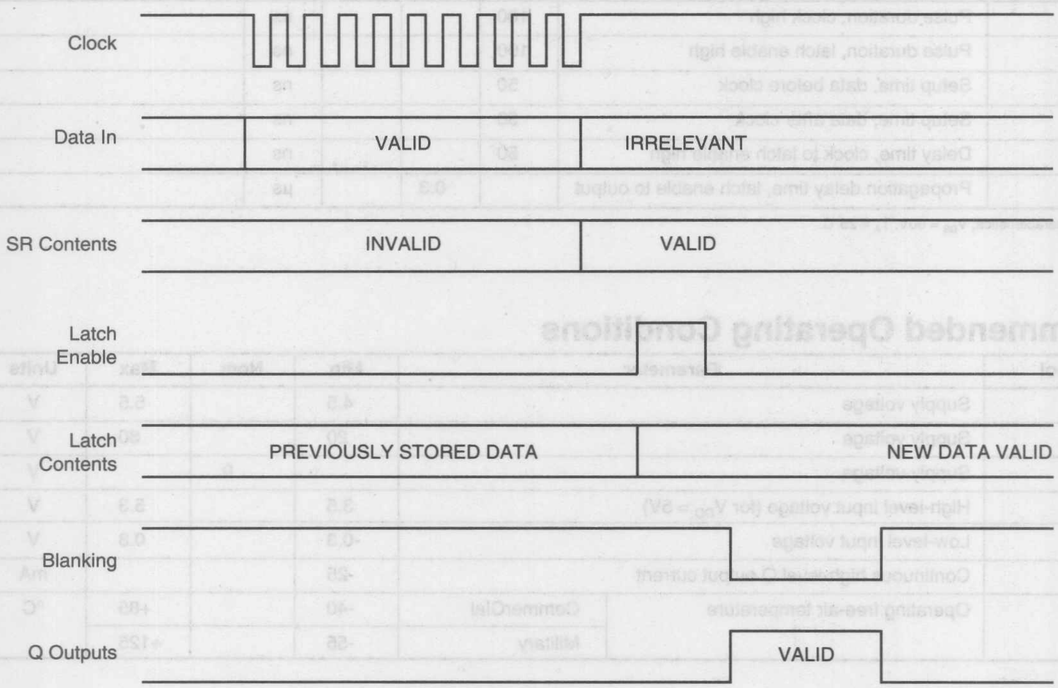
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits

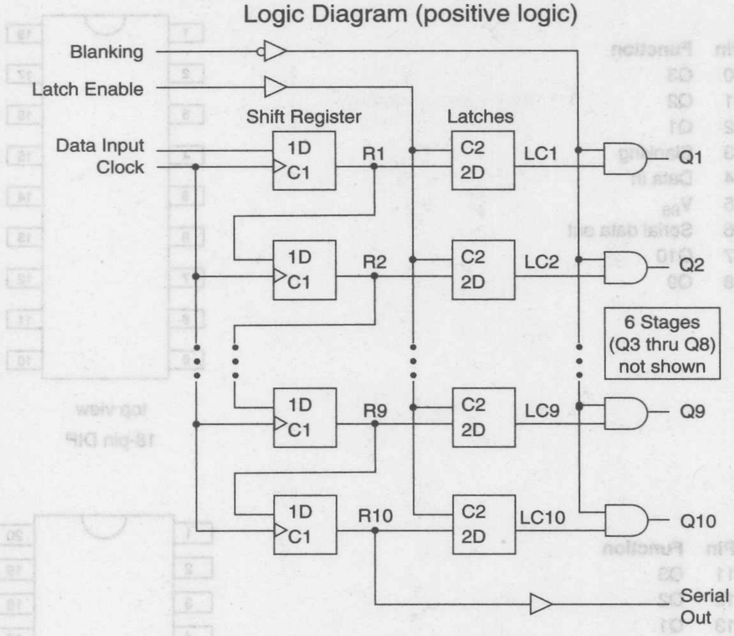


Timing Diagram



Functional Block Diagram

Logic Diagram (positive logic)

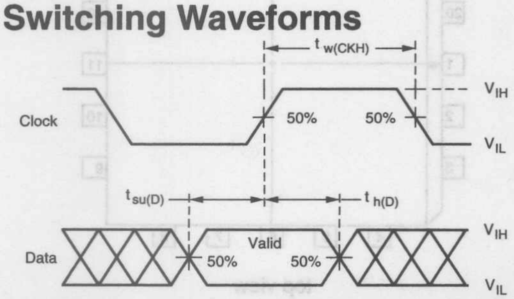


Function Table

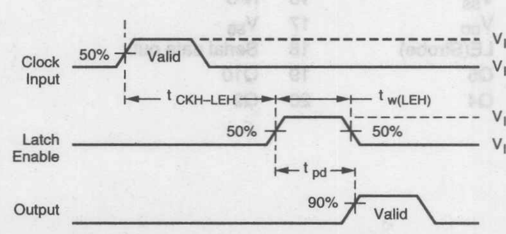
Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_{N-1}\ I_N$	Blanking Input	Output Contents $I_1\ I_2\ I_3 \ldots I_{N-1}\ I_N$
H	↑	$H\ R_1\ R_2 \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	↑	$L\ R_1\ R_2 \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	↓	$R_1\ R_2\ R_3 \ldots R_{N-1}\ R_N$	R_N				
		X X X … X X	X	L	$R_1\ R_2\ R_3 \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3 \ldots P_{N-1}\ P_N$
					X X X … X X	H	L L L … L L

L = Low logic level
H = High logic level
X = Irrelevant
P = Present state
R = Previous state

Switching Waveforms



Input Timing



Output Switching Times

Pin Configurations

18-Pin DIP

Pin	Function	Pin	Function
1	Q8	10	Q3
2	Q7	11	Q2
3	Q6	12	Q1
4	Clock	13	Blanking
5	V_{SS}	14	Data in
6	V_{DD}	15	V_{BB}
7	LE (strobe)	16	Serial data out
8	Q5	17	Q10
9	Q4	18	Q9

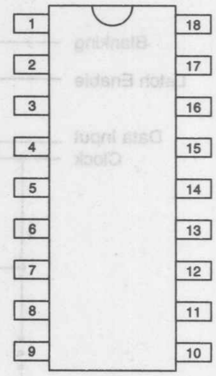
20-Pin SOW

Pin	Function	Pin	Function
1	Q8	11	Q3
2	Q7	12	Q2
3	Q6	13	Q1
4	Clock	14	Blanking
5	V_{SS}	15	Data in
6	N/C	16	V_{BB}
7	V_{DD}	17	Serial data out
8	LE (strobe)	18	N/C
9	Q5	19	Q10
10	Q4	20	Q9

20-Pin Plastic PLCC

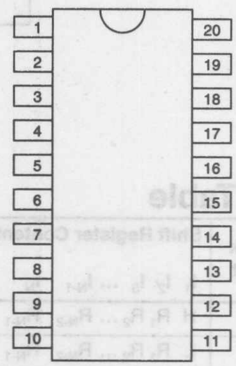
Pin	Function	Pin	Function
1	Q8	11	Q3
2	Q7	12	Q2
3	Q6	13	Q1
4	Clock	14	Blanking
5	N/C	15	Data In
6	V_{SS}	16	N/C
7	V_{DD}	17	V_{BB}
8	LE(Strobe)	18	Serial data out
9	Q5	19	Q10
10	Q4	20	Q9

Package Outlines



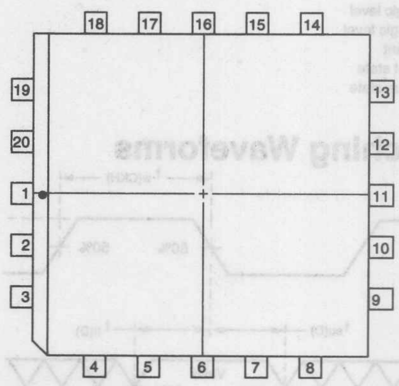
top view

18-pin DIP



top view

SOW 20



top view

20-pin PJ and PG Package

Supertex inc. HV70

34-Channel Symmetric Row Driver

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack	44 J-Lead Quad Ceramic Chip Carrier (MIL-Std-883 Processed*)
HV7022	HV7022DJ	HV7022PJ	HV7022X	RBHV7022DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ Processed with HVCMOS® technology
- ☐ Symmetric row drive (reduces latent imaging in ACTFEL displays)
- ☐ Output voltages up to 230V
- ☐ Low-power level shifting
- ☐ Source/Sink current 70mA (min.)
- ☐ Shift register speed 4MHz
- ☐ Pin-programmable shift direction
- ☐ 44-lead plastic & ceramic surface-mount packages
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +15V
Supply voltage, V_{PP}		-0.3V to +250V
Logic input levels		-0.3V to V_{DD} +0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]:	Ceramic Plastic	1500mW 1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:

1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV70 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suited for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. The HV70 offers 34 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After DATA INPUT is entered (on the falling edge of CLOCK), a logic high will cause the output to swing to V_{PP} if POL is high, or to GND if POL is low.

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Electrical Characteristics

(over recommended operating conditions of V_{DD} = 12V, T_A = 25°C and V_{PP} = 230V unless otherwise noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 4MHz
I_{PP}	High voltage supply current			4	mA	1 Output high[1]
				100	µA	All Outputs low or High-Z
				750	µA	All Outputs low or High-Z (125°C)
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	195		V	I_O= -70mA (-50mA)[2]
		Data out	11		V	I_O= -500µA
V_{OL}	Low-level output	HV_{OUT}		30	V	I_O= 70mA (+50mA)[2]
		Data out		1	V	I_O= 500µA
I_{IH}	High-level logic input current			1	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

Note:
1. The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.
2. Over military temperature range (-55°C to 125°C).

AC Characteristics (V_{DD} = 12V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		4	MHz	
t_W	Pulse duration clock high or low	125		ns	
t_{SUD}	Data set-up time before falling clock	100		ns	
t_{HD}	Data hold time after falling clock	100		ns	
t_{SUC}	Setup time clock low before V_{PP}↑ or GND↓	300		ns	
t_{SUE}	Setup time enable high before V_{PP}↑ or GND↓	300		ns	
t_{SUP}	Setup time polarity high or low before V_{PP}↑ or GND↓	300		ns	
t_{HC}	Hold time clock high after V_{PP}↑ or GND↓	500		ns	
t_{HE}	Hold time enable high after V_{PP}↑ or GND↓	300		ns	
t_{HP}	Hold time polarity high or low after V_{PP}↑ or GND↓	300		ns	
t_{DHL}	Delay time high to low level output from clock		150	ns	C_L = 10pF
t_{DLH}	Delay time low to high level output from clock		200	ns	C_L = 10pF
t_{THL}	Transition time high to low level serial output		200	ns	C_L = 15pF
t_{TLH}	Transition time low to high level serial output		100	ns	C_L = 15pF
t_{ONH}	High level turn-on time Q outputs from enable		500	ns	I_O = -50 mA, V_{OH} =195V R_L = 2 kΩ to 95V
t_{ONL}	Low level turn-on time Q outputs from enable		500	ns	I_O = 50 mA, V_{OH} =130V R_L = 2 kΩ to 30V
t_{OFFH}	High level turn-off time Q outputs from enable		1000	ns	I_O = -50 mA, V_{OH} =195V R_L = 2 kΩ to 95V
t_{OFFL}	Low level turn-off time Q outputs from enable		500	ns	I_O = 50 mA, V_{OH} =130V R_L = 2 kΩ to 30V
	Slew rate, V_{PP} or GND		45	V/µs	With one active output driving a 4.7 nF load to V_{PP} or GND

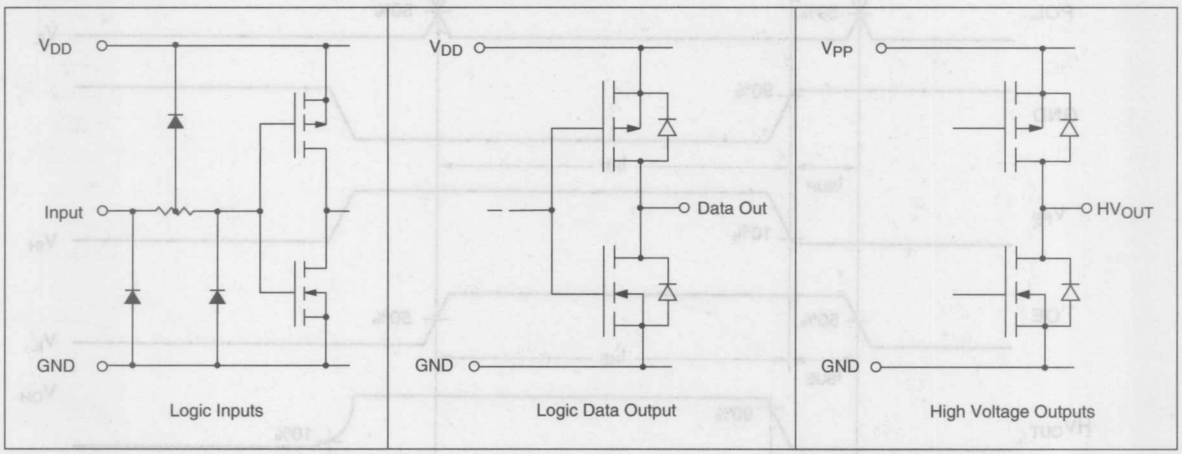
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply			230	V
V_{IH}	High-level input voltage	V_{DD} = 10.8V	8.1		V
		V_{DD} = 13.2V	9.9		
V_{IL}	Low-level input voltage	V_{DD} = 10.8V		2.7	V
		V_{DD} = 13.2V		3.3	
f_{CLK}	Clock frequency			4	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	°C
I_{DD}	Allowable pulse current through output diode			300	mA

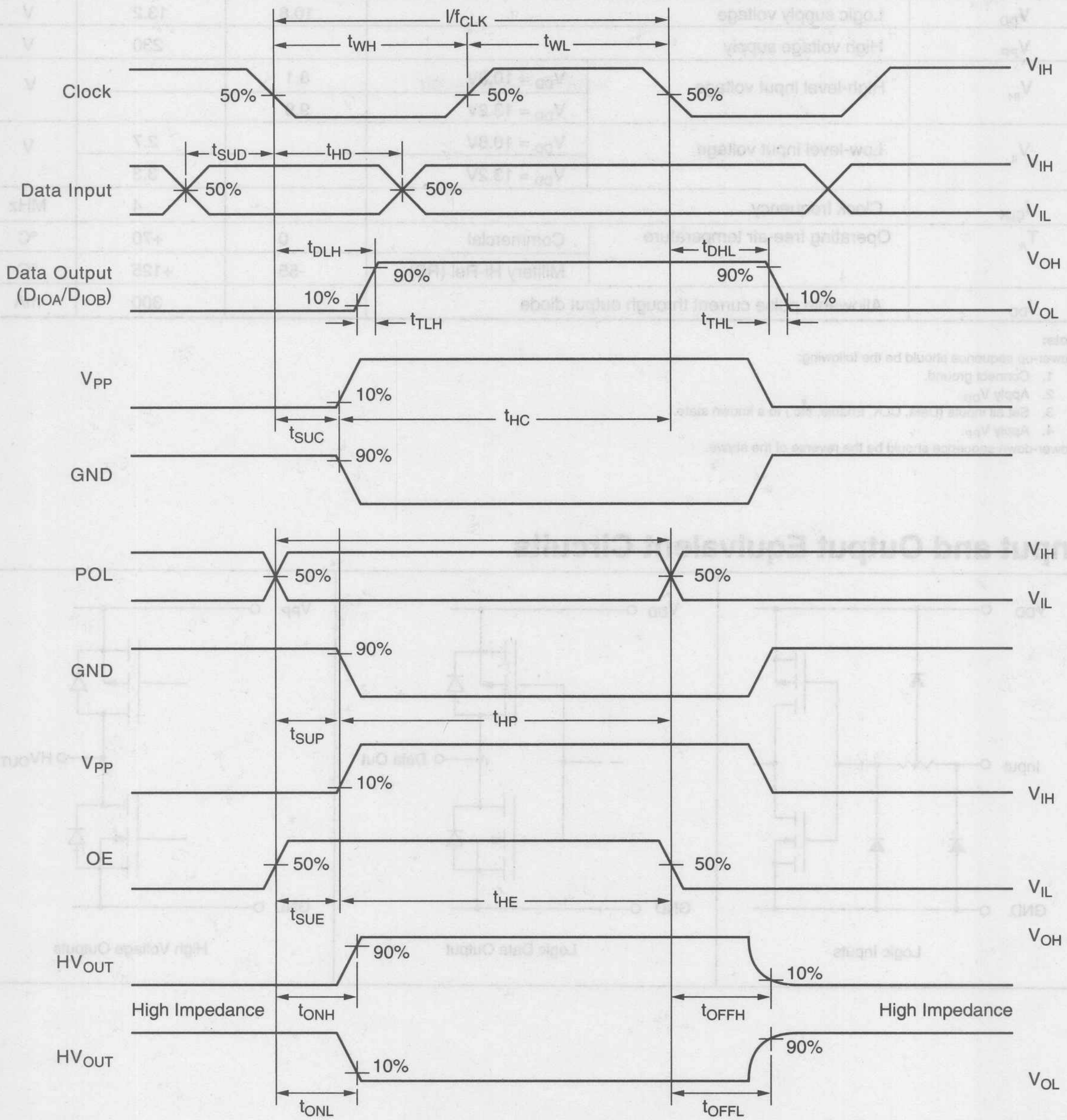
Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

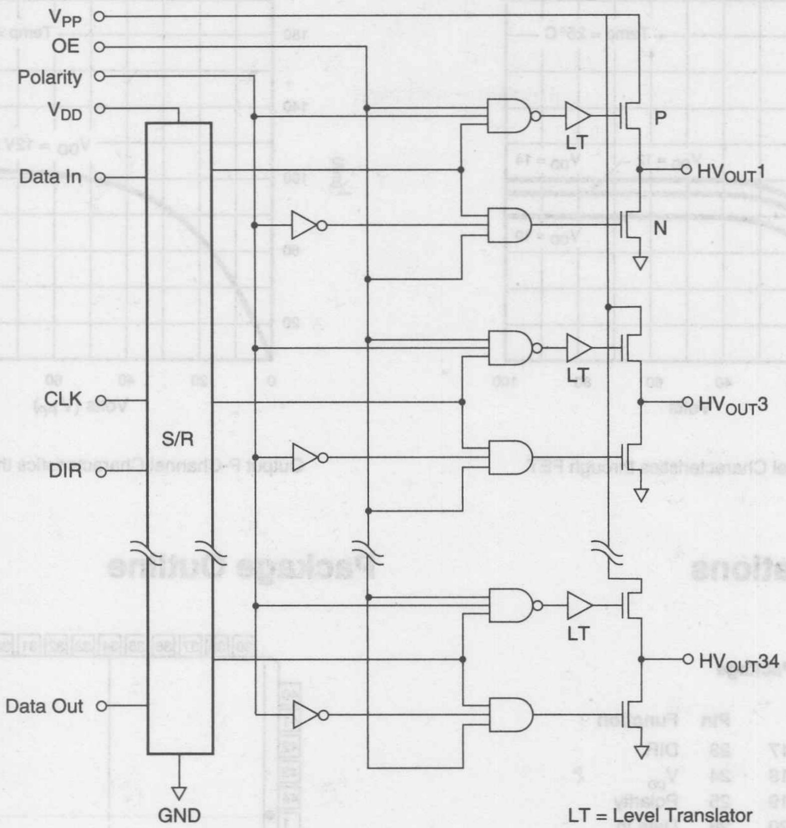
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



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Function Table

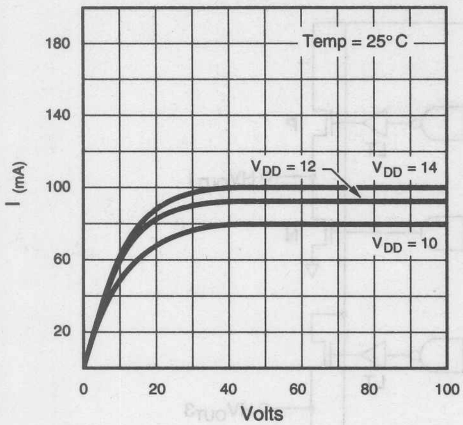
I/O Relations	Inputs					Outputs		
	CLK	DIR	Data	POL	OE	Shift Reg	HV Outputs	Data Out
O/P HIGH	X	X	H	H	H	*	H	
O/P OFF	X	X	L	H	H	*	HIGH-Z	*
O/P LOW	X	X	H	L	H	*	L	*
O/P OFF	X	X	L	L	H	*	HIGH-Z	*
O/P OFF	X	X	X	X	L	*	All O/P HIGH-Z	*
Load S/R, set DIR	↓	L	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q_{34}
	↓	H	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q_1
	No ↓	X	X	X	X	*	No Change	No Change

Notes:

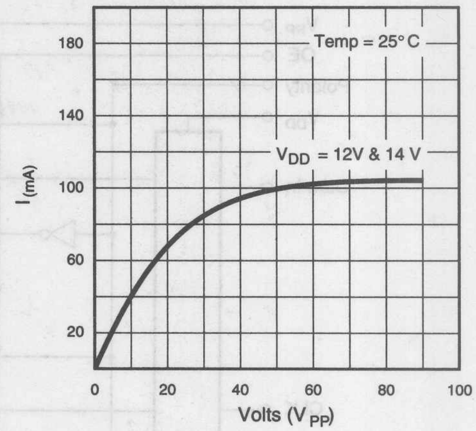
H = logic high level, L = logic low level, X = irrelevant, ↓ = high-to-low transition,
$Q_1 = HV_{OUT}$ 1, $Q_n = HV_{OUT}(n)$, etc.

* = dependent on previous state and whether an O/P or S/R command occured.

HV_{OUT} Characteristics



Output N-Channel Characteristics through FET



Output P-Channel Characteristics through FET

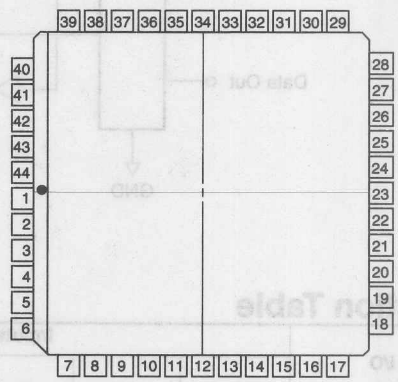
Pin Configurations

HV70
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 18/17	23	DIR
2	HV_{OUT} 17/18	24	V_{DD}
3	HV_{OUT} 16/19	25	Polarity
4	HV_{OUT} 15/20	26	Data In
5	HV_{OUT} 14/21	27	V_{PP}
6	HV_{OUT} 13/22	28	N/C
7	HV_{OUT} 12/23	29	HV_{OUT} 34/1
8	HV_{OUT} 11/24	30	HV_{OUT} 33/2
9	HV_{OUT} 10/25	31	HV_{OUT} 32/3
10	HV_{OUT} 9/26	32	HV_{OUT} 31/4
11	HV_{OUT} 8/27	33	HV_{OUT} 30/5
12	HV_{OUT} 7/28	34	HV_{OUT} 29/6
13	HV_{OUT} 6/29	35	HV_{OUT} 28/7
14	HV_{OUT} 5/30	36	HV_{OUT} 27/8
15	HV_{OUT} 4/31	37	HV_{OUT} 26/9
16	HV_{OUT} 3/32	38	HV_{OUT} 25/10
17	HV_{OUT} 2/33	39	HV_{OUT} 24/11
18	HV_{OUT} 1/34	40	HV_{OUT} 23/12
19	Data Out	41	HV_{OUT} 22/13
20	Output Enable	42	HV_{OUT} 21/14
21	Clock	43	HV_{OUT} 20/15
22	GND	44	HV_{OUT} 19/16

Note:
Pin designation for DIR L/H
Example: For DIR = L, pin 1 is HV_{OUT} 18
For DIR = H, pin 1 is HV_{OUT} 17

Package Outline



top view
44-pin J-Lead Package

Supertex inc.

HV72

Product Objective Specification

40-Channel Symmetric Row Driver

Ordering Information

Device	Package Options			
	80-Lead Ceramic Gullwing	64-Lead 3-Sided Plastic Gullwing	Die in waffle pack	80-Lead Ceramic Gullwing (MIL-STD-883 Processed*)
HV7225	HV7225DG	HV7225PG	HV7225X	RBHV7225DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- □ Processed with HVCMOS® technology
- □ Symmetric row drive (reduces latent imaging in ACTFEL displays)
- □ Output voltage up to 250V
- □ Low-power level shifting
- □ Source/Sink current 100mA (max.)
- □ Shift Register Speed 4MHz
- □ Pin-programmable shift direction (DIR, SHIFT)
- □ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7V
Supply voltage, V_{PP}		-0.5V to +275V
Logic input levels		-0.5V to V_{DD} +0.5V
Continuous total power dissipation[2]	Ceramic Plastic	1500mW 1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes: 1. All voltages are referenced to GND.
2. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV72 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. For packaged parts, a DIR pin controls the direction of data shift through the device. When DIR is at logic high, D_{IOA} is Data-in and D_{IOB} is Data-out, data is shifted from $HV_{OUT}1$ to $HV_{OUT}40$, When DIR is grounded, D_{IOB} is Data-in and D_{IOA} is Data-out, the data is then shifted from $HV_{OUT}40$ to $HV_{OUT}1$. The $\overline{POL}$ and $\overline{OE}$ pins perform the polarity select and output enable function respectively. Data is loaded on the low to high transition of the clock. A logic high will cause the output to swing to V_{PP} if $\overline{POL}$ is high, or to GND if $\overline{POL}$ is low. All outputs will be in High-Z state if $\overline{OE}$ is at logic high. Data output buffers are provided for cascading devices.

There are two output pin configurations, Option A and B. When the SHIFT pin is logic low, the device operates in Option A; when the SHIFT pin is logic high, the device operates in Option B.

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Electrical Characteristics

(over recommended operating conditions of V_{DD} = 5V, V_{PP} = 250V, and T_A = 25°C unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 4MHz
I_{pp}	High voltage supply current			1.0	mA	All outputs low or High-Z (-40°C to 85°C)
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All V_{IN} = GND or V_{DD} (-40°C to +80°C)
V_{OH}	High-level output	HV_{OUT}	200		V	I_O= -70mA (-50mA)[2]
		Data out	4.5		V	I_O= -500µA
V_{OL}	Low-level output	HV_{OUT}		50	V	I_O= 70mA (-50mA)[2]
		Data out		0.5	V	I_O= 500µA
I_{IH}	High-level logic input current			1	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

Notes:

1. Only one output can be turned on at a time.
2. Over military temperature range.

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		4	MHz	
$t_{W (H/L)}$	Pulse width - clock high or low	125		ns	
t_{SUD}	Data set-up time before clock rises	50		ns	
t_{HD}	Data hold time after clock rises	50		ns	
t_{SUC}	HV_{OUT} delay from clock rises		600	ns	
t_{SUE}	HV_{OUT} delay from output enable rises		500	ns	
t_{SUP}	HV_{OUT} delay from polarity falls		500	ns	
t_{HC}	HV_{OUT} delay from clock rises		600	ns	
t_{HE}	HV_{OUT} delay from enable falls		500	ns	
t_{HP}	HV_{OUT} delay from polarity rises		500	ns	
t_{DHL}	Delay time clock to data output falls		160	ns	C_L = 15pF
t_{DLH}	Delay time clock to data output rises		160	ns	C_L = 15pF
t_{ONF}	HV_{OUT} fall time		2	µs	C_L = 330pF R_L = 10 kΩ
t_{ONR}	HV_{OUT} rise time		2	µs	C_L = 330 pF R_L = 10 kΩ
t_{POW}	$\overline{\text{Polarity}}$ pulse width	3		µs	
t_{OEW}	$\overline{\text{Output enable}}$ pulse width	3		µs	

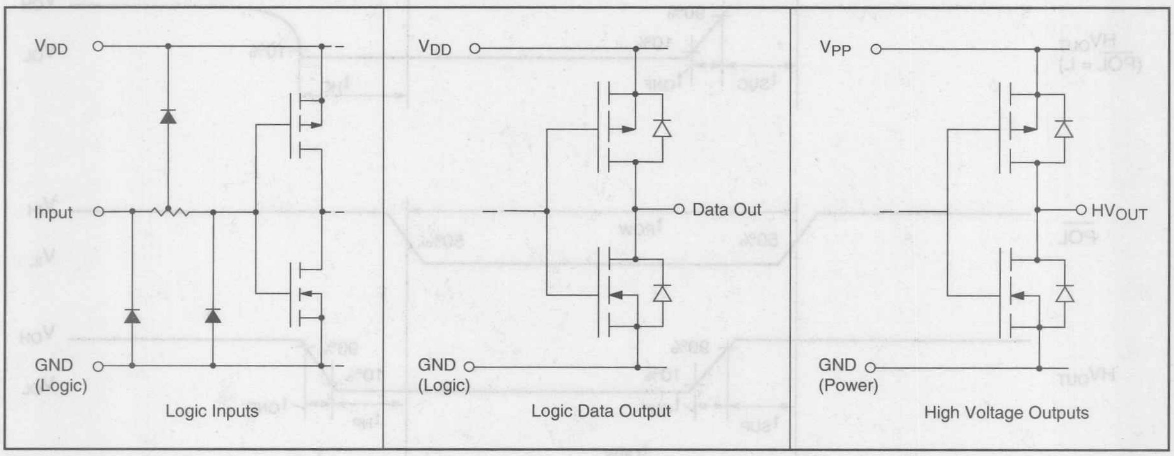
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
V_{PP}	High voltage supply†		0	250	V
V_{IH}	High-level input voltage		0.7 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		0	0.2V_{DD}	V
f_{CLK}	Clock frequency			4	MHz
I_O	High voltage output current			±70	mA
T_A	Operating free-air temperature		-40	+85	°C
		Military Hi-Rel (RB)	-55	+125	°C

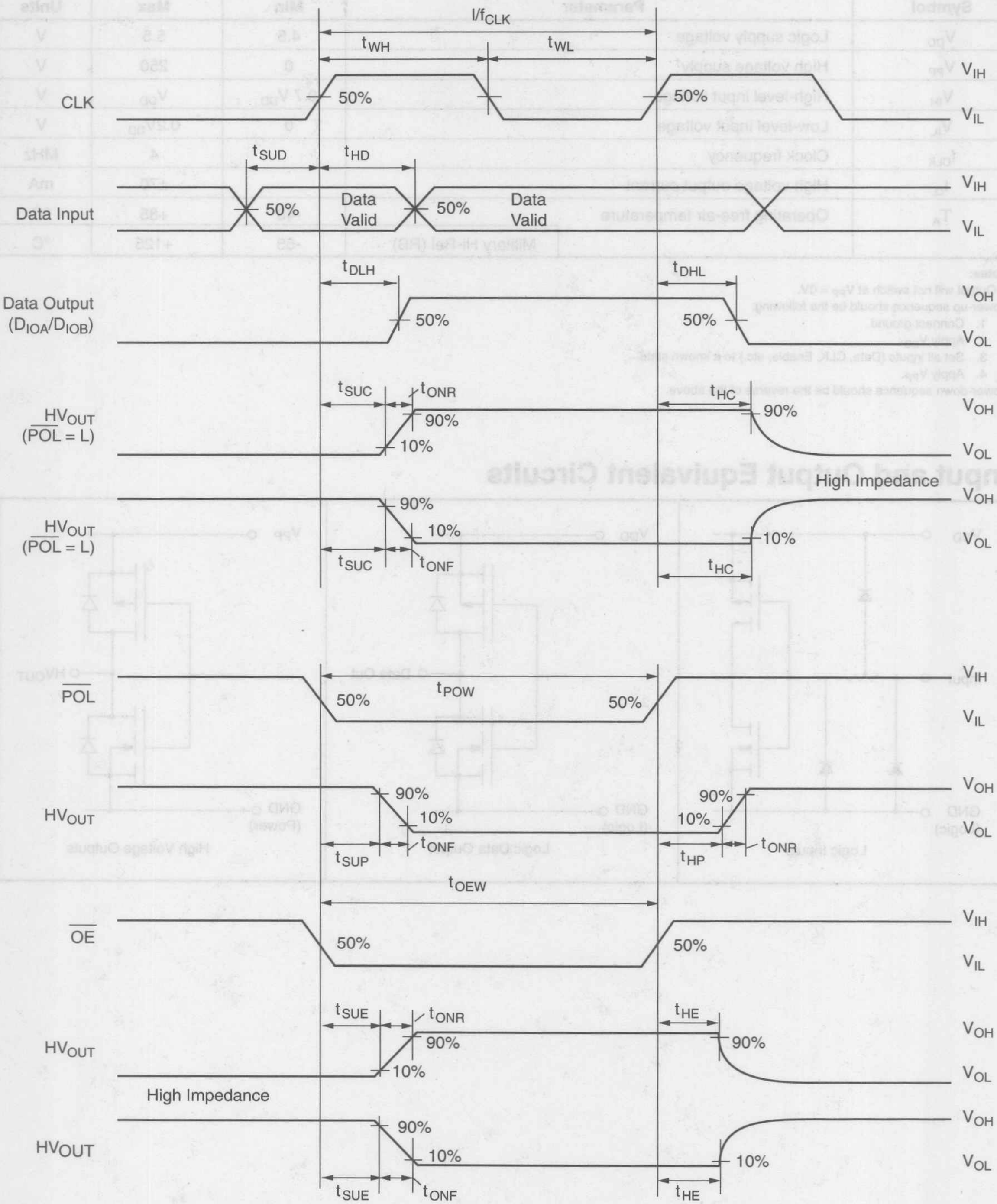
Notes:
† Output will not switch at V_{PP} = 0V.
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

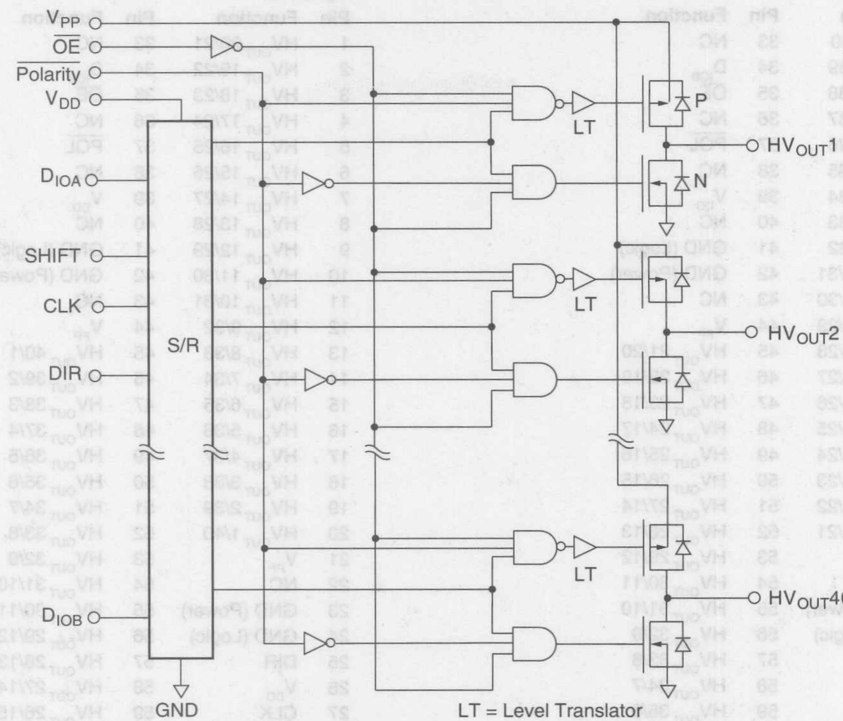
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

I/O Relations	Inputs					Outputs		
	CLK	DIR	Data	$\overline{POL}$	$\overline{OE}$	Shift Reg	HV Outputs	Data Out
O/P HIGH	X	X	H	H	L	*	H	*
O/P OFF	X	X	L	X	L	*	HIGH-Z	*
O/P LOW	X	X	H	L	L	*	L	*
O/P OFF	X	X	X	X	H	*	All O/P HIGH-Z	*
Load S/R, Set DIR	↑	H	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q40
	↑	L	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q1
I/O Relation	X	H	D_{IOA}	X	X	*	*	D_{IOB}
	X	L	D_{IOB}	X	X	*	*	D_{IOA}

Notes:
H = logic high level, L = logic low level, X = irrelevant, ↑ = low to high transition
* = dependent on previous state and whether an O/P or S/R command occured

Pin Configurations

Option A:

Pin	Function	Pin	Function
1	HV_{OUT}1/40	33	NC
2	HV_{OUT}2/39	34	D_{IOB}
3	HV_{OUT}3/38	35	$\overline{OE}$
4	HV_{OUT}4/37	36	NC
5	HV_{OUT}5/36	37	$\overline{POL}$
6	HV_{OUT}6/35	38	NC
7	HV_{OUT}7/34	39	V_{DD}
8	HV_{OUT}8/33	40	NC
9	HV_{OUT}9/32	41	GND (Logic)
10	HV_{OUT}10/31	42	GND (Power)
11	HV_{OUT}11/30	43	NC
12	HV_{OUT}12/29	44	V_{PP}
13	HV_{OUT}13/28	45	HV_{OUT}21/20
14	HV_{OUT}14/27	46	HV_{OUT}22/19
15	HV_{OUT}15/26	47	HV_{OUT}23/18
16	HV_{OUT}16/25	48	HV_{OUT}24/17
17	HV_{OUT}17/24	49	HV_{OUT}25/16
18	HV_{OUT}18/23	50	HV_{OUT}26/15
19	HV_{OUT}19/22	51	HV_{OUT}27/14
20	HV_{OUT}20/21	52	HV_{OUT}28/13
21	V_{PP}	53	HV_{OUT}29/12
22	NC	54	HV_{OUT}30/11
23	GND (Power)	55	HV_{OUT}31/10
24	GND (Logic)	56	HV_{OUT}32/9
25	DIR	57	HV_{OUT}33/8
26	V_{DD}	58	HV_{OUT}34/7
27	CLK	59	HV_{OUT}35/6
28	NC	60	HV_{OUT}36/5
29	SHIFT	61	HV_{OUT}37/4
30	NC	62	HV_{OUT}38/3
31	D_{IOA}	63	HV_{OUT}39/2
32	NC	64	HV_{OUT}40/1

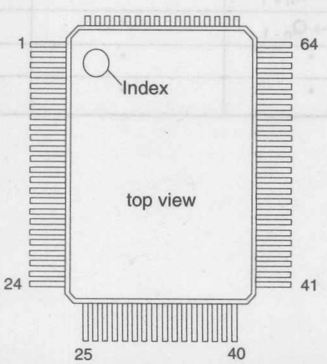
Note: Pin designation for DIR H/L, SHIFT = L.
Example: For DIR = H, pin 1 is HV_{OUT}1.
For DIR = L, pin 1 is HV_{OUT}40.
Pins 65–80 are NC (ceramic only).

Option B:

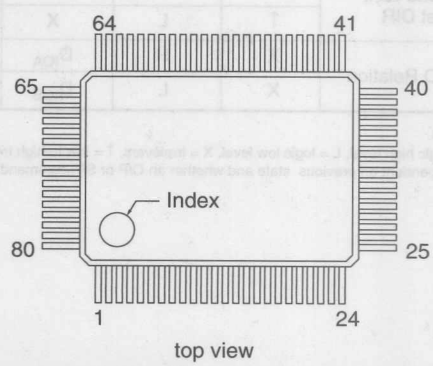
Pin	Function	Pin	Function
1	HV_{OUT}20/21	33	NC
2	HV_{OUT}19/22	34	D_{IOB}
3	HV_{OUT}18/23	35	$\overline{OE}$
4	HV_{OUT}17/24	36	NC
5	HV_{OUT}16/25	37	$\overline{POL}$
6	HV_{OUT}15/26	38	NC
7	HV_{OUT}14/27	39	V_{DD}
8	HV_{OUT}13/28	40	NC
9	HV_{OUT}12/29	41	GND (Logic)
10	HV_{OUT}11/30	42	GND (Power)
11	HV_{OUT}10/31	43	NC
12	HV_{OUT}9/32	44	V_{PP}
13	HV_{OUT}8/33	45	HV_{OUT}40/1
14	HV_{OUT}7/34	46	HV_{OUT}39/2
15	HV_{OUT}6/35	47	HV_{OUT}38/3
16	HV_{OUT}5/36	48	HV_{OUT}37/4
17	HV_{OUT}4/37	49	HV_{OUT}36/5
18	HV_{OUT}3/38	50	HV_{OUT}35/6
19	HV_{OUT}2/39	51	HV_{OUT}34/7
20	HV_{OUT}1/40	52	HV_{OUT}33/8
21	V_{PP}	53	HV_{OUT}32/9
22	NC	54	HV_{OUT}31/10
23	GND (Power)	55	HV_{OUT}30/11
24	GND (Logic)	56	HV_{OUT}29/12
25	DIR	57	HV_{OUT}28/13
26	V_{DD}	58	HV_{OUT}27/14
27	CLK	59	HV_{OUT}26/15
28	NC	60	HV_{OUT}25/16
29	SHIFT	61	HV_{OUT}24/17
30	NC	62	HV_{OUT}23/18
31	D_{IOA}	63	HV_{OUT}22/19
32	NC	64	HV_{OUT}21/20

Note: Pin designation for DIR L/H, SHIFT = H.
Example: For DIR = L, pin 1 is HV_{OUT}20.
For DIR = H, pin 1 is HV_{OUT}21.
Pins 65–80 are NC (ceramic only).

Package Outline



3-sided Plastic QFP 64-pin Gullwing Package



80-Pin Ceramic QFP Gullwing Package

32 MHz, 64-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options			
	80 Lead Quad Ceramic Gullwing	80 Lead Quad Plastic Gullwing	Die	80 Lead Quad Ceramic Gullwing (MIL-STD-883 Processed*)
HV77	HV7708DG	HV7708PG	HV7708X	RBHV7708DG
HV577	HV57708DG	HV57708PG	HV57708X	RBHV57708DG
HV79	HV7908DG	HV7908PG	HV7908X	RBHV7908DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ Processed with HVCMOS® technology
- ☐ 5V CMOS logic
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ 32MHz equivalent data rate
- ☐ Latched data outputs
- ☐ Forward and reverse shifting options (DIR pin)
- ☐ Diode to V_{PP} allows efficient power recovery
- ☐ Outputs may be hot switched
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7.5V
Output voltage, V_{PP}		-0.5V to +90V
Logic input levels		-0.3V to V_{DD} +0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range		0 to 85°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. Limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV77, HV577, and HV79 are low-voltage serial to high-voltage parallel converters with push-pull outputs. This device has been designed for use as a driver for electroluminescent displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 4 parallel 16-bit shift registers, permitting data rates 4X the speed of one (they are clocked together). There are also 64 latches and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout 64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latches is stored when $\overline{LE}$ is low.

The HV77 and HV577 have output sourcing/sinking current capability of ±15mA. The HV577 is a shrunk die version of HV77 and is recommended for all new designs requiring ±15mA. The HV79 has higher output sink/source current of ±40mA.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter			Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current				15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current				100	µA	Outputs high
					100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current				100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High-level output	HV_{OUT}	HV77/577	72		V	I_O= 15mA, V_{PP} = 80V
		HV_{OUT}	HV79	60		V	I_O = 40mA, V_{PP} = 80
		Data out		V_{DD} - 0.5		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}	HV77/577		8	V	I_O = -15mA, V_{PP} = 80V
		HV_{OUT}	HV79		20	V	I_O = -40mA, V_{PP} = 80V
		Data out			0.5	V	I_O= 100µA
I_{IH}	High-level logic input current				1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current				-1	µA	V_{IL} = 0V

AC Characteristics (T_A = 85°C max. Logic signal inputs and Data inputs have t_r, $t_f \le$ 5ns [10% and 90% points])

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	Per Register
t_{WL},t_{WH}	Clock width high or low	25		ns	
t_{SU}	Data set-up time before clock rises	10		ns	
t_H	Data hold time after clock rises	15		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low		70	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		70	ns	C_L = 15pF
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	25		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0		ns	

* t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).

Recommended Operating Conditions

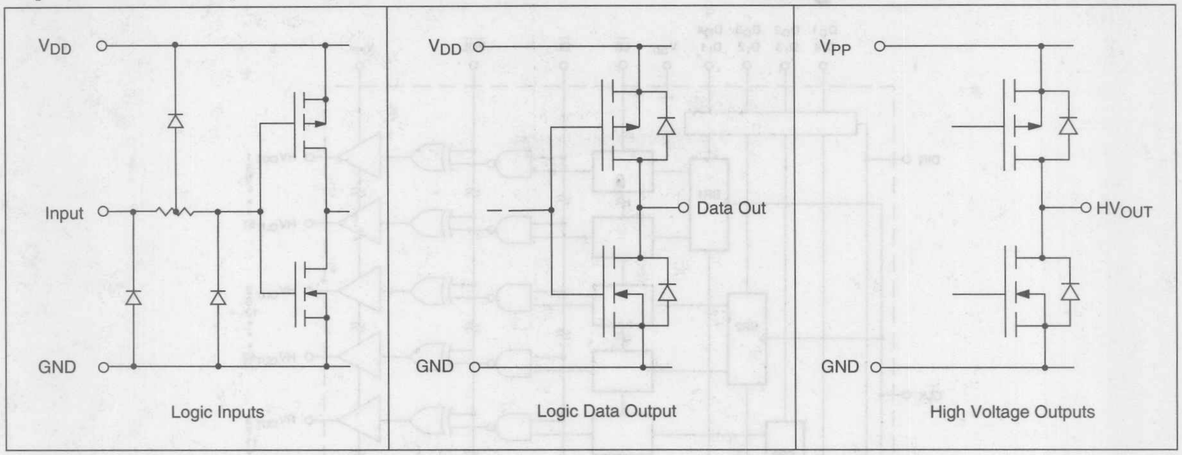
Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
V_{PP}	Output voltage		8	80	V
V_{IH}	High-level input voltage		V_{DD} -0.5V		V
V_{IL}	Low-level input voltage		0	0.5	V
f_{CLK}	Clock frequency per register			8	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	

Note: Power-up sequence should be the following:

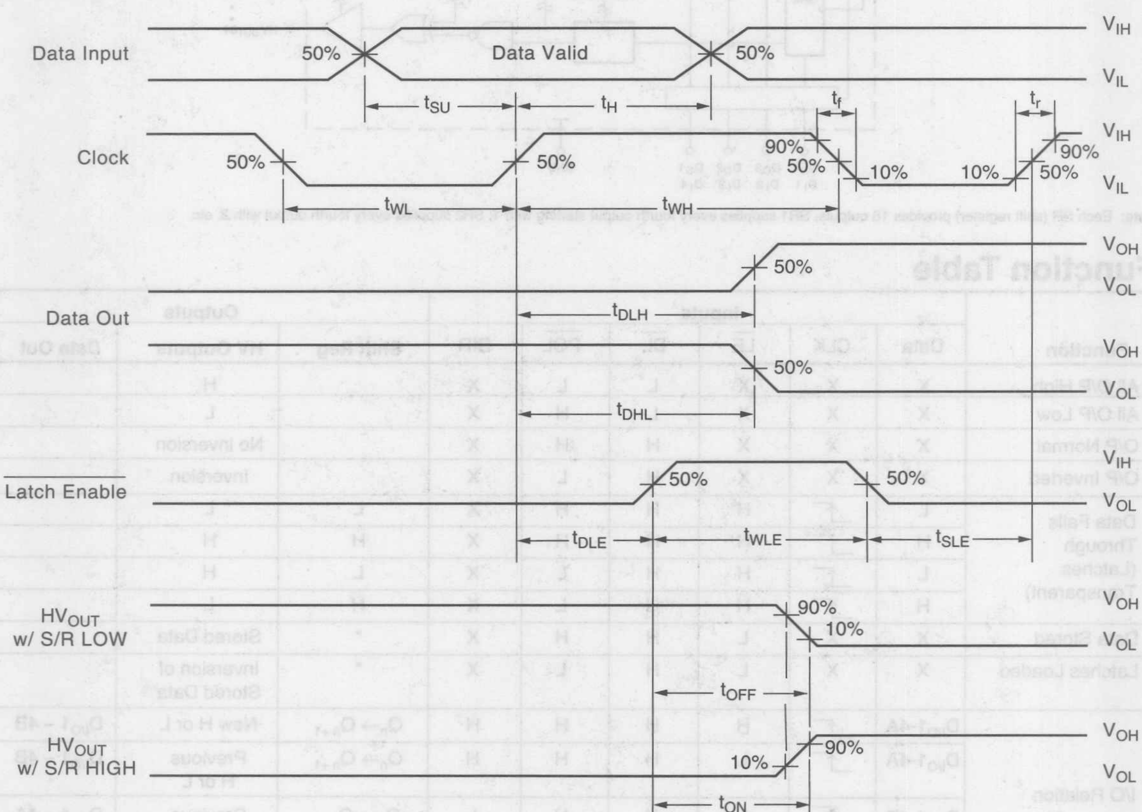
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.
The V_{PP} should not drop below V_{DD} during operations.

Input and Output Equivalent Circuits



Switching Waveforms



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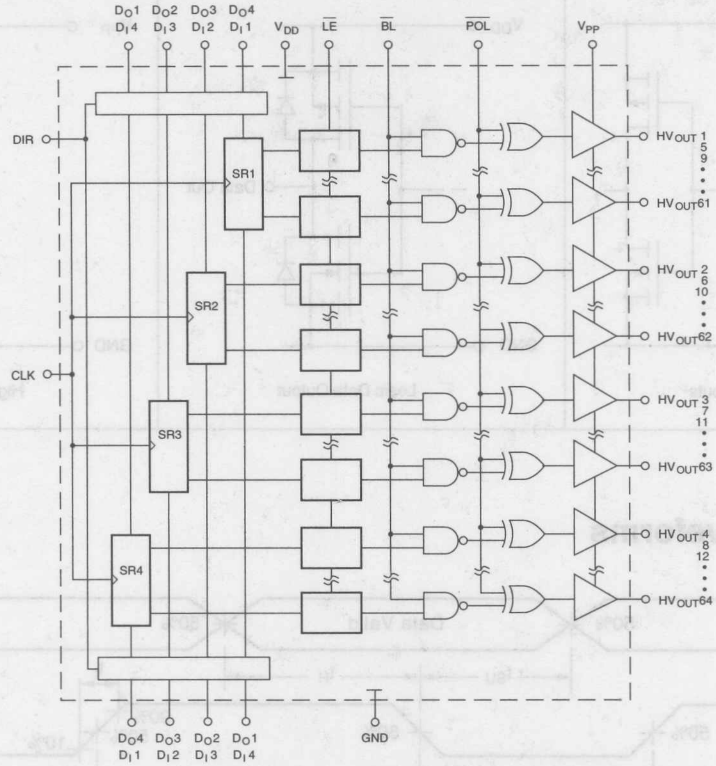
Functional Block Diagram



Note: Each SR (shift register) provides 16 outputs. SR1 supplies every fourth output starting with 1; SR2 supplies every fourth output with 2, etc.

Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P High	X	X	X	L	L	X		H	
All O/P Low	X	X	X	L	H	X		L	
O/P Normal	X	X	X	H	H	X		No inversion	
O/P Inverted	X	X	X	H	L	X		Inversion	
Data Falls Through (Latches Transparent)	L	↑	H	H	H	X	L	L	
	H	↑	H	H	H	X	H	H	
	L	↑	H	H	L	X	L	H	
	H	↑	H	H	L	X	H	L	
Data Stored	X	X	L	H	H	X	*	Stored Data	
Latches Loaded	X	X	L	H	L	X	*	Inversion of Stored Data	
I/O Relation	$D_{I/O}$1-4A	↑	H	H	H	H	$Q_n \rightarrow Q_{n+1}$	New H or L	$D_{I/O}1 - 4B$
	$D_{I/O}$1-4A	↑	L	H	H	H	$Q_n \rightarrow Q_{n+1}$	Previous H or L	$D_{I/O}1 - 4B$
	$D_{I/O}$1-4B	↑	L	H	H	L	$Q_n \rightarrow Q_{n-1}$	Previous H or L	$D_{I/O}1 - 4A$
	$D_{I/O}$1-4B	↑	H	H	H	L	$Q_n \rightarrow Q_{n-1}$	New H or L	$D_{I/O}1 - 4A$

Notes: * = dependent on previous stage's state. See Pin configuration for D_{IN} and D_{OUT} pin designation for CW and CCW shift.

Pin Configurations

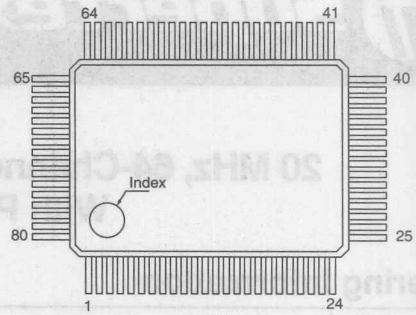
HV77/HV577/HV79

80-pin Gullwing

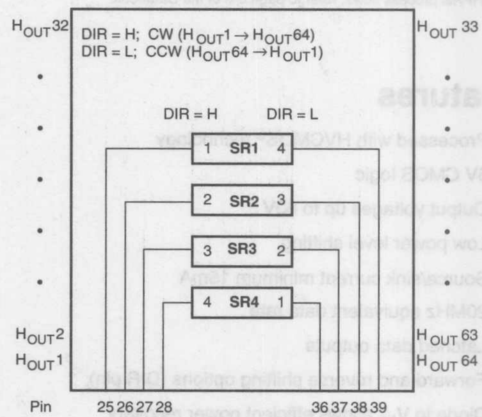
Pin	Function	Pin	Function
		40	V_{PP}
1	HV_{OUT} 24/41	41	HV_{OUT} 64/1
2	HV_{OUT} 23/42	42	HV_{OUT} 63/2
3	HV_{OUT} 22/43	43	HV_{OUT} 62/3
4	HV_{OUT} 21/44	44	HV_{OUT} 61/4
5	HV_{OUT} 20/45	45	HV_{OUT} 60/5
6	HV_{OUT} 19/46	46	HV_{OUT} 59/6
7	HV_{OUT} 18/47	47	HV_{OUT} 58/7
8	HV_{OUT} 17/48	48	HV_{OUT} 57/8
9	HV_{OUT} 16/49	49	HV_{OUT} 56/9
10	HV_{OUT} 15/50	50	HV_{OUT} 55/10
11	HV_{OUT} 14/51	51	HV_{OUT} 54/11
12	HV_{OUT} 13/52	52	HV_{OUT} 53/12
13	HV_{OUT} 12/53	53	HV_{OUT} 52/13
14	HV_{OUT} 11/54	54	HV_{OUT} 51/14
15	HV_{OUT} 10/55	55	HV_{OUT} 50/15
16	HV_{OUT} 9/56	56	HV_{OUT} 49/16
17	HV_{OUT} 8/57	57	HV_{OUT} 48/17
18	HV_{OUT} 7/58	58	HV_{OUT} 47/18
19	HV_{OUT} 6/59	59	HV_{OUT} 46/19
20	HV_{OUT} 5/60	60	HV_{OUT} 45/20
21	HV_{OUT} 4/61	61	HV_{OUT} 44/21
22	HV_{OUT} 3/62	62	HV_{OUT} 43/22
23	HV_{OUT} 2/63	63	HV_{OUT} 42/23
24	HV_{OUT} 1/64	64	HV_{OUT} 41/24
25	D_{IN} 1/D_{OUT} 4(A)	65	HV_{OUT} 40/25
26	D_{IN} 2/D_{OUT} 3(A)	66	HV_{OUT} 39/26
27	D_{IN} 3/D_{OUT} 2(A)	67	HV_{OUT} 38/27
28	D_{IN} 4/D_{OUT} 1(A)	68	HV_{OUT} 37/28
29	$\overline{LE}$	69	HV_{OUT} 36/29
30	CLK	70	HV_{OUT} 35/30
31	$\overline{BL}$	71	HV_{OUT} 34/31
32	V_{DD}	72	HV_{OUT} 33/32
33	DIR	73	HV_{OUT} 32/33
34	GND	74	HV_{OUT} 31/34
35	$\overline{POL}$	75	HV_{OUT} 30/35
36	D_{OUT} 4/D_{IN} 1(B)	76	HV_{OUT} 29/36
37	D_{OUT} 3/D_{IN} 2(B)	77	HV_{OUT} 28/37
38	D_{OUT} 2/D_{IN} 3(B)	78	HV_{OUT} 27/38
39	D_{OUT} 1/D_{IN} 4(B)	79	HV_{OUT} 26/39
		80	HV_{OUT} 25/40

Note: Pin designation for DIR = H/L.
Example: For DIR = H, pin 41 is HV_{OUT} 64.
For DIR = L, pin 41 is HV_{OUT} 1.
For CW/CCW Shift see function table $Q_N \rightarrow Q_N$+1.

Package Outline



top view
80-pin Gullwing Package



Supertex inc.

HV78

Product Objective Specification

20 MHz, 64-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options			
	80 Lead Quad Ceramic Gullwing	80 Lead Quad Plastic Gullwing	Die	80 Lead Quad Ceramic Gullwing (MIL-STD-883 Processed*)
HV78	HV7808DG	HV7808PG	HV7808X	RBHV7808DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS® technology
- 5V CMOS logic
- Output voltages up to 80V
- Low power level shifting
- Source/sink current minimum 15mA
- 20MHz equivalent data rate
- Latched data outputs
- Forward and reverse shifting options (DIR pin)
- Diode to V_{PP} allows efficient power recovery
- Outputs may be hot switched
- Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7.5V
Output voltage, V_{PP}		-0.5V to +90V
Logic input levels		-0.3V to V_{DD} +0.3V
Ground currrent[2]		1.5A
Continuous total power dissipation[3]	Ceramic Plastic	1500mW 1200mW
Operating temperature range		0 to 85°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. Limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV78 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for electroluminescent displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 2 parallel 32-bit shift registers, permitting data rates 2X the speed of one (they are clocked together). There are also 64 latches and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout 64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latches is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current			100	µA	Outputs high
				100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High-level output	HV_{OUT}	72		V	I_O= -15mA, V_{PP} = 80V
		Data out	V_{DD} - 0.5		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		8	V	I_O= 15mA, V_{PP} = 80V
		Data out		0.5	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

AC Characteristics (T_A = 85°C max. Logic signal inputs and Data inputs have t_r, $t_f \leq$ 5ns [10% and 90% points])

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	Per Register
t_{WL},t_{WH}	Clock width high or low	25		ns	
t_{SU}	Data set-up time before clock rises	10		ns	
t_H	Data hold time after clock rises	15		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low		70	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		70	ns	C_L = 15pF
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	25		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0		ns	

* t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).

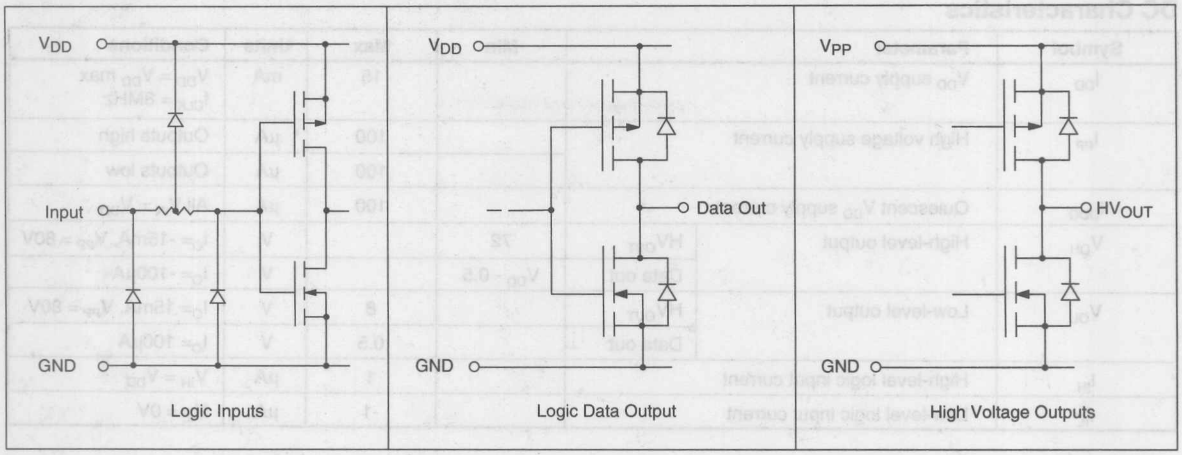
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
V_{PP}	Output voltage		8	80	V
V_{IH}	High-level input voltage		V_{DD} -0.5V		V
V_{IL}	Low-level input voltage		0	0.5	V
f_{CLK}	Clock frequency per register			12	MHz
T_A	Operating free-air temperature	Commercial	0	+70	°C
		Military Hi-Rel (RB)	-55	+125	

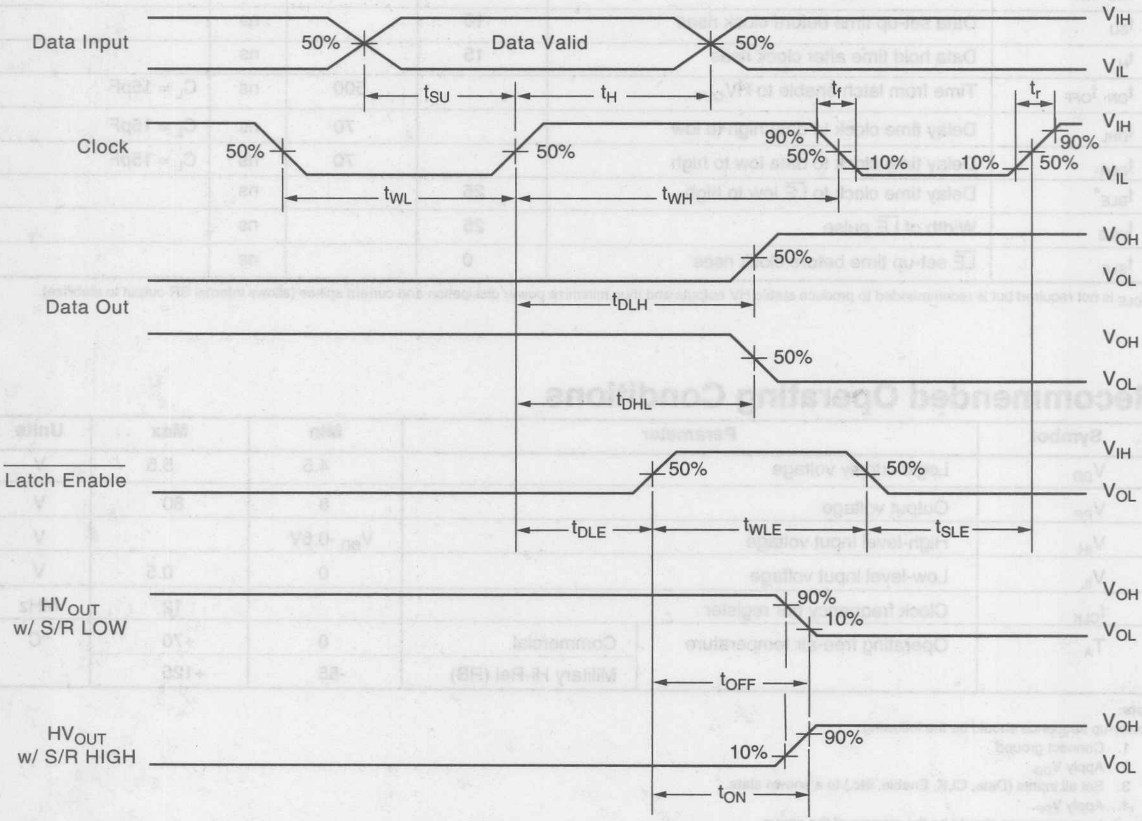
Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.
The V_{PP} should not drop below V_{DD} during operations.

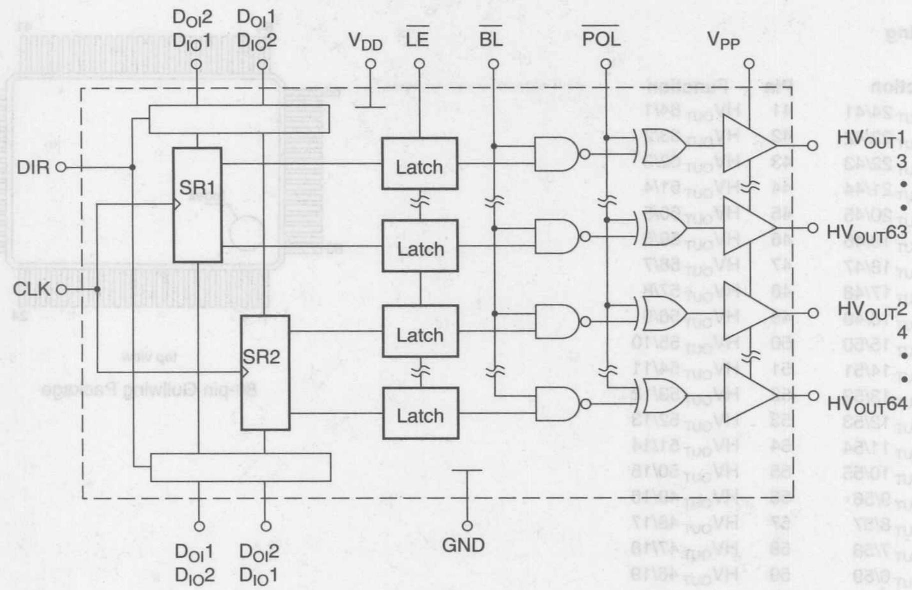
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P High	X	X	X	L	L	X		H	
All O/P Low	X	X	X	L	H	X		L	
O/P Normal	X	X	X	H	H	X		No inversion	
O/P Inverted	X	X	X	H	L	X		Inversion	
Data Falls Through (Latches Transparent)	L	↑	H	H	H	X	L	L	
	H	↑	H	H	H	X	H	H	
	L	↑	H	H	L	X	L	H	
	H	↑	H	H	L	X	H	L	
Data Stored	X	X	L	H	H	X	*	Stored Data	
Latches Loaded	X	X	L	H	L	X	*	Inversion of Stored Data	
I/O Relation	D_{OI}1-2A	↑	H	H	H	H	$Q_n \rightarrow Q_{n+1}$B	New H or L	D_{OI}1-2B
	D_{OI}1-2B	↑	L	H	H	L	$Q_n \rightarrow Q_{n+1}$A	Previous H or L	D_{OI}1-2A

Notes: * = dependent on previous stage's state.

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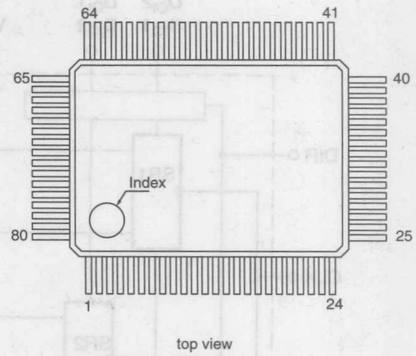
Pin Configurations

HV78
80-pin Gullwing

Pin	Function	Pin	Function
1	HV_{OUT} 24/41	41	HV_{OUT} 64/1
2	HV_{OUT} 23/42	42	HV_{OUT} 63/2
3	HV_{OUT} 22/43	43	HV_{OUT} 62/3
4	HV_{OUT} 21/44	44	HV_{OUT} 61/4
5	HV_{OUT} 20/45	45	HV_{OUT} 60/5
6	HV_{OUT} 19/46	46	HV_{OUT} 59/6
7	HV_{OUT} 18/47	47	HV_{OUT} 58/7
8	HV_{OUT} 17/48	48	HV_{OUT} 57/8
9	HV_{OUT} 16/49	49	HV_{OUT} 56/9
10	HV_{OUT} 15/50	50	HV_{OUT} 55/10
11	HV_{OUT} 14/51	51	HV_{OUT} 54/11
12	HV_{OUT} 13/52	52	HV_{OUT} 53/12
13	HV_{OUT} 12/53	53	HV_{OUT} 52/13
14	HV_{OUT} 11/54	54	HV_{OUT} 51/14
15	HV_{OUT} 10/55	55	HV_{OUT} 50/15
16	HV_{OUT} 9/56	56	HV_{OUT} 49/16
17	HV_{OUT} 8/57	57	HV_{OUT} 48/17
18	HV_{OUT} 7/58	58	HV_{OUT} 47/18
19	HV_{OUT} 6/59	59	HV_{OUT} 46/19
20	HV_{OUT} 5/60	60	HV_{OUT} 45/20
21	HV_{OUT} 4 /61	61	HV_{OUT} 44/21
22	HV_{OUT} 3/62	62	HV_{OUT} 43/22
23	HV_{OUT} 2/63	63	HV_{OUT} 42/23
24	HV_{OUT} 1/64	64	HV_{OUT} 41/24
25	D_{IO} 1/D_{OI} 2(A)	65	HV_{OUT} 40/25
26	D_{IO} 2/D_{OI} 1(A)	66	HV_{OUT} 39/26
27	NC	67	HV_{OUT} 38/27
28	NC	68	HV_{OUT} 37/28
29	$\overline{LE}$	69	HV_{OUT} 36/29
30	CLK	70	HV_{OUT} 35/30
31	$\overline{BL}$	71	HV_{OUT} 34/31
32	V_{DD}	72	HV_{OUT} 33/32
33	DIR	73	HV_{OUT} 32/33
34	GND	74	HV_{OUT} 31/34
35	$\overline{POL}$	75	HV_{OUT} 30/35
36	D_{OI} 2/D_{IO} 1(B)	76	HV_{OUT} 29/36
37	D_{OI} 1/D_{IO} 2(B)	77	HV_{OUT} 28/37
38	NC	78	HV_{OUT} 27/38
39	NC	79	HV_{OUT} 26/39
40	V_{PP}	80	HV_{OUT} 25/40

Note:
Pin designation for DIR = H/L.
Example: For DIR = H, pin 41 is HV_{OUT} 64.
For DIR = L, pin 41 is HV_{OUT} 1.
For CW/CCW Shift see function table for $Q_N \rightarrow Q_{N+1}$.

Package Outline



80-pin Gullwing Package

Supertex inc.

HV701
HV711

Product Objective Specifications

200V 40-Channel Vacuum-Fluorescent Display Driver

Ordering Information

Device	Package Options	
	60 Pin Plastic Gullwing	Die
HV701	HV701PG	HV701X
HV711	HV711PG	HV711X

Features

- ☐ 220V push-pull outputs
- ☐ 40 output lines
- ☐ 5V CMOS logic
- ☐ +2.5 / -10mA output sink/source
- ☐ Two 20-bit parallel shift registers
- ☐ 40-bit latch
- ☐ 60-pin 2-sided Gullwing
- ☐ 6MHz shift clock
- ☐ Processed with HVCMOS® technology

General Description

The HV701/711 are designed to drive vacuum fluorescent displays used in graphic applications. The 40 outputs are supplied by 40 output latches which are fed from two 20-bit shift registers that have been loaded in parallel from 2 data inputs. Data is shifted in on the HIGH-to-LOW clock transition. Logic control is provided by a latch enable (LE) and output clear ($\overline{CL}$). When $\overline{CL}$ is HIGH, data is reflected at the output; when $\overline{CL}$ is LOW all outputs are LOW. Pin assignments for the HV711 have pin reversed from the HV701 for ease in PC board layout.

Absolute Maximum Ratings

Supply voltage,[1] V_{DD}	-0.5V to +7V
Supply voltage,[1] V_{PP}	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} +0.5V
Continuous total power dissipation [2, 3]	800mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10 seconds	260°C

Notes:

1. All voltages referenced to GND
2. Duty cycle is limited by the total power dissipated in the package
3. For operation above 25°C ambient, derate linearly to 614mW/°C @ 6.4mW/°C.

Electrical Characteristics (V_{DD} = 5V, V_{PP} = 200V, T_A = -40°C to 85°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Logic supply current	I_{DD}	V_{DD} =5.5V	All outputs low			16.0	mA
		No load f_{CLK} = 6 MHz	All outputs low T_A = 25°C			12.0	mA
I_{DD} (quiesent)	I_{DDQ}	V_{DD} = 5.5V	All outputs high T_A = 25°C			100	µA
High voltage supply current	I_{PP}	V_{PP}=200V	All outputs low			250	µA
		No load	All outputs low T_A = 25°C			250	µA
			All outputs high T_A = 25°C			250	µA
High-level input voltage	V_{IH}		V_{DD} = 4.5V	3.6			V
			V_{DD} = 5.5V	4.4			V
Low-level input voltage	V_{IL}		V_{DD} = 4.5V			0.9	V
			V_{DD} = 5.5V			1.1	V
Input leak current	I_I	T_A =25°C				±1	µA
Input capacitance	C_I	T_A =25°C				25	pF
High-level data output voltage	V_{OH}	I_O = -0.1mA	V_{DD} = 4.5V	3.6			V
			V_{DD} = 5.5V	4.4			V
Low-level data output voltage	V_{OL}	I_O = +0.1mA	V_{DD} = 4.5V			0.9	V
			V_{DD} = 5.5V			1.1	V
High-level output voltage	V_{HVOH}	I_{HVO} = -1.0mA, T_A =25°C		198			V
Low-level output voltage	V_{HVOL}	I_{HVO} = +0.5mA, T_A =25°C				2.0	V
High-level output current	I_{HVOH}	V_{HVO} = 195V T_A =25°C		-10			mA
Low-level output current	I_{HVOL}	V_{HVO} = 10V, T_A =25°C		2.5			mA

Switching Characteristics (V_{DD} = 5V, V_{PP} = 200V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay time, clk to data out	t_{PD}	See Figure 1,2			150	ns
Delay time high voltage output, low to high	t_{DLH}	See Figure 1, 2,[1] Each HVO [2]			4.0	µs
Delay time high voltage output, high to low	t_{DHL}	See Figure 1, 2,[1] Each HVO [2]			0.3	µs
Transition time high voltage output, low to high	t_{TLH}	See Figure 1, 2,[1] Each HVO [2]			6.0	µs
Transition time high voltage output, high to low	t_{THL}	See Figure 1, 2,[1] Each HVO [2]			0.3	µs

Notes:

1. The values of t_{DLH} and t_{DHL} are the delay times from $\overline{CL}$.
2. High voltage output terminal.

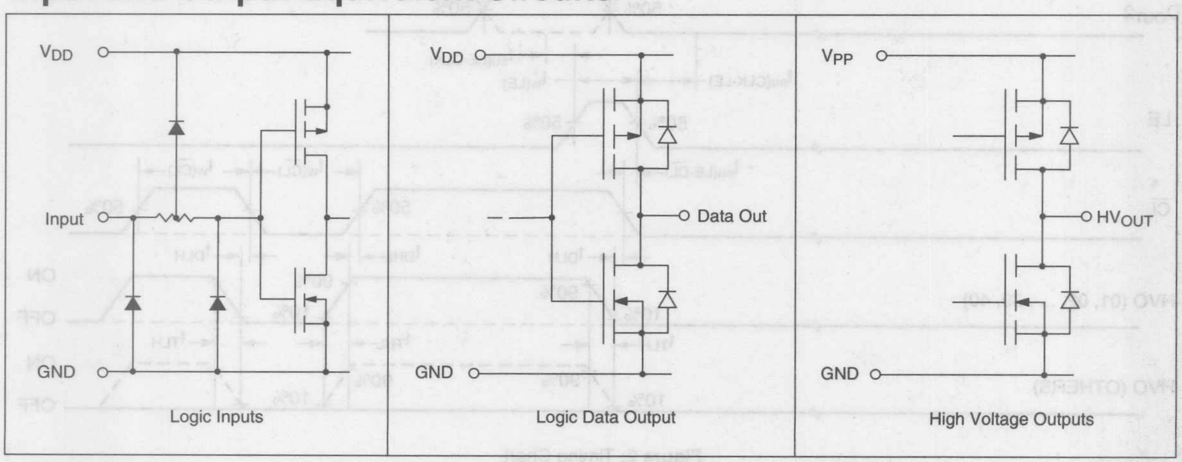
Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage	V_{DD}	Logic Supply	4.5	5.5	V
Supply voltage	V_{PP}	High voltage supply	25	200	V
High-level input voltage	V_{IH}	Each input, $V_{DD} = 4.5V$	3.6		V
		$V_{DD} = 5.5V$	4.4		V
Low-level input voltage	V_{IL}	Each input, $V_{DD} = 4.5$		0.9	V
		$V_{DD} = 5.5$		1.1	V
High-level output current	I_{HVOH}	Each HVO*		-10	mA
Low-level output current	I_{HVOL}	Each HVO*		2.5	mA
Clock frequency	f_{CLK}	Cascade		6.0	MHz
Clock pulse width	$t_{w(CLK)}$	See Figure 1, 2	70		ns
Data setup time	t_{su}	See Figure 1, 2	20		ns
Data hold time	t_h	See Figure 1, 2	45		ns
Data pulse width	$t_{w(D)}$	See Figure 1, 2	145		ns
Latch enable pulse width	$t_{w(LE)}$	See Figure 1, 2	80		ns
Data setup time CLK-LE	$t_{su(CLK\text{-}LE)}$	See Figure 1, 2	45		ns
Data setup time LE-CLK	$t_{su(LE\text{-}CLK)}$	See Figure 1, 2	10		ns
Data setup time LE-$\overline{CL}$	$t_{su(LE\text{-}\overline{CL})}$	See Figure 1, 2	10		µs
Clear pulse width	$t_{w(\overline{CL})}$	See Figure 1, 2	2		µs
Operating free-air temperature range	T_{ope}		-40	+85	°C

Note:
HVO*; High voltage output terminal
Power-up sequence should be the following:
1. Connect ground.
2. Apply VDD.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply VPP.

Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits



Logic Inputs | Logic Data Output | High Voltage Outputs

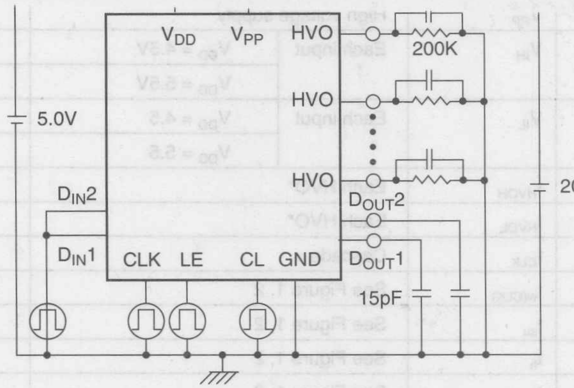


Figure 1: Test Circuit

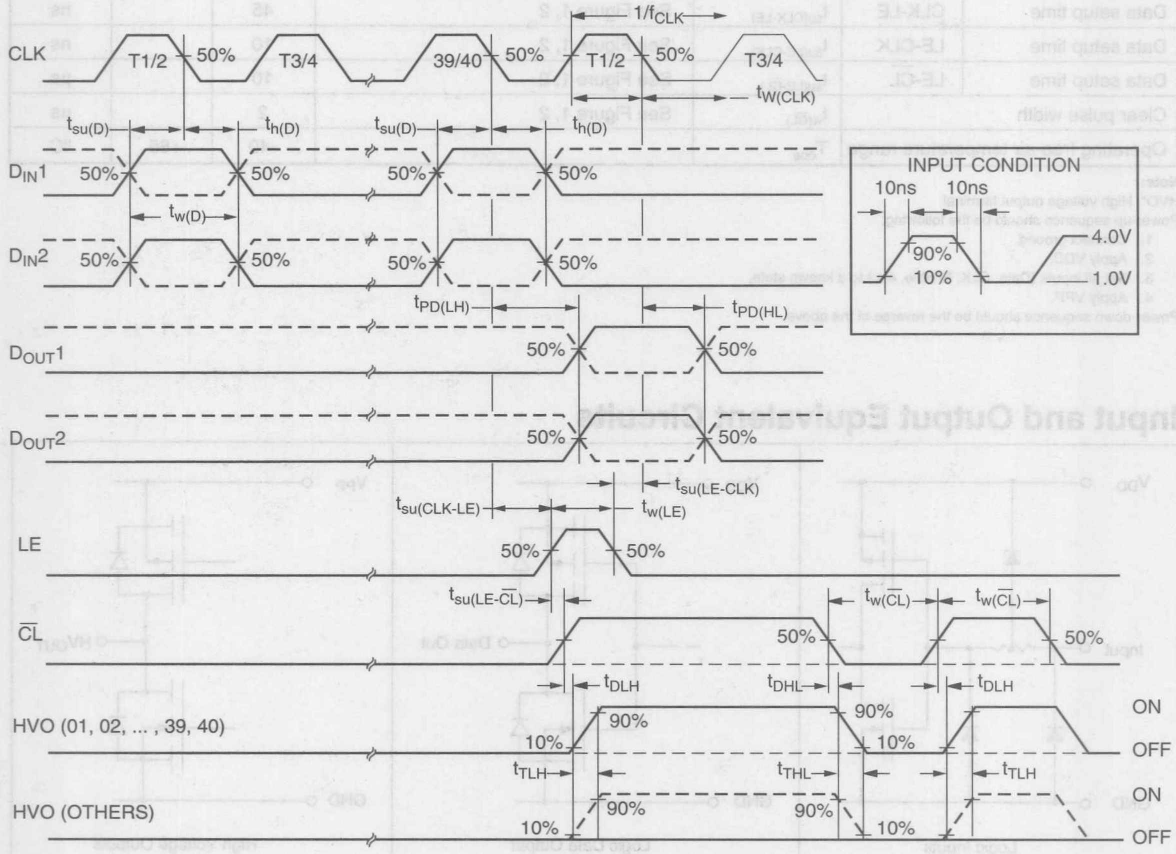
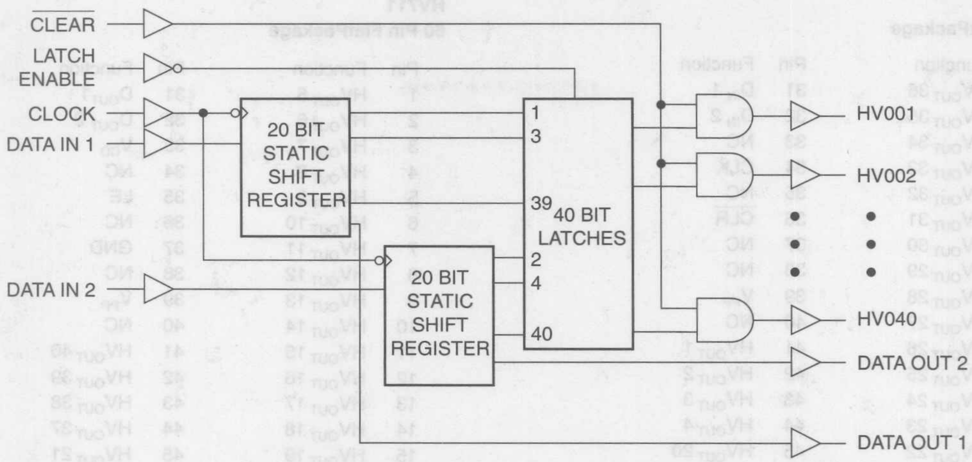


Figure 2: Timing Chart

Logic Diagram



Input Truth Table

CLK	Shift Register
⌐_	Data is Loaded
No Change	*

Output Truth Table

Data	LE	$\overline{CLR}$	Output
X	X	L	All O/P Low
H	H	H	High
L	H	H	Low
X	L	H	Previous Latch Data

Note:
High = high level, L = low level, X = high or low level,
⌐_ = high-to-low level transition
* Previous state

Pin Configurations

HV701
60 Pin FlatPackage

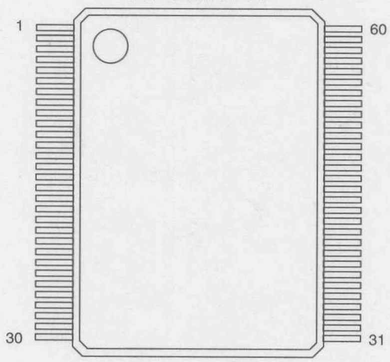
Pin	Function	Pin	Function
1	HV_{OUT} 36	31	D_{IN} 1
2	HV_{OUT} 35	32	D_{IN} 2
3	HV_{OUT} 34	33	NC
4	HV_{OUT} 33	34	CLK
5	HV_{OUT} 32	35	NC
6	HV_{OUT} 31	36	$\overline{CLR}$
7	HV_{OUT} 30	37	NC
8	HV_{OUT} 29	38	NC
9	HV_{OUT} 28	39	V_{PP}
10	HV_{OUT} 27	40	NC
11	HV_{OUT} 26	41	HV_{OUT} 1
12	HV_{OUT} 25	42	HV_{OUT} 2
13	HV_{OUT} 24	43	HV_{OUT} 3
14	HV_{OUT} 23	44	HV_{OUT} 4
15	HV_{OUT} 22	45	HV_{OUT} 20
16	HV_{OUT} 21	46	HV_{OUT} 19
17	HV_{OUT} 37	47	HV_{OUT} 18
18	HVout 38	48	HV_{OUT} 17
19	HV_{OUT} 39	49	HV_{OUT} 16
20	HV_{OUT} 40	50	HV_{OUT} 15
21	NC	51	HV_{OUT} 14
22	V_{PP}	52	HV_{OUT} 13
23	NC	53	HV_{OUT} 12
24	GND	54	HV_{OUT} 11
25	NC	55	HV_{OUT} 10
26	LE	56	HV_{OUT} 9
27	NC	57	HV_{OUT} 8
28	V_{DD}	58	HV_{OUT} 7
29	D_{OUT} 2	59	HV_{OUT} 6
30	D_{OUT} 1	60	HV_{OUT} 5

HV711
60 Pin FlatPackage

Pin	Function	Pin	Function
1	HV_{OUT} 5	31	D_{OUT} 1
2	HV_{OUT} 6	32	D_{OUT} 2
3	HV_{OUT} 7	33	V_{DD}
4	HV_{OUT} 8	34	NC
5	HV_{OUT} 9	35	LE
6	HV_{OUT} 10	36	NC
7	HV_{OUT} 11	37	GND
8	HV_{OUT} 12	38	NC
9	HV_{OUT} 13	39	V_{PP}
10	HV_{OUT} 14	40	NC
11	HV_{OUT} 15	41	HV_{OUT} 40
12	HV_{OUT} 16	42	HV_{OUT} 39
13	HV_{OUT} 17	43	HV_{OUT} 38
14	HV_{OUT} 18	44	HV_{OUT} 37
15	HV_{OUT} 19	45	HV_{OUT} 21
16	HV_{OUT} 20	46	HV_{OUT} 22
17	HV_{OUT} 4	47	HV_{OUT} 23
18	HV_{OUT} 3	48	HV_{OUT} 24
19	HV_{OUT} 2	49	HV_{OUT} 25
20	HV_{OUT} 1	50	HV_{OUT} 26
21	NC	51	HV_{OUT} 27
22	V_{PP}	52	HV_{OUT} 28
23	NC	53	HV_{OUT} 29
24	NC	54	HV_{OUT} 30
25	$\overline{CLR}$	55	HV_{OUT} 31
26	NC	56	HV_{OUT} 32
27	CLK	57	HV_{OUT} 33
28	NC	58	HV_{OUT} 34
29	D_{IN} 2	59	HV_{OUT} 35
30	D_{IN} 1	60	HV_{OUT} 36

Package Outline

HV701/HV711



top view

Supertex inc.

HV702
HV712

Product Objective Specifications

200V 40-Channel Vacuum-Fluorescent Display Driver

Ordering Information

Device	Package Options	
	60 Pin Plastic Gullwing	Die
HV702	HV702PG	HV702X
HV712	HV712PG	HV712X

Features

- ☐ 220V push-pull outputs
- ☐ 40 output lines
- ☐ 5V CMOS logic
- ☐ +2.5 / -10mA output sink/source
- ☐ 40-bit shift register
- ☐ 40-bit latch
- ☐ 60-pin 2-sided Gullwing
- ☐ 6MHz shift clock
- ☐ Processed with HVCMOS® technology

General Description

The HV702/712 are designed to drive vacuum fluorescent displays used in graphic applications. The 40 outputs are supplied by 40 output latches which are fed from a 40-bit shift register. Data is shifted in on the HIGH-to-LOW clock transition. Logic control is provided by a latch enable (LE) and output clear ($\overline{CL}$). When $\overline{CL}$ is HIGH, data is reflected at the output: when $\overline{CL}$ is LOW all outputs are LOW.

Pin assignments for the HV712 have pin reversed from the HV702 for ease in PC board layout.

Absolute Maximum Ratings

Supply voltage,[1] V_{DD}	-0.5V to +7V
Supply voltage,[1] V_{PP}	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} +0.5V
Continuous total power dissipation [2, 3]	800mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10 seconds	260°C

Notes:
1. All voltages referenced to GND
2. Duty cycle is limited by the total power dissipated in the package
3. For operation above 25°C ambient, derate linearly to 614mW/°C @ 6.4mW/°C.

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Logic supply current	I_{DD}	V_{DD} =5.5V	All outputs low			[illegible]	mA
		No load f_{CLK} = 6MHz	All outputs low T_A = 25°C			12.0	mA
I_{DD} (quiescent)	I_{DDQ}	V_{DD} = 5.5V T_A = 25°C	All outputs high			100	µA
High voltage supply current	I_{PP}	V_{PP}=200V No load	All outputs low			250	µA
		T_A = 25°C	All outputs low			250	µA
		T_A = 25°C	All outputs high			250	µA
High-level input voltage	V_{IH}		V_{DD} = 4.5V	3.6			V
			V_{DD} = 5.5V	4.4			V
Low-level input voltage	V_{IL}		V_{DD} = 4.5V			0.9	V
			V_{DD} = 5.5V			1.1	V
Input leak current	I_I	T_A =25°C				±1	µA
Input capacitance	C_I	T_A =25°C				25	pF
High-level data output voltage	V_{OH}	I_O = -0.1mA	V_{DD} = 4.5V	3.6			V
			V_{DD} = 5.5V	4.4			V
Low-level data output voltage	V_{OL}	I_O = +0.1mA	V_{DD} = 4.5V			0.9	V
			V_{DD} = 5.5V			1.1	V
High-level output voltage	V_{HVOH}	I_{HVO} = -1.0mA, T_A =25°C		198			V
Low-level output voltage	V_{HVOL}	I_{HVO} = +0.5mA, T_A =25°C				2.0	V
High-level output current	I_{HVOH}	V_{HVO} = 195V T_A =25°C		-10			mA
Low-level output current	I_{HVOL}	V_{HVO} = 10V, T_A =25°C		2.5			mA

Switching Characteristics (V_{DD} = 5V, V_{PP} = 200V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay time, clk to data out	t_{PD}	See Figure 1,2			150	ns
Delay time high voltage output, low to high	t_{DLH}	See Figure 1, 2,[1] Each HVO [2]			4.0	µs
Delay time high voltage output, high to low	t_{DHL}	See Figure 1, 2,[1] Each HVO [2]			0.3	µs
Transition time high voltage output, low to high	t_{TLH}	See Figure 1, 2,[1] Each HVO [2]			6.0	µs
Transition time high voltage output, high to low	t_{THL}	See Figure 1, 2,[1] Each HVO [2]			0.3	µs

Notes:

1. The values of t_{DLH} and t_{DHL} are the delay times from $\overline{CL}$.
2. High voltage output terminal.

Recommended Operating Conditions

Parameter		Symbol	Conditions		Min	Max	Unit
Supply voltage		V_{DD}	Logic Supply		4.5	5.5	V
Supply voltage		V_{PP}	High voltage supply		25	200	V
High-level input voltage		V_{IH}	Each input	$V_{DD} = 4.5V$	3.6		V
				$V_{DD} = 5.5V$	4.4		V
Low-level input voltage		V_{IL}	Each input	$V_{DD} = 4.5$		0.9	V
				$V_{DD} = 5.5$		1.1	V
High-level output current		I_{HVOH}	Each HVO*			-10	mA
Low-level output current		I_{HVOL}	Each HVO*			2.5	mA
Clock frequency		f_{CLK}	Cascade			6.0	MHz
Clock pulse width		$t_{w(CLK)}$	See Figure 1, 2		70		ns
Data setup time		t_{su}	See Figure 1, 2		20		ns
Data hold time		t_h	See Figure 1, 2		45		ns
Data pulse width		$t_{w(D)}$	See Figure 1, 2		145		ns
Latch enable pulse width		$t_{w(LE)}$	See Figure 1, 2		80		ns
Data setup time	CLK-LE	$t_{su(CLK-LE)}$	See Figure 1, 2		45		ns
Data setup time	LE-CLK	$t_{su(LE-CLK)}$	See Figure 1, 2		10		ns
Data setup time	LE-$\overline{CL}$	$t_{su(LE-\overline{CL})}$	See Figure 1, 2		10		µs
Clear pulse width		$t_{w(\overline{CL})}$	See Figure 1, 2		2		µs
Operating free-air temperature range		T_{ope}			-40	+85	°C

Note:
HVO*; High voltage output terminal
Power-up sequence should be the following:
1. Connect ground.
2. Apply VDD.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply VPP.

Power-down sequence should be the reverse of the above.

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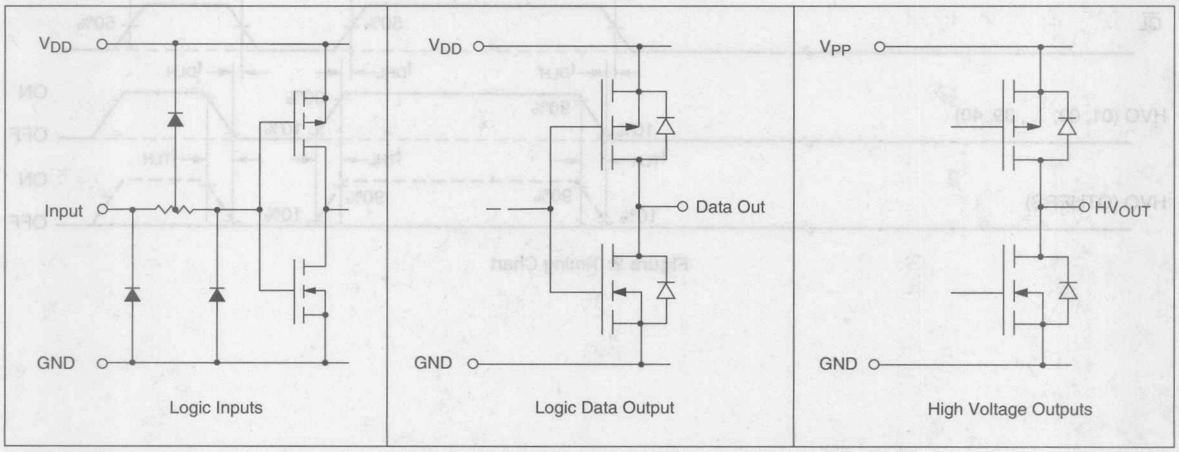
Input and Output Equivalent Circuits



Parameter Measurement Information

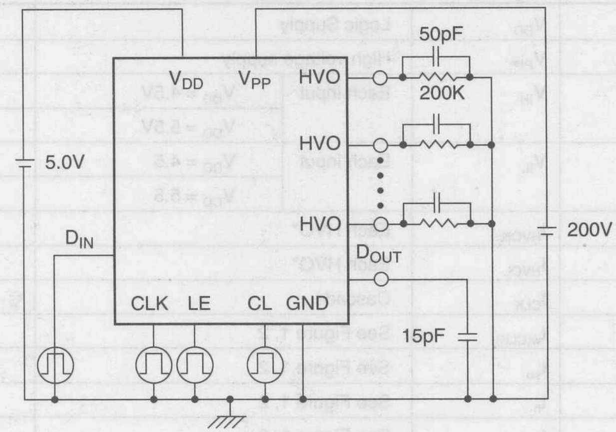


Figure 1: Test Circuit

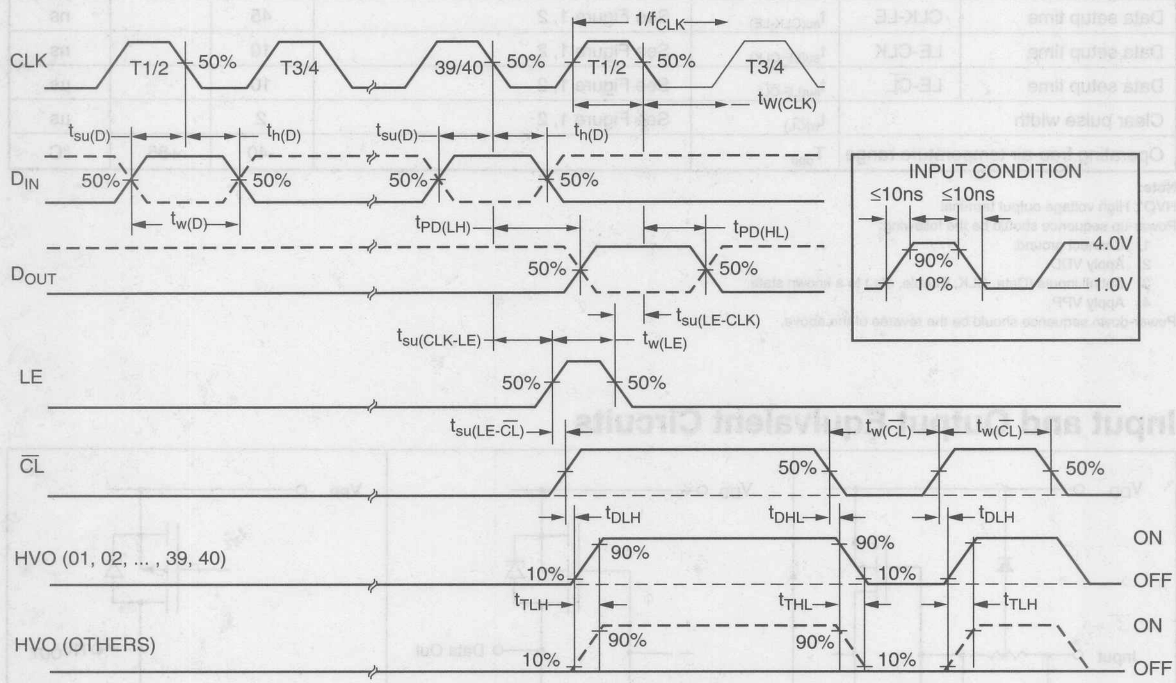
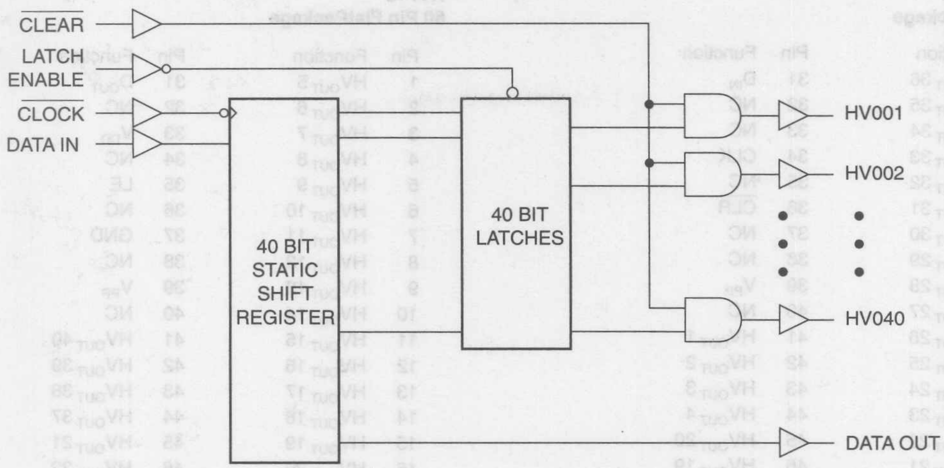


Figure 2: Timing Chart

Logic Diagram



Input Truth Table

CLK	Shift Register
⌐L (high-to-low transition)	Data is Loaded
No Change	*

Output Truth Table

Data	LE	$\overline{CLR}$	Output
X	X	L	All O/P Low
H	H	H	High
L	H	H	Low
X	L	H	Previous Latch Data

Note:
High = high level, L = low level, X = high or low level,
⌐L = high-to-low level transition
* Previous state

Pin Configurations

HV702
60 Pin FlatPackage

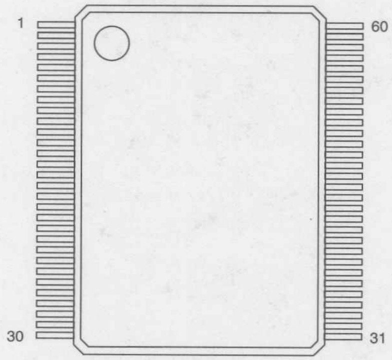
Pin	Function	Pin	Function
1	HV_{OUT} 36	31	D_{IN}
2	HV_{OUT} 35	32	NC
3	HV_{OUT} 34	33	NC
4	HV_{OUT} 33	34	CLK
5	HV_{OUT} 32	35	NC
6	HV_{OUT} 31	36	$\overline{CLR}$
7	HV_{OUT} 30	37	NC
8	HV_{OUT} 29	38	NC
9	HV_{OUT} 28	39	V_{PP}
10	HV_{OUT} 27	40	NC
11	HV_{OUT} 26	41	HV_{OUT} 1
12	HV_{OUT} 25	42	HV_{OUT} 2
13	HV_{OUT} 24	43	HV_{OUT} 3
14	HV_{OUT} 23	44	HV_{OUT} 4
15	HV_{OUT} 22	45	HV_{OUT} 20
16	HV_{OUT} 21	46	HV_{OUT} 19
17	HV_{OUT} 37	47	HV_{OUT} 18
18	HV_{OUT} 38	48	HV_{OUT} 17
19	HV_{OUT} 39	49	HV_{OUT} 16
20	HV_{OUT} 40	50	HV_{OUT} 15
21	NC	51	HV_{OUT} 14
22	V_{PP}	52	HV_{OUT} 13
23	NC	53	HV_{OUT} 12
24	GND	54	HV_{OUT} 11
25	NC	55	HV_{OUT} 10
26	LE	56	HV_{OUT} 9
27	NC	57	HV_{OUT} 8
28	V_{DD}	58	HV_{OUT} 7
29	NC	59	HV_{OUT} 6
30	D_{OUT}	60	HV_{OUT} 5

HV712
60 Pin FlatPackage

Pin	Function	Pin	Function
1	HV_{OUT} 5	31	D_{OUT}
2	HV_{OUT} 6	32	NC
3	HV_{OUT} 7	33	V_{DD}
4	HV_{OUT} 8	34	NC
5	HV_{OUT} 9	35	LE
6	HV_{OUT} 10	36	NC
7	HV_{OUT} 11	37	GND
8	HV_{OUT} 12	38	NC
9	HV_{OUT} 13	39	V_{PP}
10	HV_{OUT} 14	40	NC
11	HV_{OUT} 15	41	HV_{OUT} 40
12	HV_{OUT} 16	42	HV_{OUT} 39
13	HV_{OUT} 17	43	HV_{OUT} 38
14	HV_{OUT} 18	44	HV_{OUT} 37
15	HV_{OUT} 19	45	HV_{OUT} 21
16	HV_{OUT} 20	46	HV_{OUT} 22
17	HV_{OUT} 4	47	HV_{OUT} 23
18	HV_{OUT} 3	48	HV_{OUT} 24
19	HV_{OUT} 2	49	HV_{OUT} 25
20	HV_{OUT} 1	50	HV_{OUT} 26
21	NC	51	HV_{OUT} 27
22	V_{PP}	52	HV_{OUT} 28
23	NC	53	HV_{OUT} 29
24	NC	54	HV_{OUT} 30
25	$\overline{CLR}$	55	HV_{OUT} 31
26	NC	56	HV_{OUT} 32
27	CLK	57	HV_{OUT} 33
28	NC	58	HV_{OUT} 34
29	NC	59	HV_{OUT} 35
30	D_{IN}	60	HV_{OUT} 36

Package Outline

HV702/HV712



top view

Supertex inc.

HV83
HV84

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

		Package Options		
Device	Recommended Operating V_{PP} max	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Dice in waffle pack
HV83	80V	HV8308DJ	HV8308PJ	HV8308X
HV84	80V	HV8408DJ	HV8408PJ	HV8408X

Features

- ☐ Processed with HVCMOS® technology
- ☐ CMOS compatible inputs
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +15V
Supply voltage, V_{PP}		-0.5V to +80V
Logic input levels[2]		-0.5 to V_{DD} + 0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Plastic Ceramic	1200mW 1500mW
Operating temperature range	Commercial Military	-40°C to +85°C -55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV83 and HV84 are low voltage serial to high voltage parallel converters wtih push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. $HV_{OUT}1$ is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV84 shifts in the counterclockwise direction when viewed from the top of the package and the HV83 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

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Electrical Characteristics (V_{PP} = 60V, V_{DD} = 12V, T_A =25°C)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PP}	V_{PP} Supply Current		100	µA	HV_{OUT} outputs HIGH to LOW
I_{DDQ}	I_{DD} Supply Current (Quiescent)		100	µA	All inputs = V_{DD} or GND
I_{DD}	I_{DD} Supply Current (Operating)		15	mA	V_{DD} = V_{DD} max, f_{CLK} = 8 MHz
V_{OH} (Data)	Shift Register Output Voltage	11.5		V	I_O = -100µA
V_{OL} (Data)	Shift Register Output Voltage		0.5	V	I_O = 100µA
I_{IH}	Current Leakage, any input		1	µA	Input = V_{DD}
I_{IL}	Current Leakage, any input		-1	µA	Input = GND
V_{OC}	HV_{OUT} Output Clamp Diode Voltage		-1.5	V	I_{OL} = -100mA
V_{OH}	HV_{OUT} Output when Sourcing	52		V	I_{OH} = -20mA, 0 to 70°C
V_{OL}	HV_{OUT} Output when Sinking		8	V	I_{OL} = 20mA, 0 to 70°C

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock Frequency		8	MHz	
t_{WL} or t_{WH}	Clock width, HIGH or LOW	62		ns	
t_{SU}	Setup time before CLK rises	25		ns	
t_H	Hold time after CLK rises	10		ns	
t_{DLH} (Data)	Data Output Delay after L to H CLK		110	ns	C_L = 15pF
t_{DHL} (Data)	Data Output Delay after H to L CLK		110	ns	C_L = 15pF
t_{DLE}	LE Delay after L to H CLK	50		ns	
t_{WLE}	Width of LE Pulse	50		ns	
t_{SLE}	LE Setup Time before L to H CLK	50		ns	
t_{ON}	Delay from LE to HV_{OUT}, L to H		500	ns	
t_{OFF}	Delay from LE to HV_{OUT}, H to L		500	ns	

Recommended Operating Conditions

(over 0 to 70°C for commercial temperature range and -40°C to 85°C for industrial)

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Logic Voltage Supply	10.8	13.2	V	
V_{PP}	High Voltage Supply	8.0	80	V	HV8308 and HV8408
V_{IH}	Input HIGH Voltage	V_{DD}-2.0	V_{DD}	V	
V_{IL}	Input LOW Voltage	0	2.0	V	
f_{CLK}	Clock Frequency	0	8	MHz	

Note:

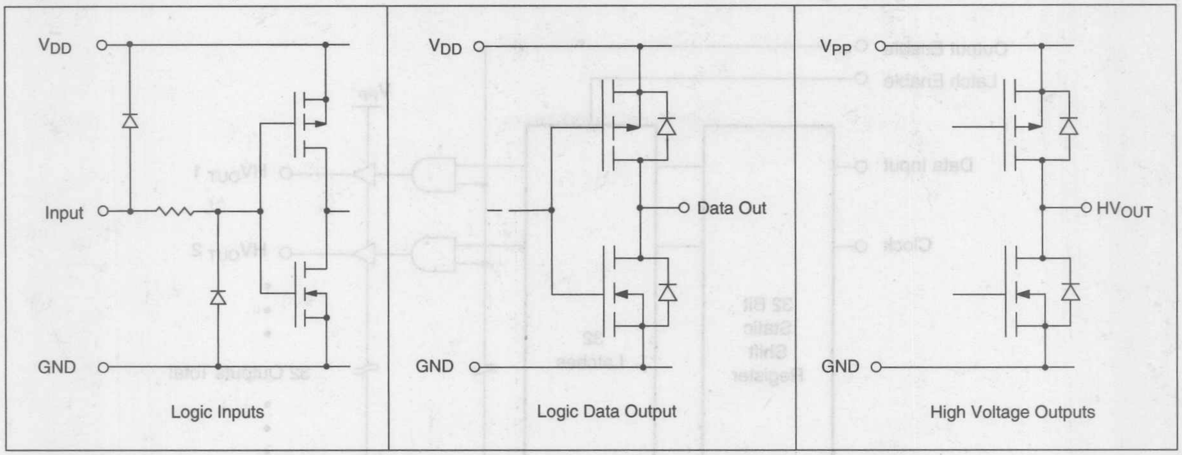
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

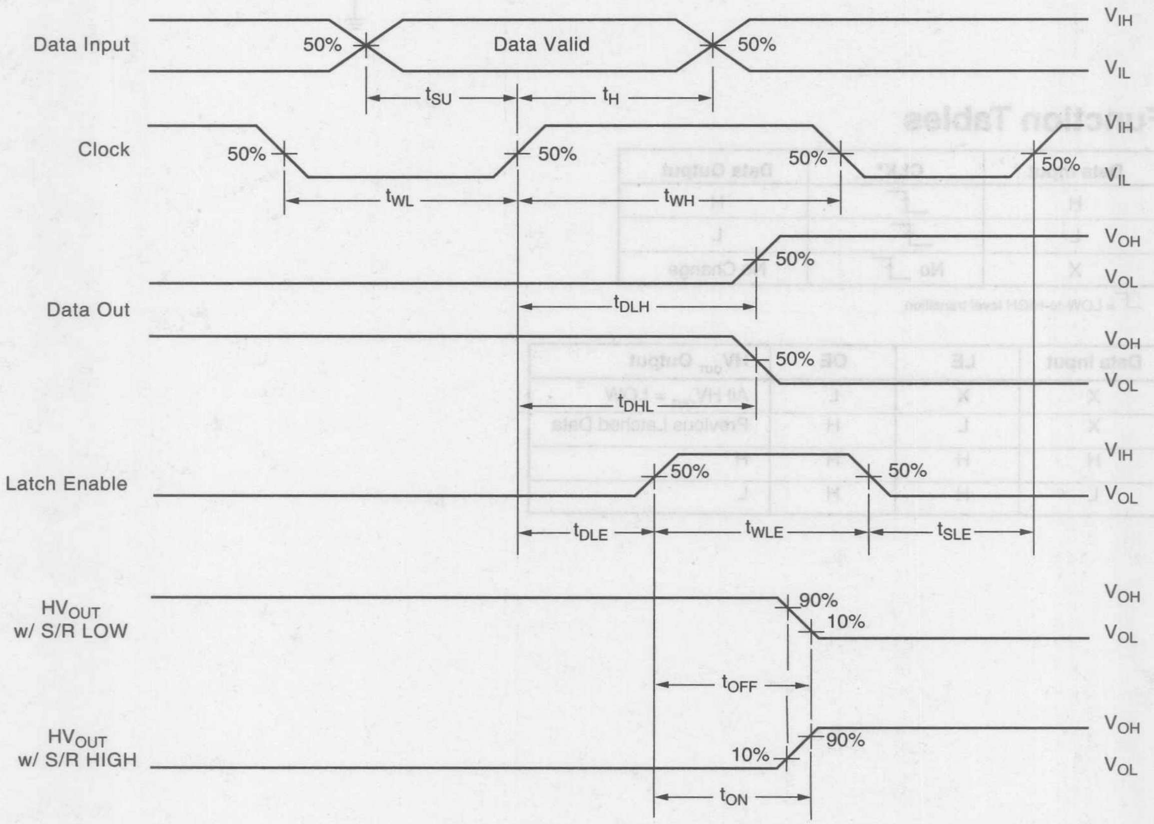
Power-down sequence should be the reverse of the above.

5. V_{PP} is not allowed to float during operation.
6. The V_{PP} should not drop below V_{DD} during operations.

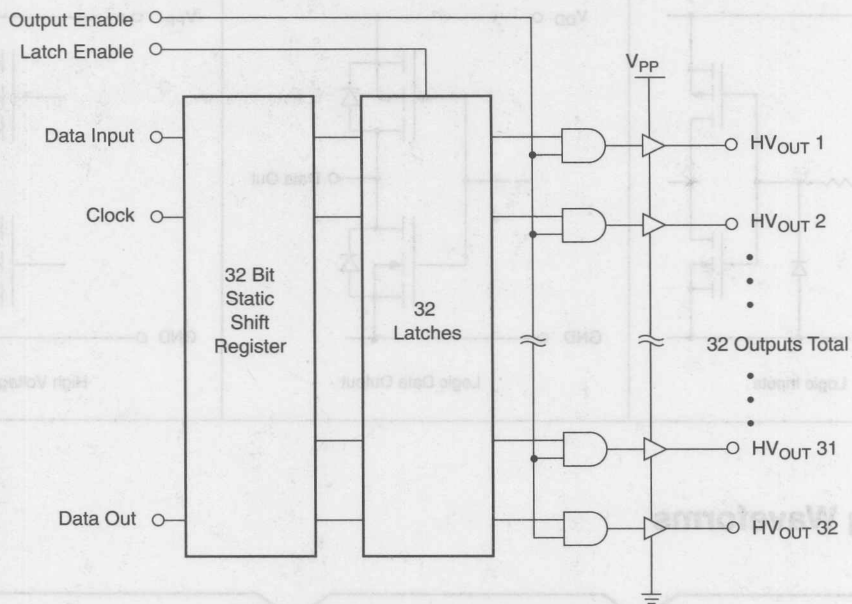
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Tables

Data Input	CLK*	Data Output
H	↑	H
L	↑	L
X	No ↑	No Change

* ↑ = LOW-to-HIGH level transition

Data Input	LE	OE	HV_{OUT} Output
X	X	L	All HV_{OUT} = LOW
X	L	H	Previous Latched Data
H	H	H	H
L	H	H	L

Pin Configuration

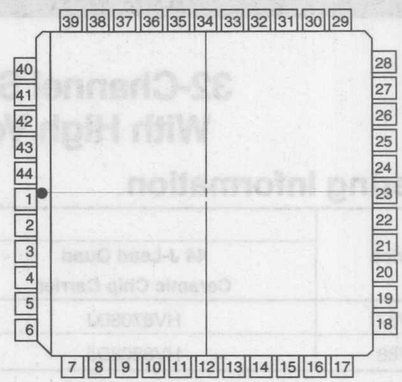
HV83
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Output Enable
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HV_{OUT} 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	N/C	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

HV84
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Output Enable
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	N/C	43	HV_{OUT} 14
22	Clock	44	HV_{OUT} 15

Package Outline



top view

44-pin J-Lead Package

Supertex inc.

HV87
HV88

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV87	HV8708DJ	HV8708PJ	HV8708X
HV88	HV8808DJ	HV8808PJ	HV8808X

Features

- ☐ Processed with HVCMOS® technology
- ☐ CMOS compatible outputs
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +15V
Output voltage, V_{PP}		-0.5V to +80V
Logic input levels[2]		-0.5V to V_{DD} +0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV87 and HV88 are low-voltage serial to high-voltage parallel converters wtih push-pull outputs.These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays. The inputs are fully CMOS compatible.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV87 shifts data in the clockwise direction when viewed from the top of the package and the HV88 shifts in the counterclockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HV_{OUT}32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current			100	µA	Outputs high
				100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	HV_{OUT}	52		V	I_O= -20mA
		Data out	10		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		8	V	I_O= 20mA
		Data out		1.0	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

AC Characteristics (V_{DD} = 5V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	10		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	50		ns	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	Output off voltage		8	75	V
V_{IH}	High-level input voltage		V_{DD} -2.0V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	-4.0	+85	°C

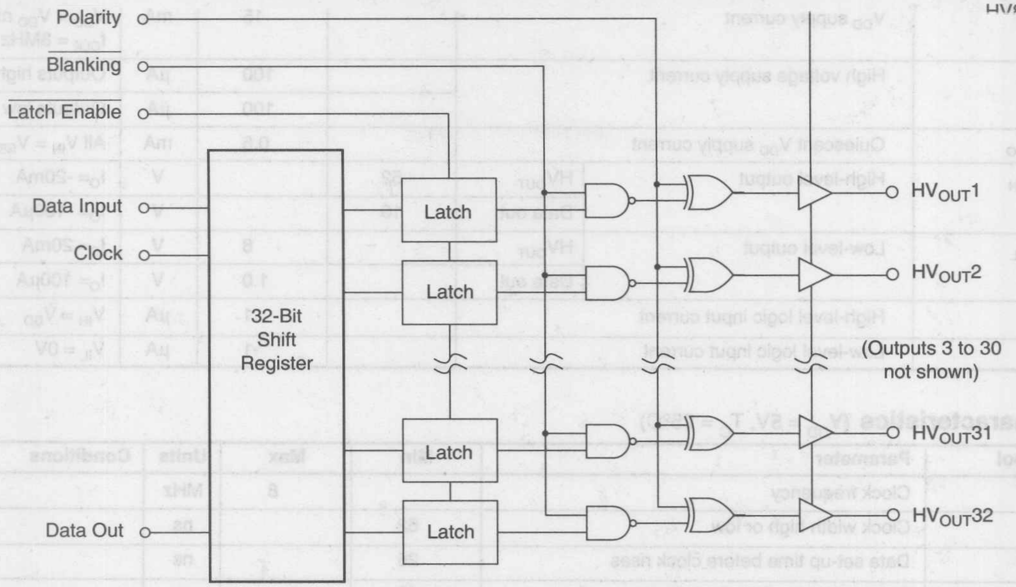
Note:

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

5. V_{PP} is not allowed to float during operation.
6. The V_{PP} should not drop below V_{DD} during operations.

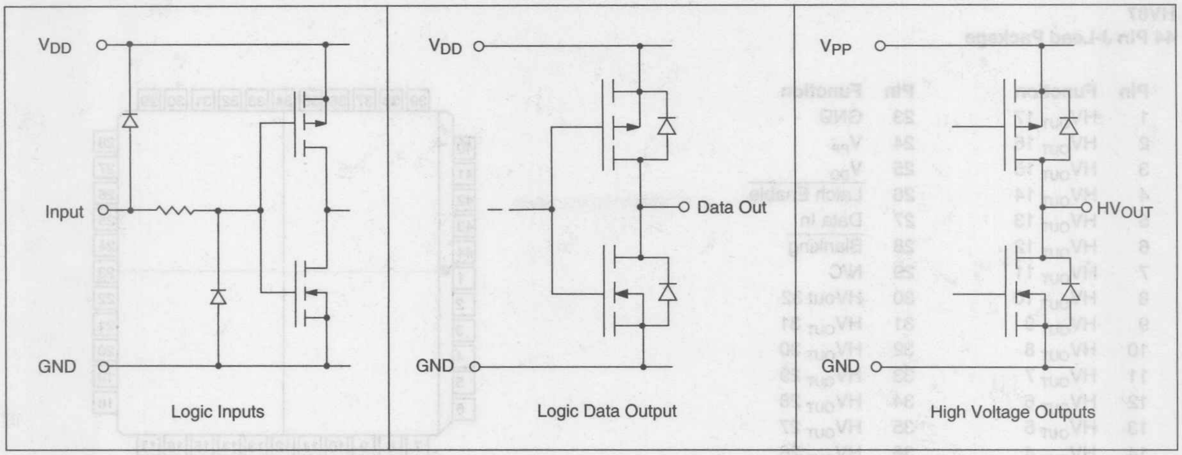


Function Table

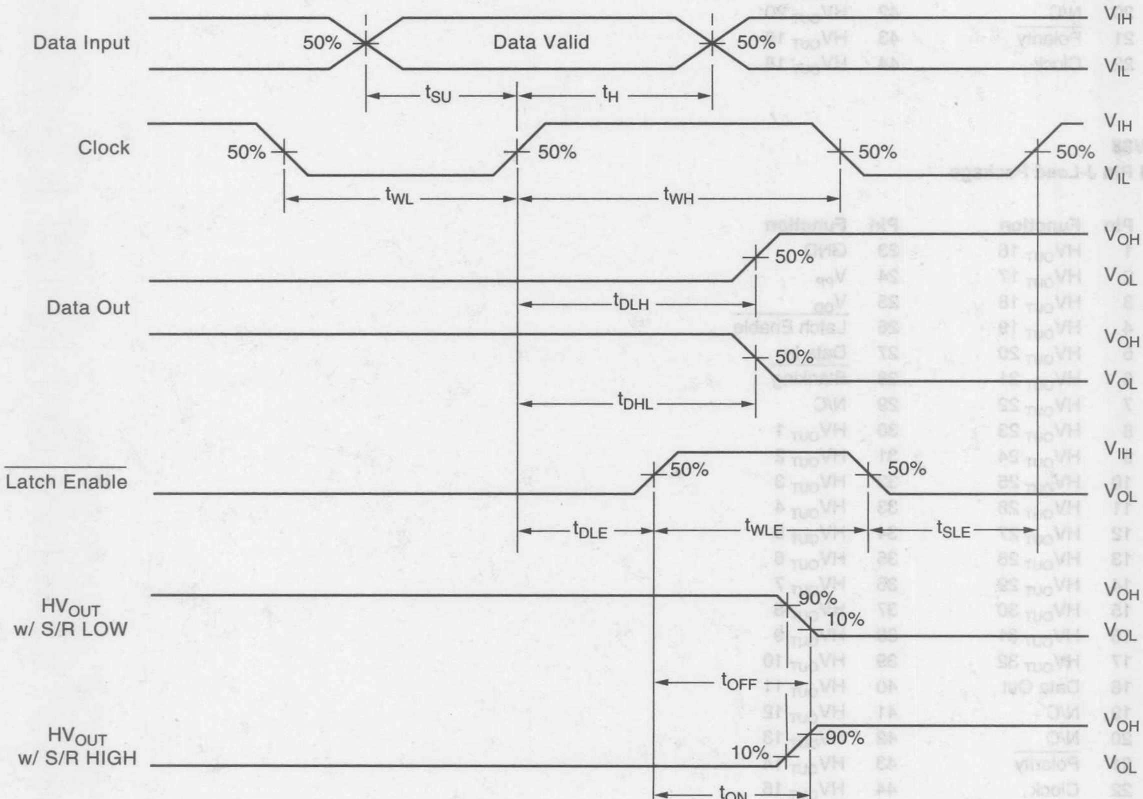
Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out
All on	X	X	X	L	L	*	*…*	H	H…H	*
All off	X	X	X	L	H	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*…*	*	*…*	*
Load latches	X	H or L	↑	H	H	*	*…*	*	*…*	*
	X	H or L	↑	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Transparent latch mode	L	↑	H	H	H	L	*…*	L	*…*	*
	H	↑	H	H	H	H	*…*	H	*…*	*

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last LE high.

Input and Output Equivalent Circuits



Switching Waveforms



Pin Configurations

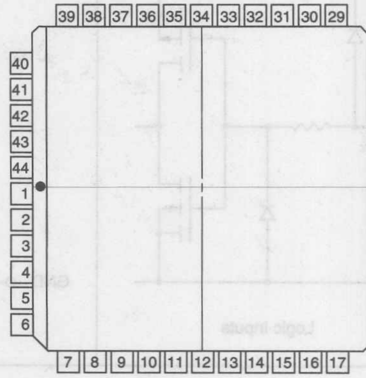
HV87
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Blanking
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HVout 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	Polarity	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

HV88
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Blanking
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	Polarity	43	HV_{OUT} 14
22	Clock	44	HV_{OUT} 15

Package Outline



top view

44-pin J-Lead Package

Supertex inc.

HV93
HV94

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options			
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Dice in Waffle Pack	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD883 processed*)
HV93	80V	HV9308DJ	HV9308PJ	HV9308X	RBHV9308DJ
HV94	80V	HV9408DJ	HV9408PJ	HV9408X	RBHV9408DJ

*For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- ☐ Processed with HVCMOS® technology
- ☐ Low power level shifting
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ 5V CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery
- ☐ 44-lead ceramic surface mount package
- ☐ Hi-Rel processing available

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +7V
Supply voltage, V_{PP}		-0.5V to +80V
Logic input levels[2]		-0.5 to V_{DD} + 0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Plastic Ceramic	1200mW 1500mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extrenes.
2. All voltages are referenced to V_{SS}.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV93 and HV94 are low voltage serial to high voltage parallel converters wtih push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. $HV_{OUT}1$ is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV94 shifts in the counterclockwise direction when viewed from the top of the package and the HV93 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

Electrical Characteristics (V_{PP} = 60V, V_{DD} = 5V, T_A =25°C)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PP}	V_{PP} Supply Current		100	µA	HV_{OUT} outputs HIGH to LOW
I_{DDQ}	I_{DD} Supply Current (Quiescent)		100	µA	All inputs = V_{DD} or GND
I_{DD}	I_{DD} Supply Current (Operating)		15	mA	V_{DD} = V_{DD} max, f_{CLK} = 8 MHz
V_{OH} (Data)	Shift Register Output Voltage	V_{DD}-0.5		V	I_O = -100µA
V_{OL} (Data)	Shift Register Output Voltage		0.5	V	I_O = 100µA
I_{IH}	Current Leakage, any input		1	µA	Input = V_{DD}
I_{IL}	Current Leakage, any input		-1	µA	Input = GND
V_{OC}	HV_{OUT} Output Clamp Diode Voltage		-1.5	V	I_{OL} -100mA
V_{OH}	HV_{OUT} Output when Sourcing	52		V	I_{OH} = -20mA, 0 to 70°C
V_{OL}	HV_{OUT} Output when Sinking		4	V	I_{OL} = 5mA, 0 to 70°C

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock Frequency		8	MHz	
t_{WL} or t_{WH}	Clock width, HIGH or LOW	62		ns	
t_{SU}	Setup time before CLK rises	25		ns	
t_H	Hold time after CLK rises	10		ns	
t_{DLH} (Data)	Data Output Delay after L to H CLK		110	ns	C_L = 15pF
t_{DHL} (Data)	Data Output Delay after H to L CLK		110	ns	C_L = 15pF
t_{DLE}	LE Delay after L to H CLK	50		ns	
t_{WLE}	Width of LE Pulse	50		ns	
t_{SLE}	LE Setup Time before L to H CLK	50		ns	
t_{ON}	Delay from LE to HV_{OUT}, L to H		500	ns	
t_{OFF}	Delay from LE to HV_{OUT}, H to L		500	ns	

Recommended Operating Conditions

(over 0 to 70°C for commercial temperature range and -55°C to 125°C for military)

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{PP}	High Voltage Supply	8.0	80	V	HV9308 and HV9408
V_{IH}	Input HIGH Voltage	V_{DD}-0.5	V_{DD}	V	
V_{IL}	Input LOW Voltage	0	0.5	V	
f_{CLK}	Clock Frequency	0	8	MHz	

Note:

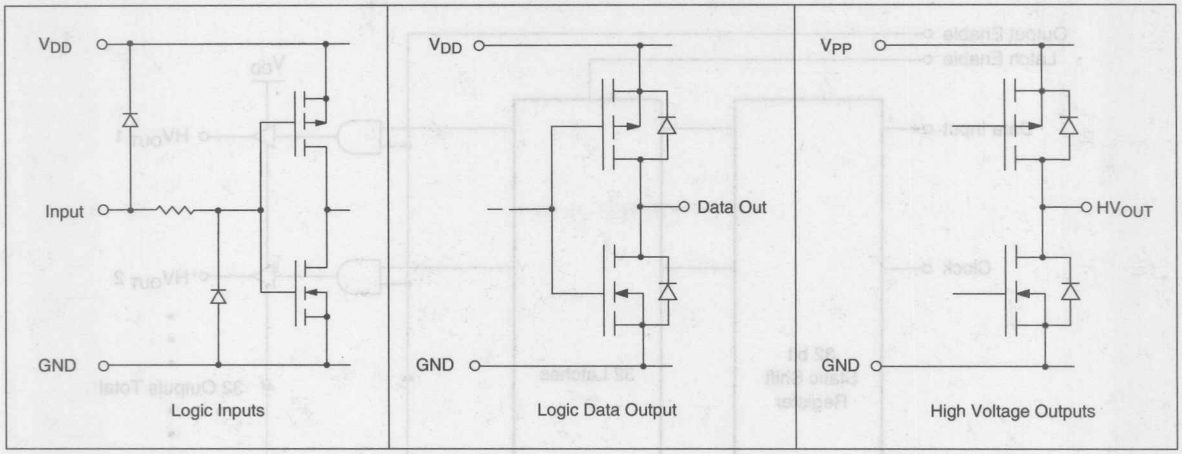
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

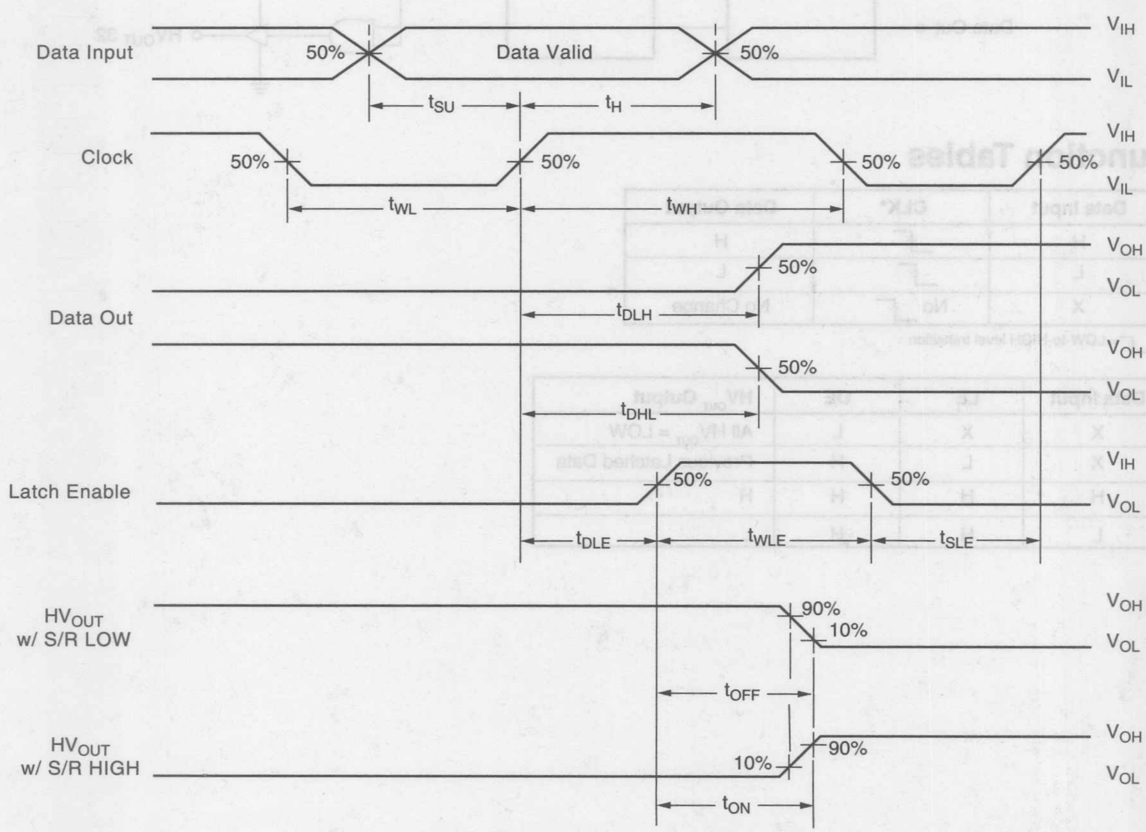
Power-down sequence should be the reverse of the above.

5. The V_{PP} should not drop below V_{DD} during operations.

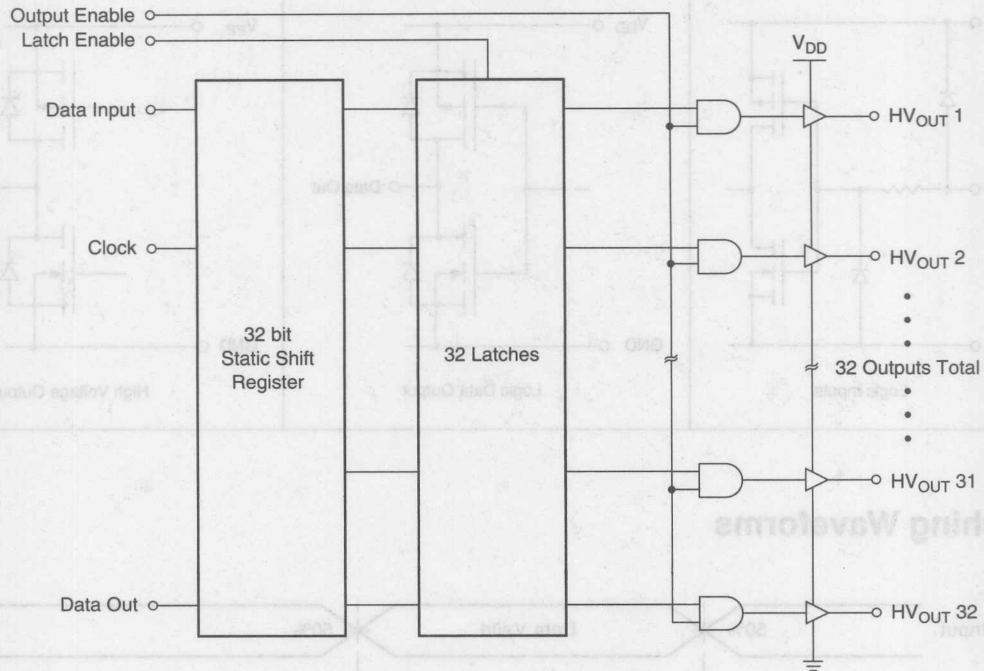
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Tables

Data Input	CLK*	Data Output
H	↑	H
L	↑	L
X	No ↑	No Change

* ↑ = LOW-to-HIGH level transition

Data Input	LE	OE	HV_{OUT} Output
X	X	L	All HV_{OUT} = LOW
X	L	H	Previous Latched Data
H	H	H	H
L	H	H	L

Pin Configuration

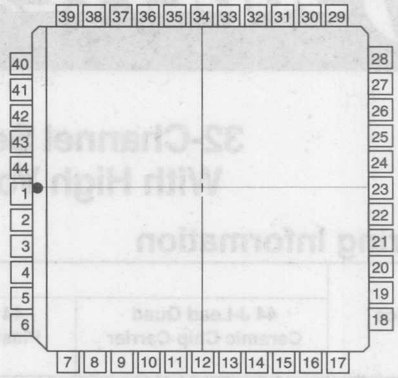
HV93
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Output Enable
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HV_{OUT} 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	N/C	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

HV94
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Output Enable
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	N/C	43	HV_{OUT} 14
22	Clock	44	HV_{OUT} 15

Package Outline



top view
44-pin J-Lead Package

Supertex inc.

HV97
HV98

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Package Options			
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV97	HV9708DJ	HV9708PJ	HV9708X	RBHV9708DJ
HV98	HV9808DJ	HV9808PJ	HV9808X	RBHV9808DJ

*For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS® technology
- Output voltages up to 80V
- Low power level shifting
- Shift register speed 8MHz
- Latched data outputs
- Forward and reverse shifting options
- Diode to V_{PP} allows efficient power recovery
- 5V CMOS compatible inputs
- Hi-Rel processing available

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +7V
Output voltage, V_{PP}		V_{DD} to +80V
Logic input levels[2]		-0.5V to V_{DD} +0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV97 and HV98 are low-voltage serial to high-voltage parallel converters wtih push-pull outputs.These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays. The inputs are fully CMOS compatible.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV97 shifts data in the clockwise direction when viewed from the top of the package and the HV98 shifts in the counterclockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (V_{PP} = 60V, V_{DD} = 5V, T_A =25°C)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PP}	V_{PP} Supply Current		100	µA	HV_{OUT} outputs HIGH to LOW
I_{DDQ}	I_{DD} Supply Current (Quiescent)		100	µA	All inputs = V_{DD} or GND
I_{DD}	I_{DD} Supply Current (Operating)		15	mA	V_{DD} = V_{DD} max, f_{CLK} = 8 MHz
V_{OH} (Data)	Shift Register Output Voltage	V_{DD}-0.5		V	I_O = -100µA
V_{OL} (Data)	Shift Register Output Voltage		0.5	V	I_O = 100µA
I_{IH}	Current Leakage, any input		1	µA	Input = V_{DD}
I_{IL}	Current Leakage, any input		-1	µA	Input = GND
V_{OC}	HV_{OUT} Output Clamp Diode Voltage		-1.5	V	I_{OL} = 20mA
V_{OH}	HV_{OUT} Output when Sourcing	52		V	I_{OH} = -20mA, 0 to 70°C
V_{OL}	HV_{OUT} Output when Sinking		4	V	I_{OL} = 5mA, 0 to 70°C

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock Frequency		8	MHz	
t_{WL} or t_{WH}	Clock width, HIGH or LOW	62		ns	
t_{SU}	Setup time before CLK rises	25		ns	
t_H	Hold time after CLK rises	10		ns	
t_{DLH} (Data)	Data Output Delay after L to H CLK		100	ns	C_L = 15pF
t_{DHL} (Data)	Data Output Delay after H to L CLK		100	ns	C_L = 15pF
t_{DLE}	LE Delay after L to H CLK	50		ns	
t_{WLE}	Width of LE Pulse	50		ns	
t_{SLE}	LE Setup Time before L to H CLK	50		ns	
t_{ON}	Delay from LE to HV_{OUT}, L to H		500	ns	
t_{OFF}	Delay from LE to HV_{OUT}, H to L		500	ns	

Recommended Operating Conditions

(over 0 to 70°C for commercial temperature range and -55°C to 125°C for military)

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{PP}	High Voltage Supply	8.0	80	V	
V_{IH}	Input HIGH Voltage	V_{DD}-0.5	V_{DD}	V	
V_{IL}	Input LOW Voltage	0	0.5	V	
f_{CLK}	Clock Frequency	0	8	MHz	

Note:

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

5. The V_{PP} should not drop below V_{DD} or float during operations.

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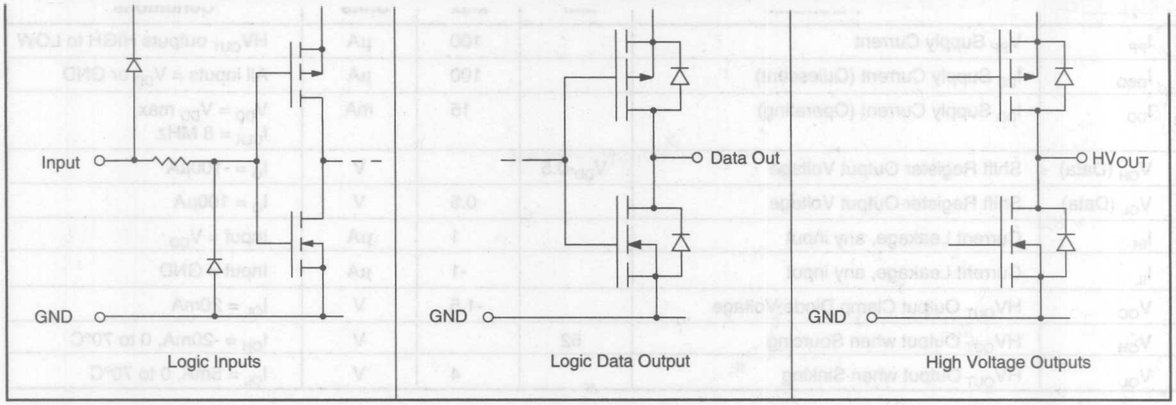
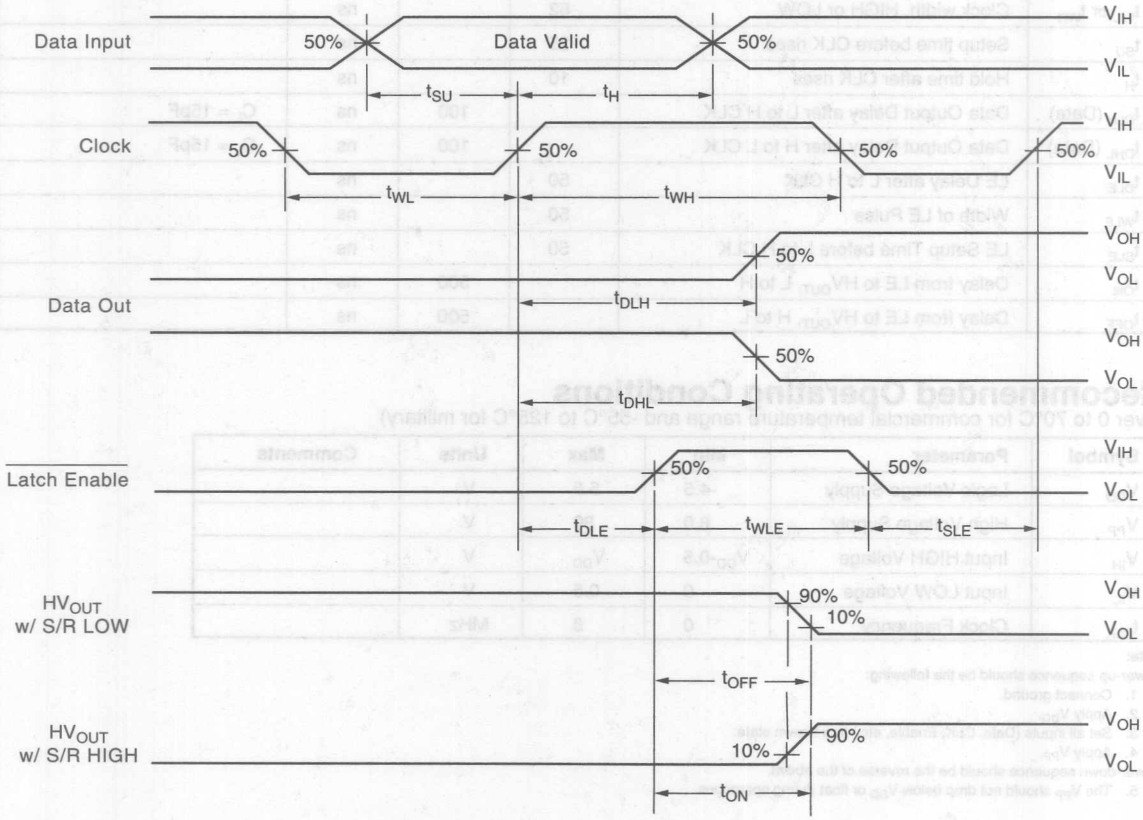
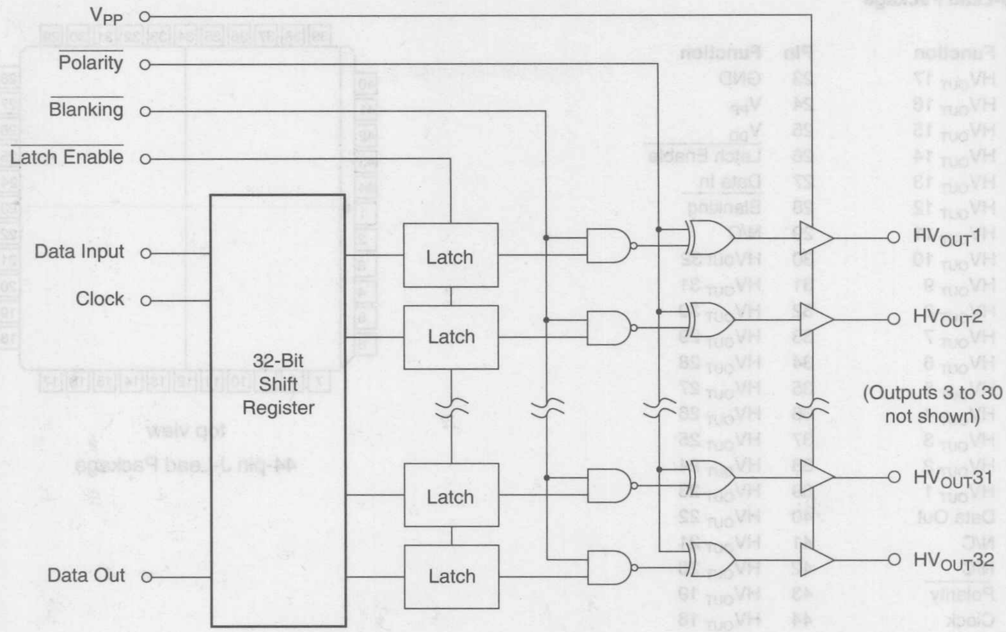


Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1	Shift Reg 2…32	HV Outputs 1	HV Outputs 2…32	Data Out
All on	X	X	X	L	L	*	*…*	H	H…H	*
All off	X	X	X	L	H	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Load S/R	H or L	$\uparrow$	L	H	H	H or L	*…*	*	*…*	*
Load latches	X	H or L	$\uparrow$	H	H	*	*…*	*	*…*	*
	X	H or L	$\uparrow$	H	L	*	*…*	$\overline{*}$	$\overline{*\ldots*}$	*
Transparent latch mode	L	$\uparrow$	H	H	H	L	*…*	L	*…*	*
	H	$\uparrow$	H	H	H	H	*…*	H	*…*	*

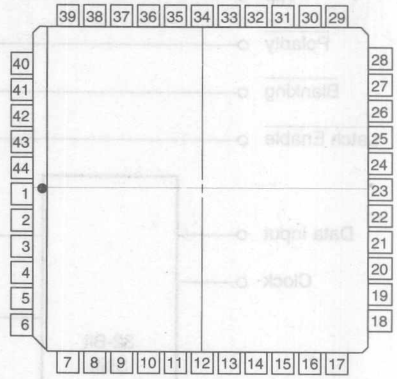
Notes:
H = high level, L = low level, X = irrelevant, $\uparrow$ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

Pin Configurations

HV97
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	$\overline{\text{Latch Enable}}$
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	$\overline{\text{Blanking}}$
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HVout 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	$\overline{\text{Polarity}}$	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

Package Outline



top view

44-pin J-Lead Package

HV98
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	$\overline{\text{Latch Enable}}$
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	$\overline{\text{Blanking}}$
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	$\overline{\text{Polarity}}$	43	HV_{OUT} 14
22	Clock	44	HV_{OUT} 15

Chapter 12 – High Voltage Analog Switches and Multiplexers

Supertex inc.

4-Channel High Voltage Analog Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Order Number / Package		
			18-pin Ceramic Side-brazed DIP*	18-pin Plastic DIP	Die
+70V	-70V	110V P-P	HV1014C	HV1014P	HV1014X
+80V	-80V	130V P-P	HV1016C	HV1016P	HV1016X

* Consult factory for Cerdip and Ceramic LCC availability.

Features

- HVCMOS® Technology
- Up to 130V peak to peak switching capability
- Output On-resistance typically 25 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 45 dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip direct control and latch logic circuitry

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +90V†
V_{NN} negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5 to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

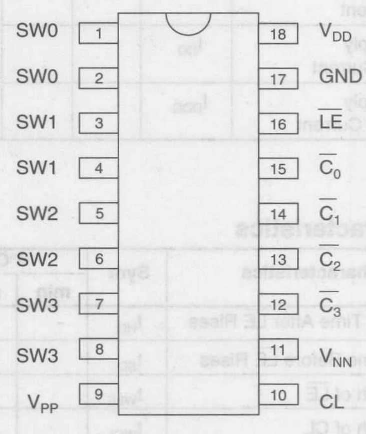
* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1016.

General Description

This device is a 4-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the data inputs. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view
18-pin DIP

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		25		25	40		45	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		15		15	30		35	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		28		28	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		30		18	35		40	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching (0-3)	ΔR_{ONS}		15			15		15	%	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 4 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				1.6	3.2			mA	1 SW ON, I_{SW} = 5mA,
Neg. HV Supply Current	I_{NNQ}				-1.6	-3.2			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				1.2	2.4			mA	V_{PP} = +50V, V_{NN} = -50V,
Neg. HV Supply Current	I_{NNQ}				-1.2	-2.4			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					2.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4				mA	Input Freq. = 3MHz
Logic Supply Quiescent Current	I_{DDQ}				10	500			µA	

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Data Hold Time After $\overline{LE}$ Rises	t_{HD}			5					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Time Width of CL	t_{WCL}			150					ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L = 10KΩ
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

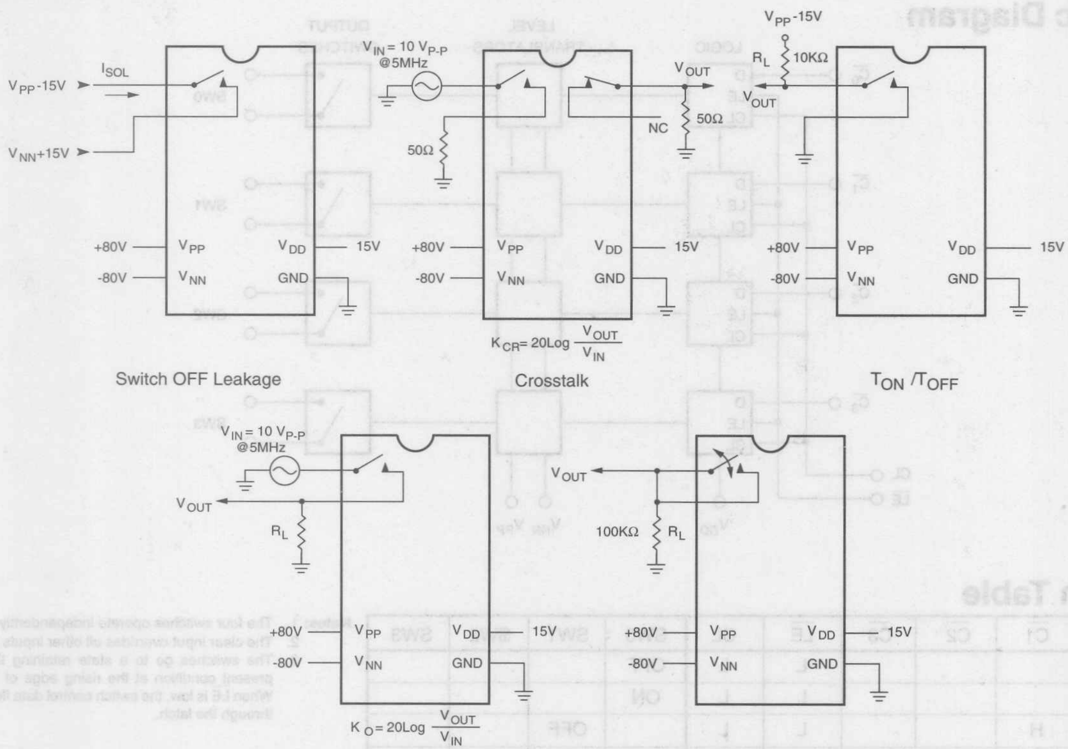
* For HV1016. For HV1014; V_{PP} = +70V, V_{NN} = -70V, and V_{DD} = 15V.

Operating Conditions

Symbol	Parameter	Device		Value
		HV1014	HV1016	
V_{DD}	Logic power supply voltage	X	X	+10V to +15.5V
V_{PP}	Positive high voltage supply	X		+50V to +70V
			X	+50V to +80V
V_{NN}	Negative high voltage supply	X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note:
1. Power up/down sequence is arbitrary except GND must be powered-up first and powered -down last.
2. V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.

Test Circuits



Switch OFF Leakage

Crosstalk

T_{ON} /T_{OFF}

OFF Isolation

DC Offset ON/OFF

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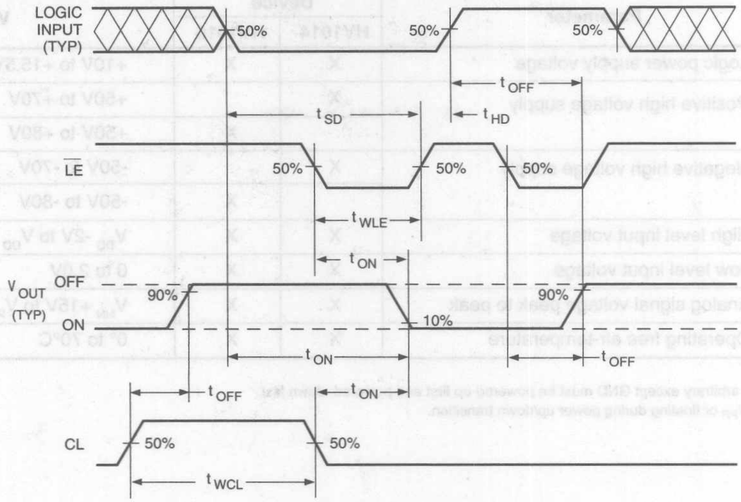
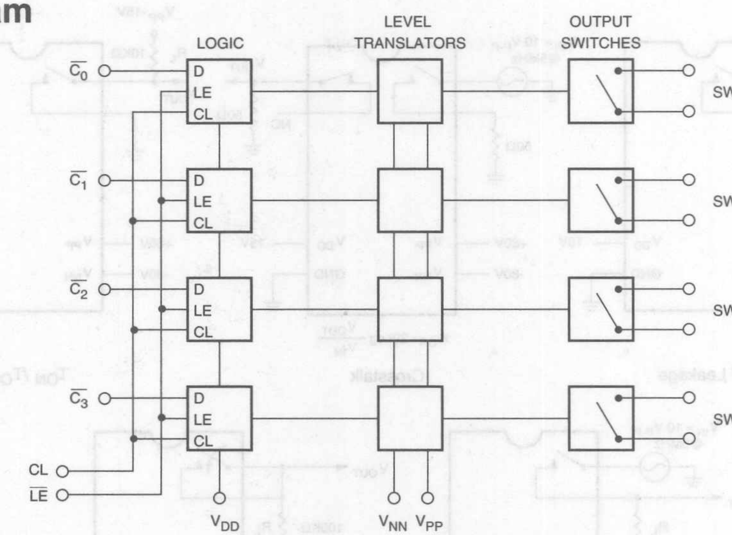
Logic Timing Waveforms



Logic Diagram



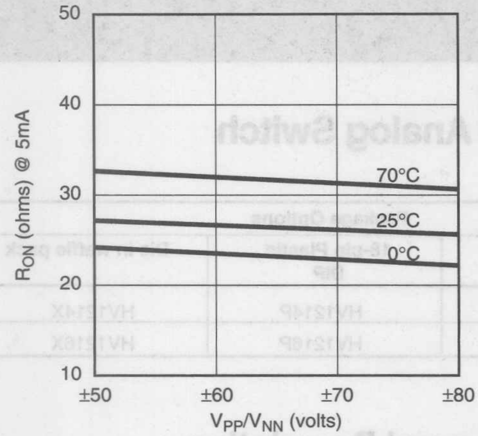
Truth Table

$\overline{C_0}$	$\overline{C1}$	$\overline{C2}$	$\overline{C3}$	$\overline{LE}$	CL	SW0	SW1	SW2	SW3
H				L	L	OFF			
L				L	L	ON			
	H			L	L		OFF		
	L			L	L		ON		
		H		L	L			OFF	
		L		L	L			ON	
			H	L	L				OFF
			L	L	L				ON
X	X	X	X	X	H	OFF	OFF	OFF	OFF
X	X	X	X	H	L	HOLD			

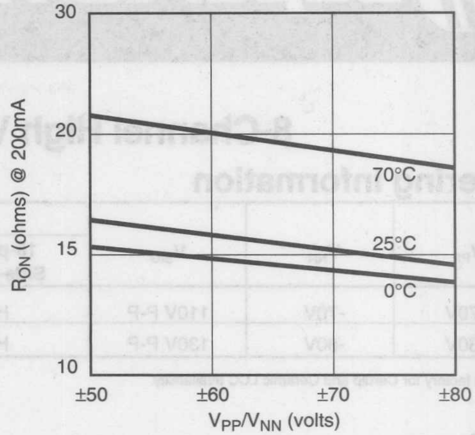
Notes:
1. The four switches operate independently.
2. The clear input overrides all other inputs.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the switch control data flows through the latch.

Typical Performance Curves

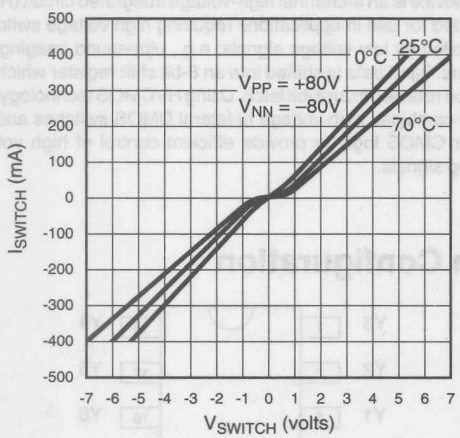
R_{ON} vs. V_{PP}/V_{NN}



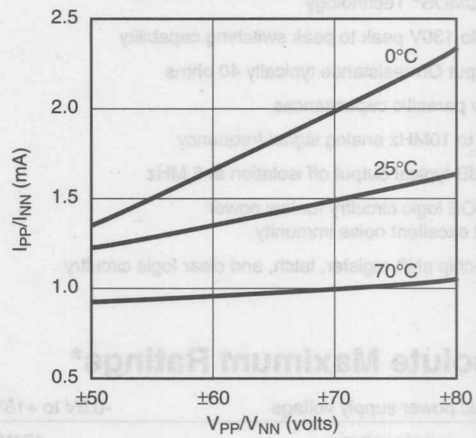
R_{ON} vs. V_{PP}/V_{NN}



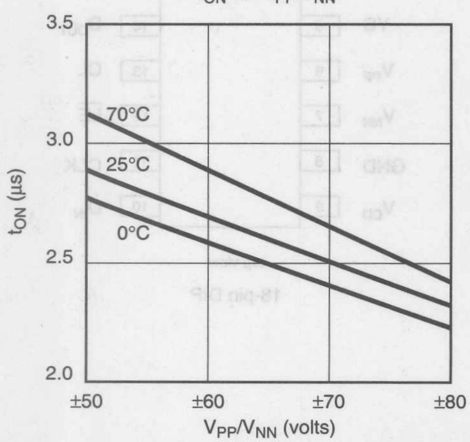
Switch Current vs. Switch Voltage



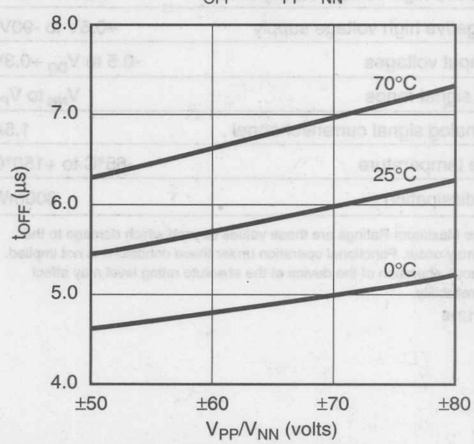
I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



t_{ON} vs. V_{PP}/V_{NN}



t_{OFF} vs. V_{PP}/V_{NN}



8-Channel High Voltage Analog Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			18-pin Ceramic Side-brazed DIP*	18-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1214C	HV1214P	HV1214X
+80V	-80V	130V P-P	HV1216C	HV1216P	HV1216X

* Consult factory for Cerdip and Ceramic LCC availability.

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch, and clear logic circuitry

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +90V†
V_{NN} negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5 to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

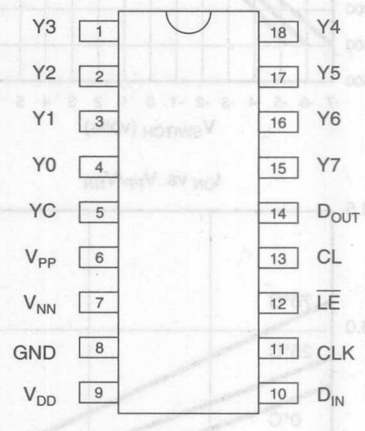
* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1216

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

18-pin DIP

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		40		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching	ΔR_{ONS}		30		10	30		30	%	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SWS ON, I_{SW} = 5mA
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4	6			mA	f_{CLK} = 3 MHz
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} -0.7V
Data Out Sink Current	I_{SINK}	0.7		0.8	0.9		0.7		mA	V_{OUT} = 0.7V
Logic Supply Quiesent Current	I_{DDQ}				10	500			µA	

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AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Clock Delay Time Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L = 10KΩ
Time Width of CL	t_{WCL}			150					ns	
Off Isolation	KO			-35	-45				dB	f = 5MHz
Clock Frequency	f_{CLK}					3.0			MHz	50% Duty Cycle f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			5.0					ns	
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq = 5MHz

* For HV1216. For HV1214; V_{PP} = +70V, V_{NN} = -70V, and V_{DD} = 15V .

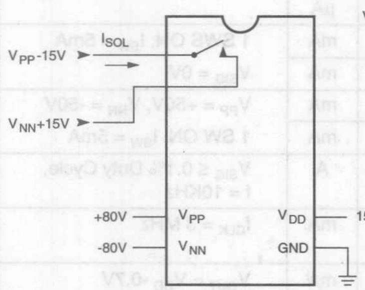
Operating Conditions

Symbol	Parameter	Device HV1214	Device HV1216	Value
V_{DD}	Logic power supply voltage	X	X	+10V to +15.5V
V_{PP}	Positive high voltage supply	X		+50.0V to +70V
			X	+50.0V to +80V
V_{NN}	Negative high voltage supply	X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

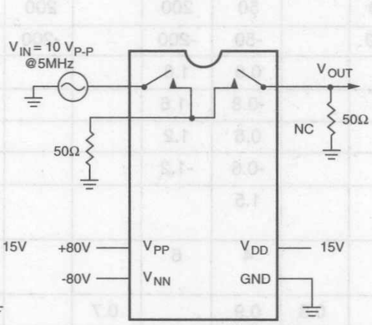
Note:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered - down last.
2. V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.

Test Circuits

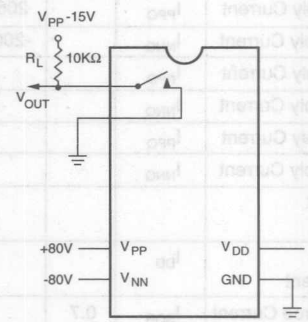


Switch OFF Leakage

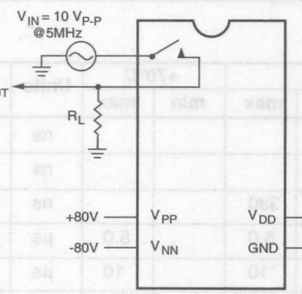


$K_{CR} = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

Crosstalk

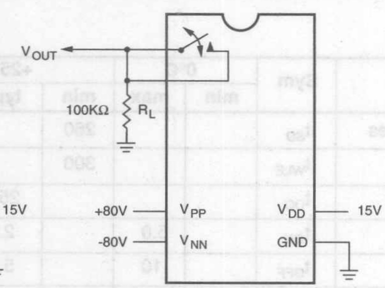


T_{ON} /T_{OFF}



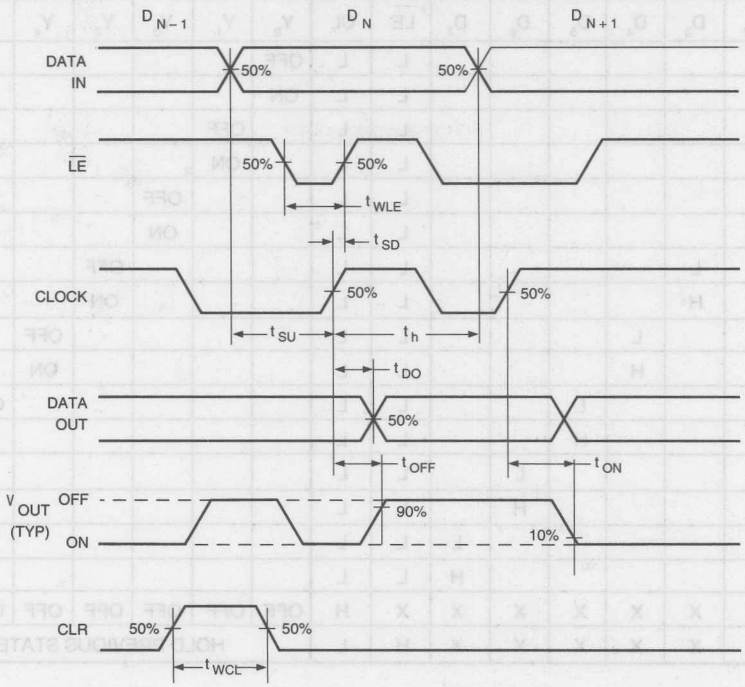
$K_O = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

OFF Isolation

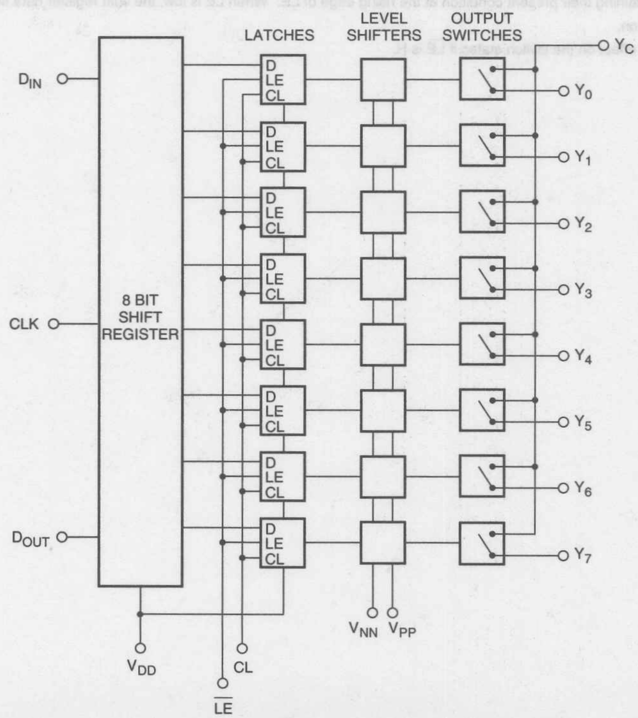


DC Offset ON/OFF

Logic Timing Waveform



Logic Diagram



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Truth Table

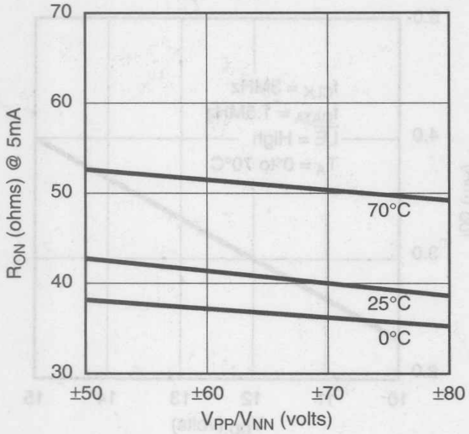
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	$\overline{LE}$	CL	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:

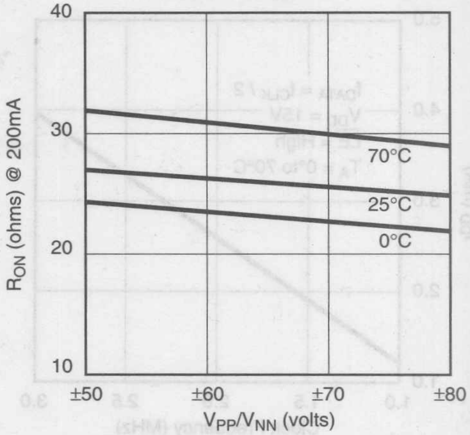
1. The eight switches operate independently, but connect to a common Z line.
2. Serial data is clocked in on the L→H transition of CLK.
3. The clear input overrides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.

Typical Performance Curves

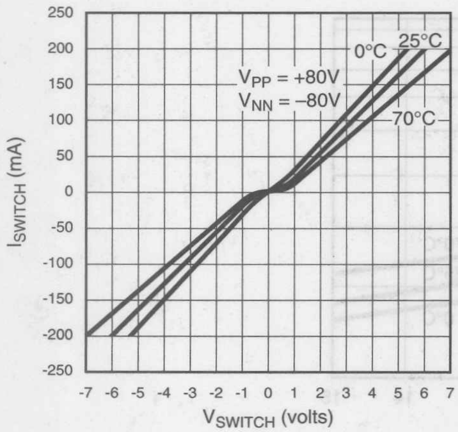
R_{ON} vs. V_{PP}/V_{NN}



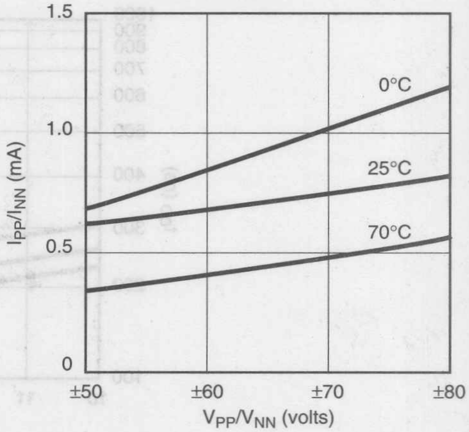
R_{ON} vs. V_{PP}/V_{NN}



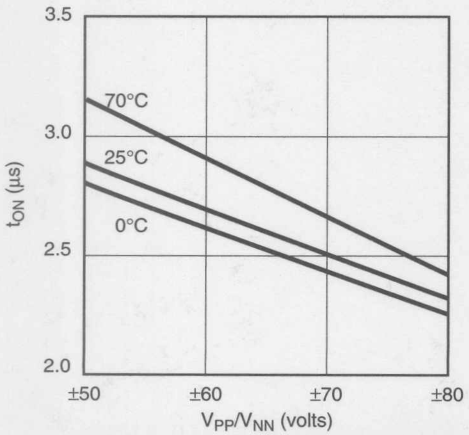
Switch Current vs. Switch Voltage



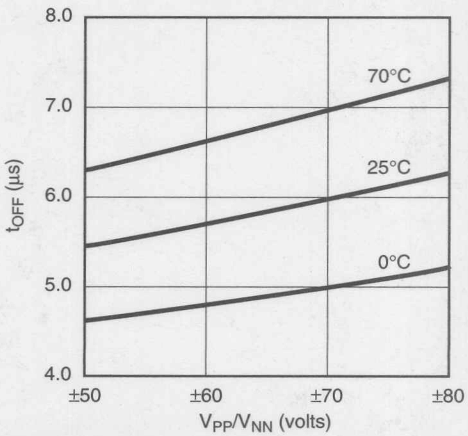
I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



t_{ON} vs. V_{PP}/V_{NN}



t_{OFF} vs. V_{PP}/V_{NN}



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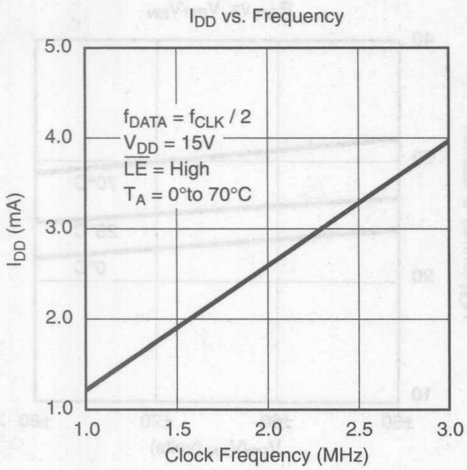
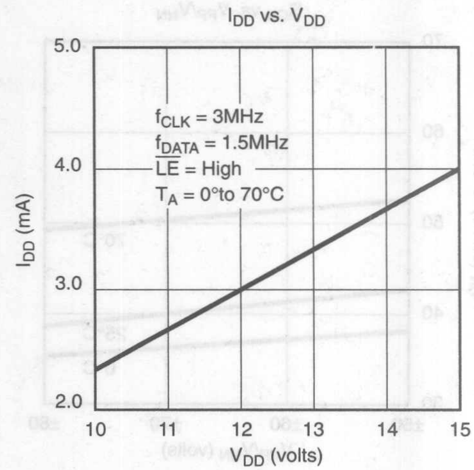
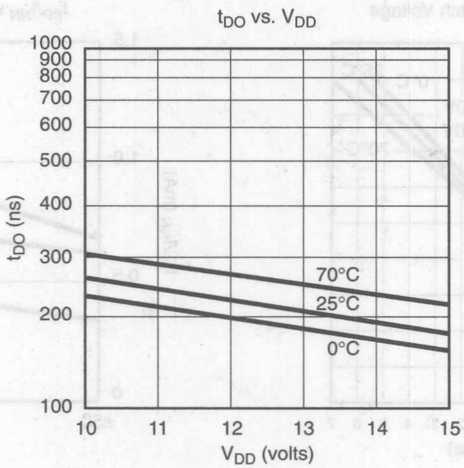
Typical Performance Curves







8-Channel High Voltage Analog Switch with Decoded Switch Selection

Ordering Information

			Package Options		
V_{PP}	V_{NN}	V_{SIG}	20-pin Ceramic Side-brazed DIP	20-pin Plastic DIP	Die
+70V	-70V	110V P-P	HV1414C	HV1414P	HV1414X
+80V	-80V	130V P-P	HV1416C	HV1416P	HV1416X

* Consult factory for Cerdip and Ceramic LCC availability.

Features

- ☐ HVCMOS® Technology
- ☐ Up to 130V peak to peak switching capability
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip decode, latch and chip select logic circuitry

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC), configured as a 1 of 8 decode function, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the decoded data.

The unique control logic on this device provides individual control of each switch, allowing more than one switch to be turned on at a time. The clear function turns off all switches simultaneously. The chip select inputs control the latches, holding the output stable while the address and data are changed. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

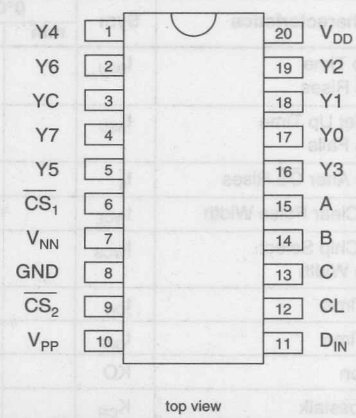
Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +90V†
V_{NN} negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5 to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1416

Pin Configuration



20-pin DIP

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Switch (ON) Resistance	R_{ONS}		50		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching	ΔR_{ONS}		30		10	30		30	%	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		10	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SW ON, I_{SW} = 5mA,
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V,
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4				mA	Input Freq. = 3MHz
Logic Supply Quiescent Current	I_{DDQ}				10	500			µA	

AC Characteristics

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
D_{IN} Set Up Time Before $\overline{CS}$ Rises	t_{DSU}			260					ns	
Address Set Up Time Before $\overline{CS}$ Falls	t_{ASU}			120					ns	
Hold Time After $\overline{CS}$ Rises	t_h			35					ns	
Minimum Clear Pulse Width	t_{WCL}			150					ns	
Minimum Chip Select Low Pulse Width	t_{WCS}			300					ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L = 10KΩ
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

* For HV1416. For HV1414; V_{PP} = +70V, V_{NN} = -70V, and V_{DD} = 15V.

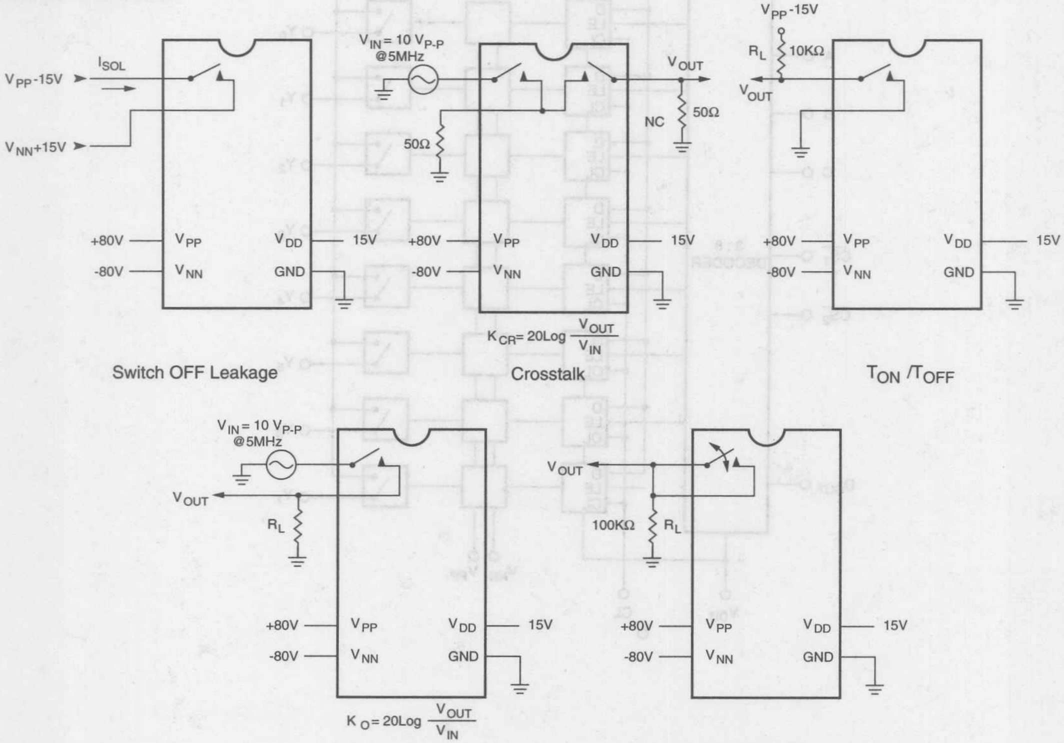
Operating Conditions

Symbol	Parameter	Device		Value
		HV1414	HV1416	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50V to +70V
			X	+50V to +80V
V_{NN}		X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Note:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.

Test Circuits



Switch OFF Leakage

Crosstalk

T_{ON} /T_{OFF}

OFF Isolation

DC Offset ON/OFF

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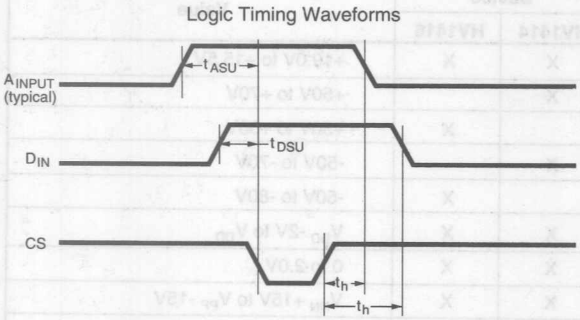
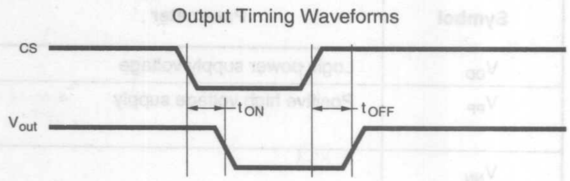
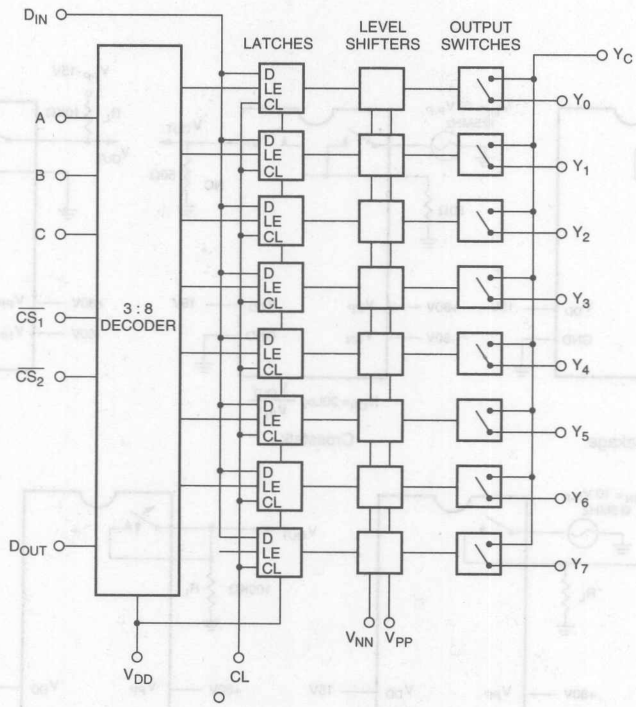
Switching Waveforms





Logic Diagram



Truth Table

C	B	A	$\overline{CS_1}$	$\overline{CS_2}$	D_{IN}	CL	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L	L	L	L	L	L	L	OFF							
L	L	L	L	L	H	L	ON							
L	L	H	L	L	L	L		OFF						
L	L	H	L	L	H	L		ON						
L	H	L	L	L	L	L			OFF					
L	H	L	L	L	H	L			ON					
L	H	H	L	L	L	L				OFF				
L	H	H	L	L	H	L				ON				
H	L	L	L	L	L	L					OFF			
H	L	L	L	L	H	L					ON			
H	L	H	L	L	L	L						OFF		
H	L	H	L	L	H	L						ON		
H	H	L	L	L	L	L							OFF	
H	H	L	L	L	H	L							ON	
H	H	H	L	L	L	L								OFF
H	H	H	L	L	H	L								ON
X	X	X	H	X	X	L	HOLDS PREVIOUS STATE							
X	X	X	X	H	X	L	HOLDS PREVIOUS STATE							
X	X	X	X	X	X	H	ALL OUTPUTS OFF							

Notes:
1. D_{IN} controls the switches through flow-through latches, which are clocked (enabled) by an 8-way decoder controlled by A, B, C, $\overline{CS_1}$, and $\overline{CS_2}$. Therefore, the latch for a particular switch goes into the HOLD state when any of the above inputs prevents selection. $\overline{CS_1}$ or $\overline{CS_2}$ can be used as an active LOW clock input.
2. Spurious clocking may occur if A, B, or C is changed with $\overline{CS_1}$ and $\overline{CS_2}$ both low.
3. The clear input CL overrides all other inputs.
4. The eight switches operate independently.

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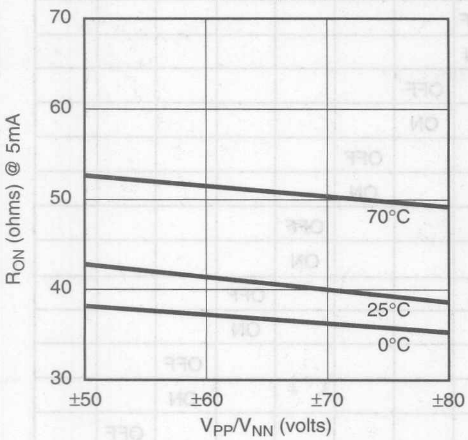
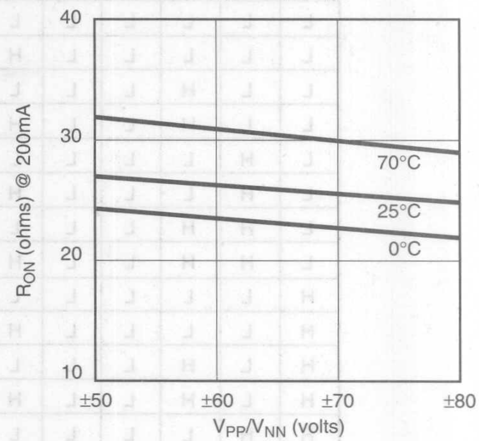
Typical Performance Curves

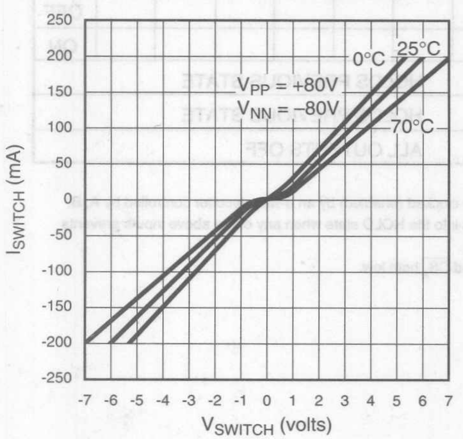
R_{ON} vs. V_{PP}/V_{NN}



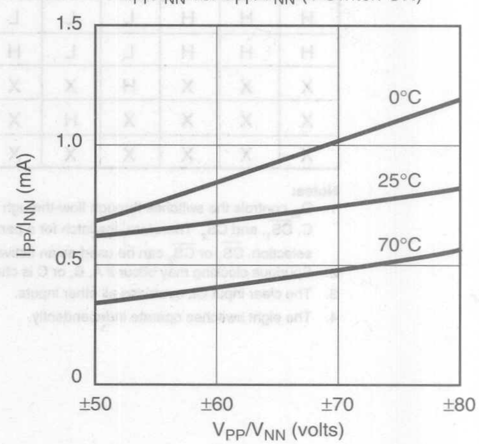
R_{ON} vs. V_{PP}/V_{NN}



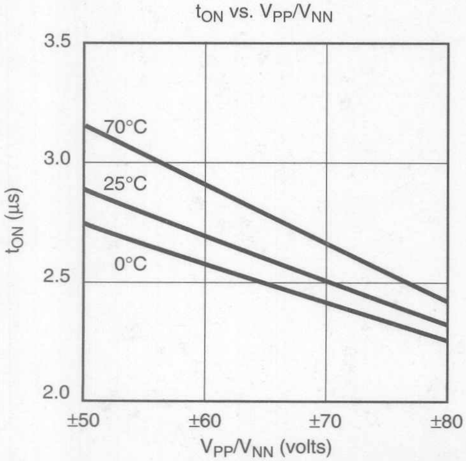
Switch Current vs. Switch Voltage



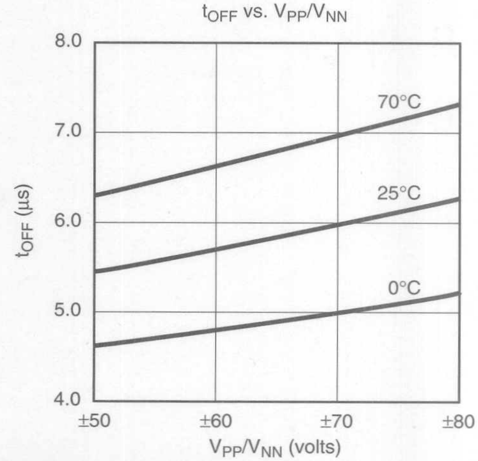
I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



t_{ON} vs. V_{PP}/V_{NN}



t_{OFF} vs. V_{PP}/V_{NN}



Supertex inc.

1 of 8 Decoded 8-Channel High Voltage Analog Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options		
			20-pin Ceramic Side-brazed DIP	20-pin Plastic DIP	Die in waffle pack
+70V	-70V	110V P-P	HV1514C	HV1514P	HV1514X
+80V	-80V	130V P-P	HV1516C	HV1516P	HV1516X

*Consult factory for Cerdip and Ceramic LCC availability.

Features

- HVCMOS® Technology
- Up to 130V peak to peak switching capability
- Output On-resistance typically 40 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 45 dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip decode, latch and chip select logic circuitry

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +90V†
V_{NN} negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5 to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A†
Storage temperature	-65°C to +150°C
Power dissipation	800mW

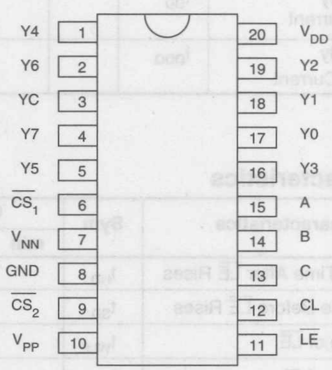
* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1516

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC), configured as a 1 of 8 decode functions, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. ON-chip latches are provided for the decoded data. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Pin Configuration



top view

20-pin DIP

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Switch (ON) Resistance	R_{ONS}		50		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching x and y (0-3)	ΔR_{ONS}		30		10	30		30	%	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SW ON, I_{SW} = 5mA,
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4				mA	Input Freq. = 3MHz
Logic Supply Quiescent Current	I_{DDQ}				10	500			µA	

AC Characteristics

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Data Hold Time After $\overline{LE}$ Rises	t_{HD}			5.0					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Time Width of CL	t_{WCL}			150					ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L = 10KΩ
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

* For HV1516. For HV1514; V_{PP} = +70V, V_{NN} = -70V, and V_{DD} = 15V.

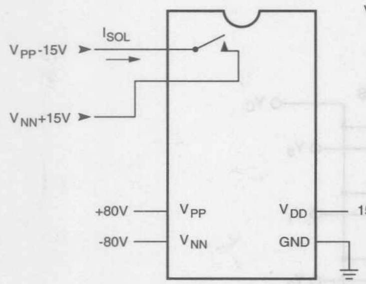
Operating Conditions

Symbol	Parameter	Device		Value
		HV1514	HV1516	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50V to +70V
			X	+50V to +80V
V_{NN}	Negative high voltage supply	X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

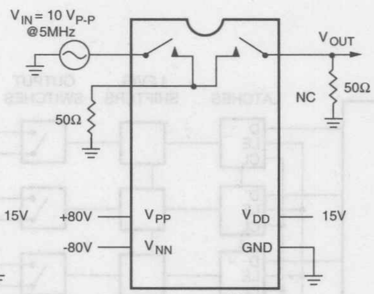
Note:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.

Test Circuits

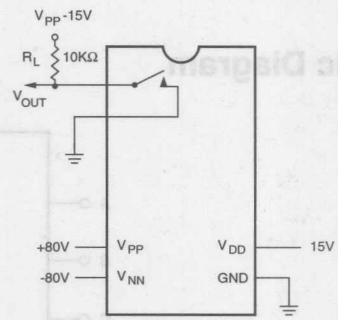


Switch OFF Leakage

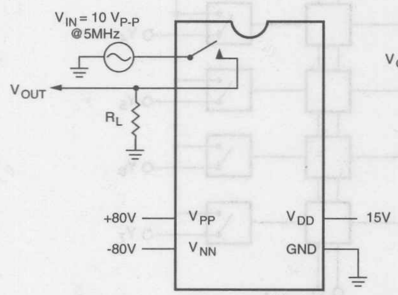


$K_{CR} = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

Crosstalk

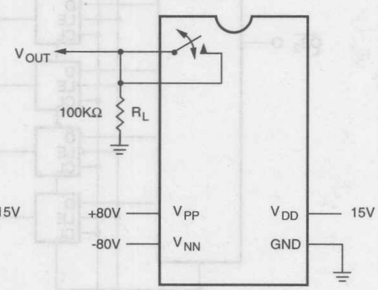


T_{ON} /T_{OFF}



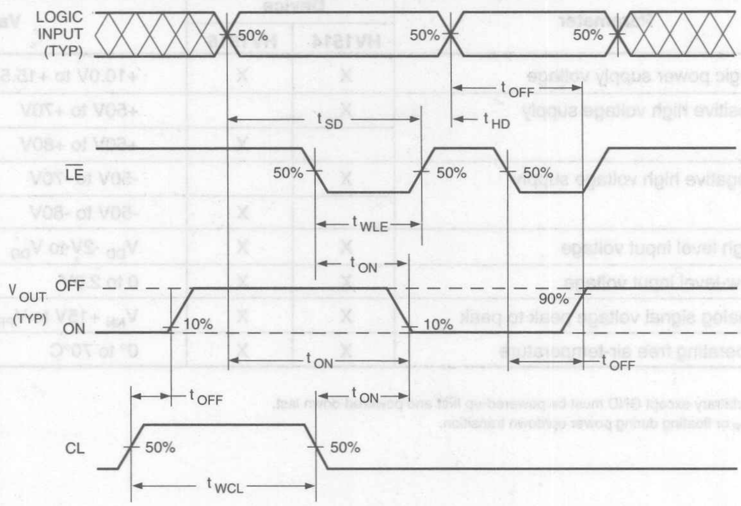
$K_O = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

OFF Isolation

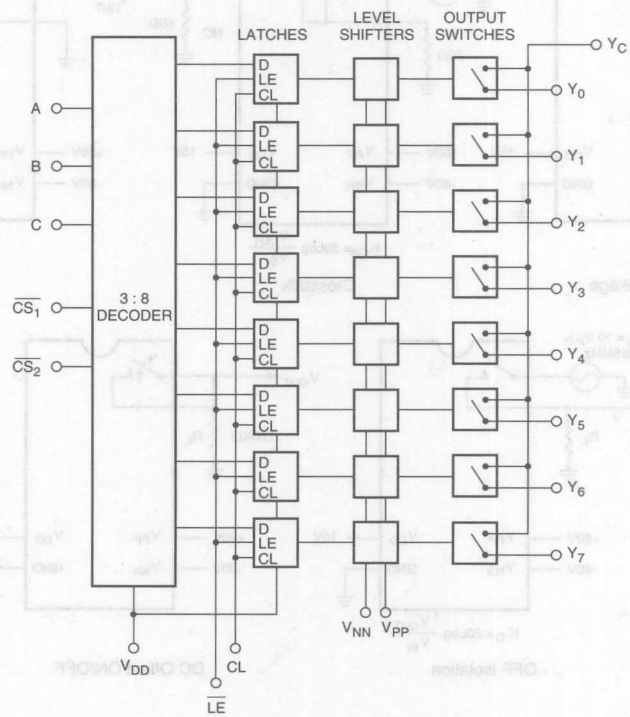


DC Offset ON/OFF

Logic Timing Waveforms



Logic Diagram



Truth Table

C	B	A	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{LE}$	CL	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	L	L	L	L	L	ON							
L	L	H	L	L	L	L		ON						
L	H	L	L	L	L	L			ON					
L	H	H	L	L	L	L				ON				
H	L	L	L	L	L	L					ON			
H	L	H	L	L	L	L						ON		
H	H	L	L	L	L	L							ON	
H	H	H	L	L	L	L								ON
X	X	X	H	X	L	L	ALL OUTPUTS OFF							
X	X	X	X	H	L	L	ALL OUTPUTS OFF							
X	X	X	X	X	X	H	ALL OUTPUTS OFF							
X	X	X	X	X	H	L	HOLDS PREVIOUS STATE							

Notes:
1. Address data at A, $\overline{B}$, C cause on of the eight switches to be selected for connection to the common bus C.
2. The clear input CL overrides all other inputs.
3. Since the latch follows the decoder, only the CL input matters when $\overline{LE}$ is H.
4. The switches go to a state retaing their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the decoded selection address information flows through the latch.

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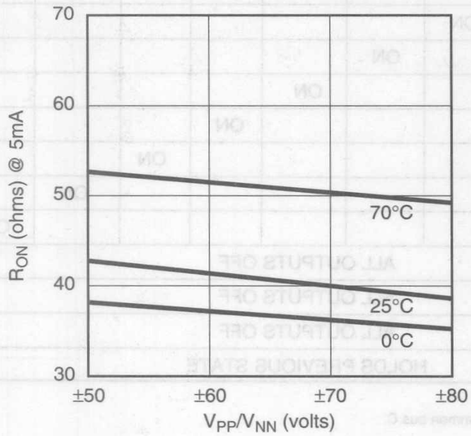
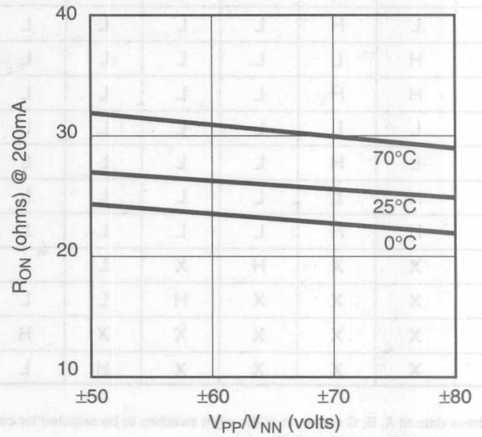
Typical Performance Curves

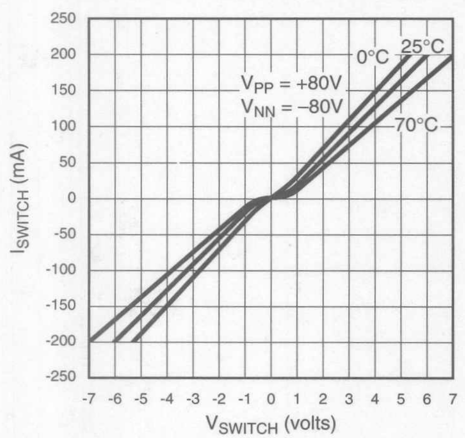
R_{ON} vs. V_{PP}/V_{NN}



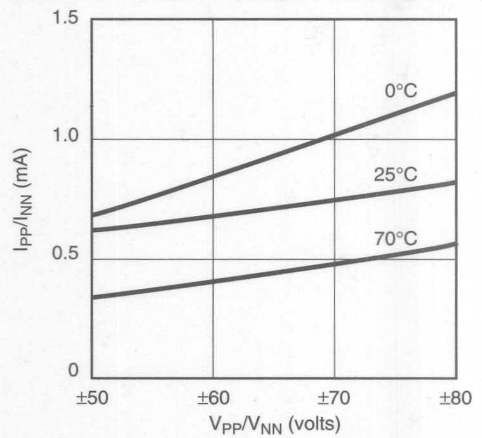
R_{ON} vs. V_{PP}/V_{NN}



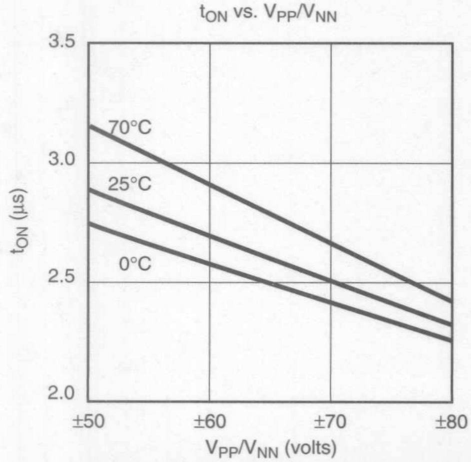
Switch Current vs. Switch Voltage



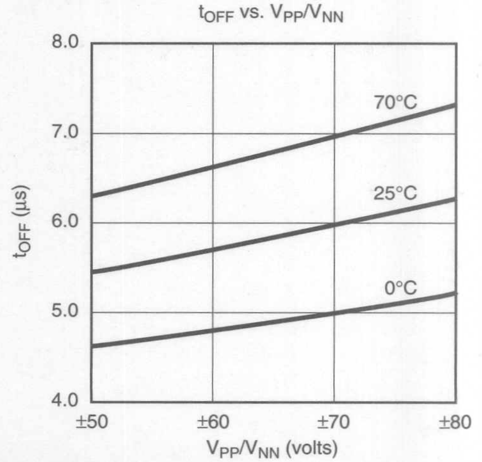
I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



t_{ON} vs. V_{PP}/V_{NN}



t_{OFF} vs. V_{PP}/V_{NN}



8-Channel High Voltage Analog Switch

Ordering Information

			Package Options				
V_{PP}	V_{NN}	V_{SIG}	24-pin Ceramic Side-brazed DIP*	Die	36-pin Leaded Ceramic Chip Carrier*	24-pin Plastic DIP	28-lead Plastic Chip Carrier
+70V	-70V	110V P-P	HV1614C	HV1614X	HV1614CS	HV1614P	HV1614PJ
+80V	-80V	130V P-P	HV1616C	HV1616X	HV1616CS	HV1616P	HV1616PJ

* Consult factory for Cerdip and Ceramic LCC availability.

Features

- HVCMOS® technology
- Up to 130V peak to peak switching capability
- Output On-resistance typically 40 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 45 dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip shift register and latch logic circuitry
- Surface mount package available

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} Positive high voltage supply	-0.5V to +90V†
V_{NN} Negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1616

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Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		50		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching	ΔR_{ONS}		15			15		15	%	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SW ON, I_{SW} = 5mA,
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V,
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4	6			mA	f_{CLK} = 3MHz
Logic Supply Quiescent Current	I_{DDQ}				10	500			µA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	0.7		0.8	0.9		0.7		mA	V_{OUT} = 0.7V

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L =10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L =10KΩ
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Max Clock Freq	f_{CLK}					3.0			MHz	50% Duty Cycle f_{DATA} = $f_{CLK}/2$
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			35					ns	
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

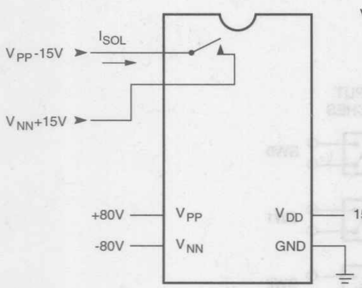
* For HV1616. For HV1614; V_{PP} = +70V. V_{NN} = -70V, and V_{DD} = 15V.

Operating Conditions

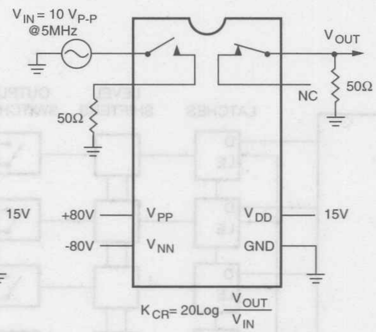
Symbol	Parameter	Device		Value
		HV1614	HV1616	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50V to +70V
			X	+50V to +80V
V_{NN}	Negative high voltage supply	X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

Notes:
1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.

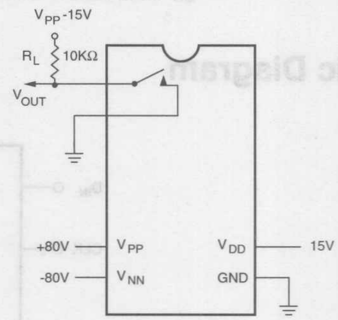
Test Circuits



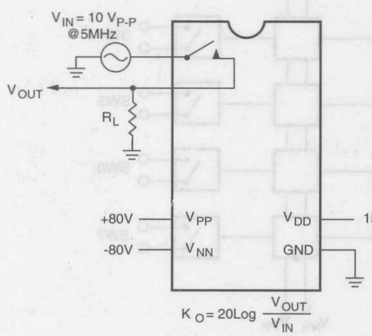
Switch OFF Leakage



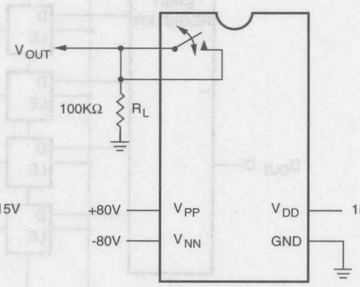
Crosstalk



T_{ON} /T_{OFF}

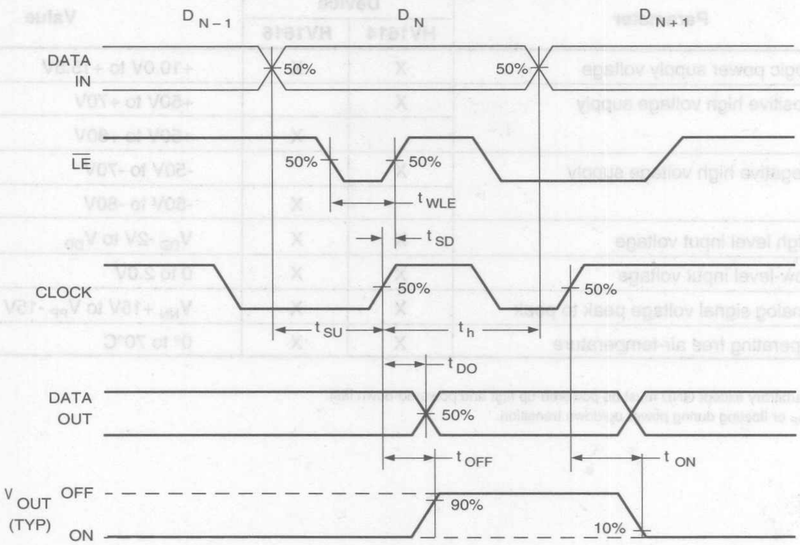


OFF Isolation

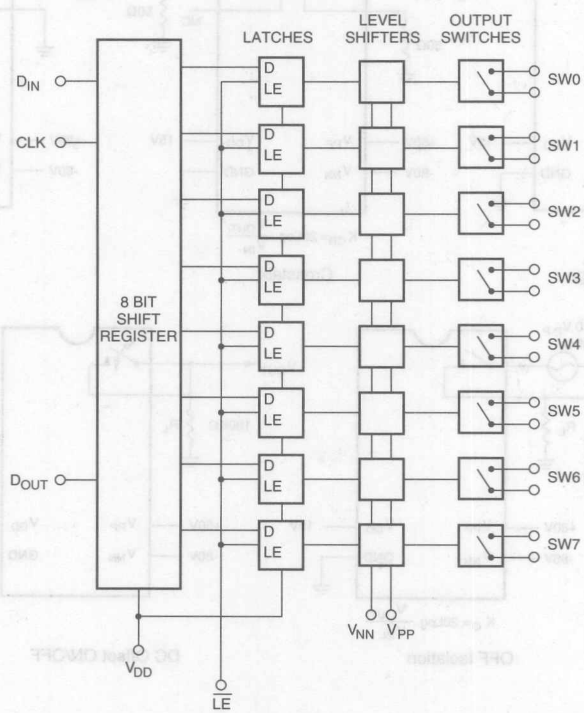


DC Offset ON/OFF

Logic Timing Waveforms



Logic Diagram



Truth Table

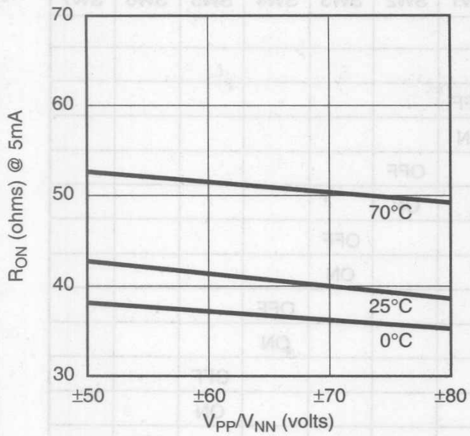
D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

Notes:

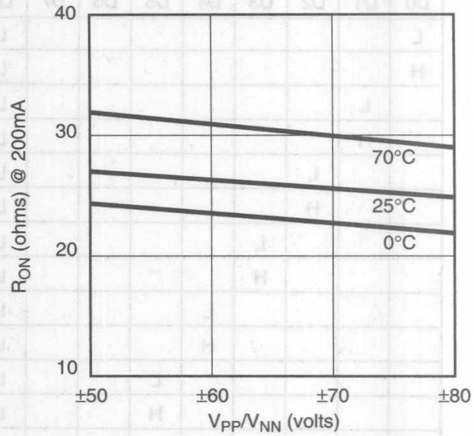
1. The eight switches operate independently.
2. Serial data is clocked in on the L → H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of LE. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.

Typical Performance Curves

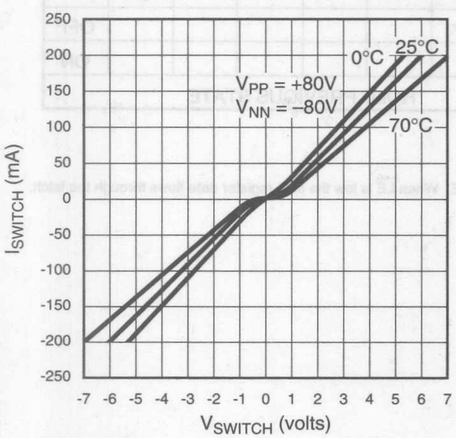
R_{ON} vs. V_{PP}/V_{NN}



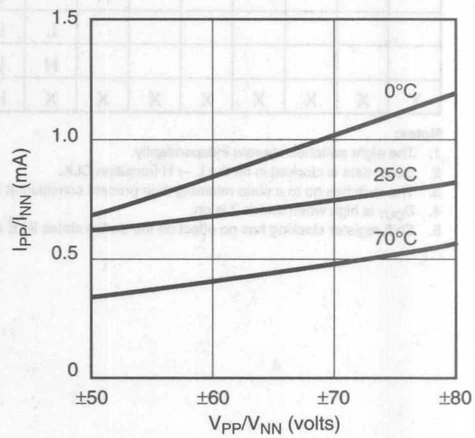
R_{ON} vs. V_{PP}/V_{NN}



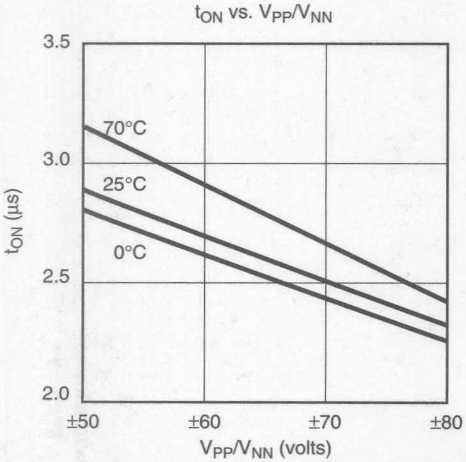
Switch Current vs. Switch Voltage



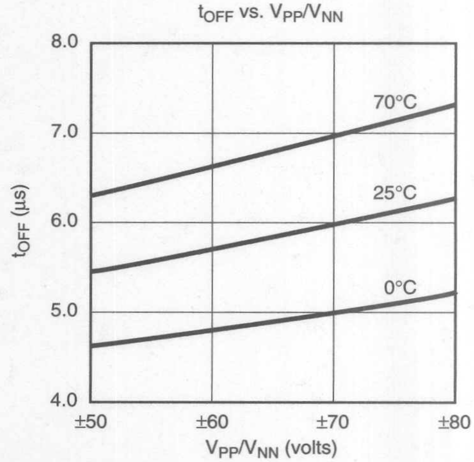
I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



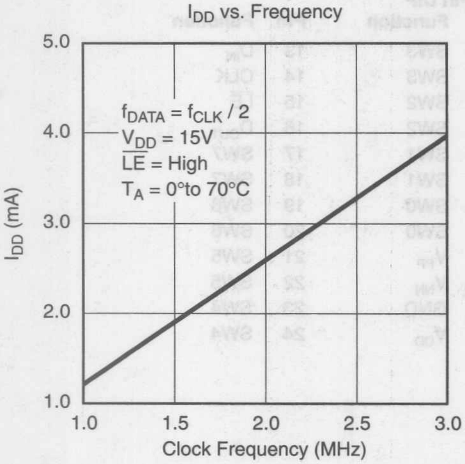
t_{ON} vs. V_{PP}/V_{NN}

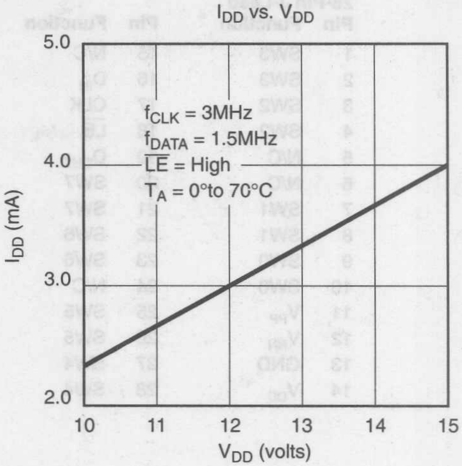


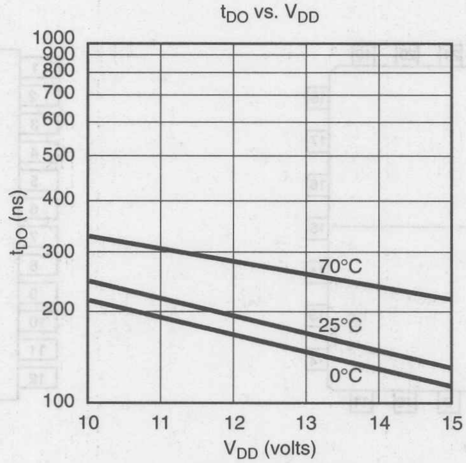
t_{OFF} vs. V_{PP}/V_{NN}



Typical Performance Curves







Pin Configurations

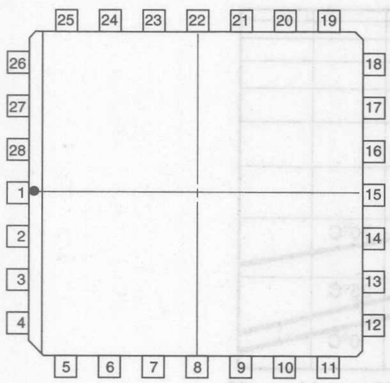
28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	N/C	19	D_{OUT}
6	N/C	20	SW7
7	SW1	21	SW7
8	SW1	22	SW6
9	SW0	23	SW6
10	SW0	24	N/C
11	V_{PP}	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

24-Pin DIP

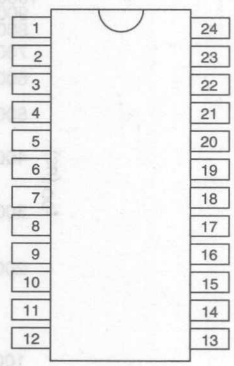
Pin	Function	Pin	Function
1	SW3	13	D_{IN}
2	SW3	14	CLK
3	SW2	15	$\overline{LE}$
4	SW2	16	D_{OUT}
5	SW1	17	SW7
6	SW1	18	SW7
7	SW0	19	SW6
8	SW0	20	SW6
9	V_{PP}	21	SW5
10	V_{NN}	22	SW5
11	GND	23	SW4
12	V_{DD}	24	SW4

Package Outlines



top view

28-pin J-lead Package



top view

24-pin DIP

Supertex inc.

8-Channel High Voltage Analog Switch

Ordering Information

			Package Options				
V_{PP}	V_{NN}	V_{SIG}	28-pin Ceramic Side-brazed DIP*	Die	36-pin Leaded Ceramic Chip Carrier*	28-pin Plastic DIP	28-lead Plastic Chip Carrier
+70V	-70V	110V P-P	HV1814C	HV1814X	HV1814CS	HV1814P	HV1814PJ
+80V	-80V	130V P-P	HV1816C	HV1816X	HV1816CS	HV1816P	HV1816PJ

* Consult factory for Cerdip and Ceramic LCC availability.

Features

- ☐ HVCMOS® technology
- ☐ Up to 130V peak to peak output switching
- ☐ Output On-resistance typically 40 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 45 dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power and excellent noise immunity
- ☐ On-chip shift register, latch and clear logic circuitry

General Description

This device is an 8-channel high-voltage integrated circuit (HVIC) intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. Using HVCMOS technology, this HVIC combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} Positive high voltage supply	-0.5V to +90V†
V_{NN} Negative high voltage supply	+0.5V to -90V†
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	800mW

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV1816

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Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V and V_{DD} = 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		50		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching	ΔR_{ONS}		15			15		15	%	V_{PP} = +50V, V_{NN} = -50V I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SW ON, I_{SW} = 5mA
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V,
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4	6			mA	f_{CLK} = 3MHz
Logic Supply Quiescent Current	I_{DDQ}				10	500			µA	
Data Out Source Current	I_{SOR}	0.7		0.8	0.9		0.7		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	0.7		0.8	0.9		0.7		mA	V_{OUT} = 0.7V

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Clock Delay Time to Data Out	t_{DO}				250	330			ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L =10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L =10KΩ
Time Width of CL	t_{WCL}			150					ns	
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Max Clock Freq	f_{CLK}					3.0			MHz	50% Duty Cycle f_{DATA} = f_{CLK}/2
Set Up Time Data to Clock	t_{SU}			0					ns	
Hold Time Data from Clock	t_h			35					ns	
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

*For HV1816. For HV1814; V_{PP} = +70V. V_{NN} = -70V, and V_{DD} = 15V unless otherwise noted)

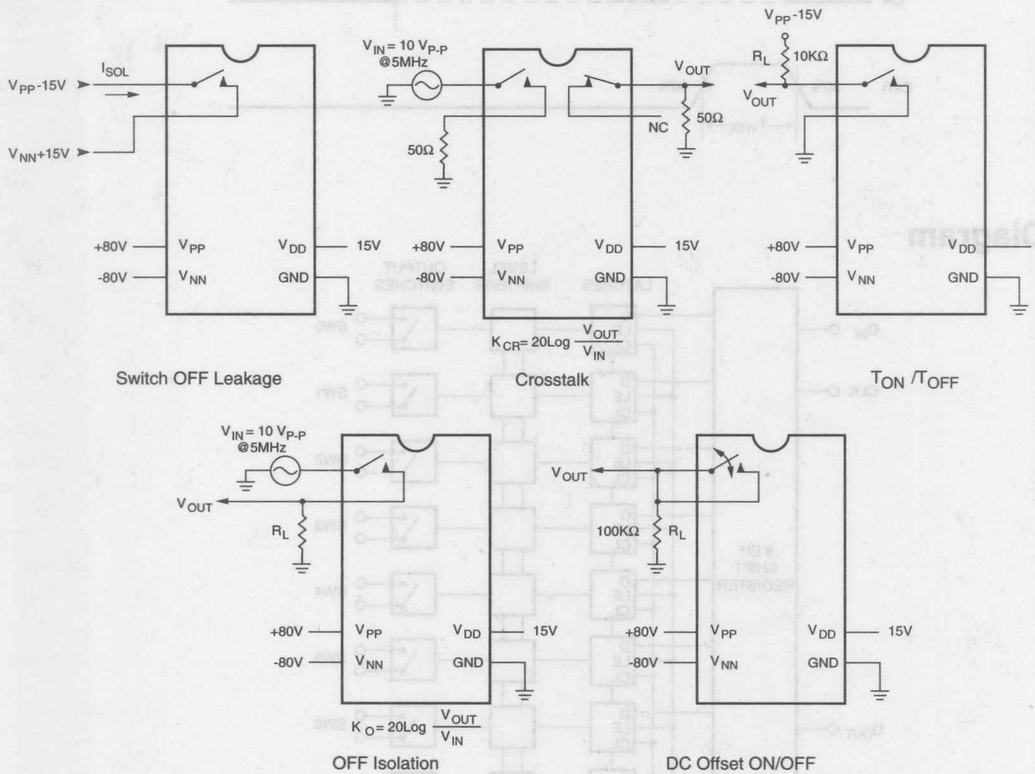
Operating Conditions

Symbol	Parameter	Device		Value
		HV1814	HV1816	
V_{DD}	Logic power supply voltage	X	X	+10.0V to +15.5V
V_{PP}	Positive high voltage supply	X		+50V to +70V
			X	+50V to +80V
V_{NN}	Negative high voltage supply	X		-50V to -70V
			X	-50V to -80V
V_{IH}	High level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	X	X	0° to 70°C

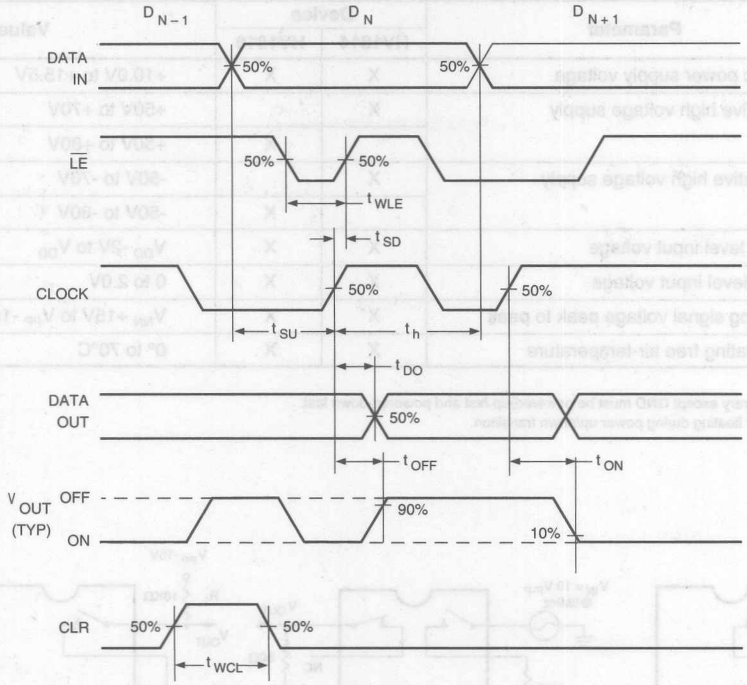
Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.

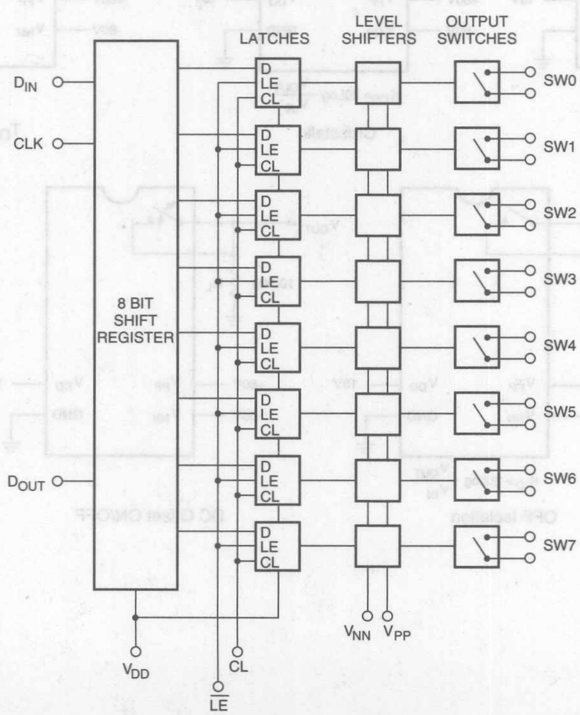
Test Circuits



Logic Timing Waveforms



Logic Diagram



Truth Table

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	$\overline{LE}$	CL	SW_0	SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	SW_7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							

Notes:
1. The eight switches operate independently.
2. Serial data is clocked in on the L → H transition CLK.
3. The clear input over rides all other inputs.
4. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
5. D_{OUT} is high when switch 7 is on.
6. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.

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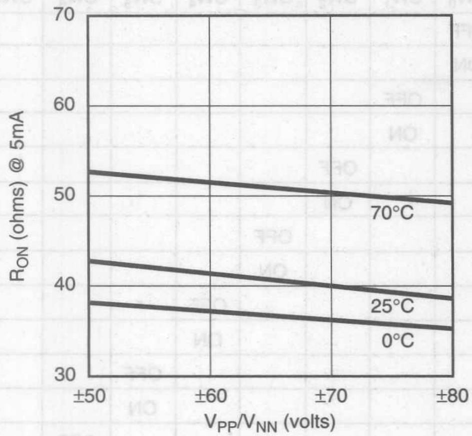
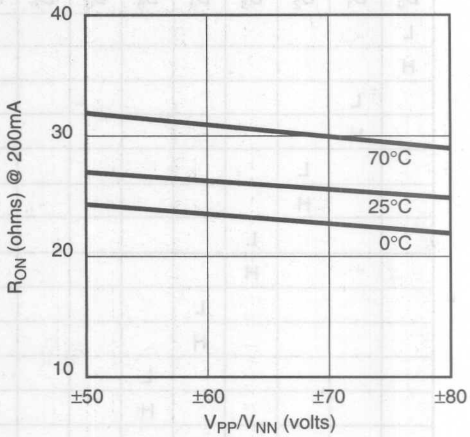
Typical Performance Curves

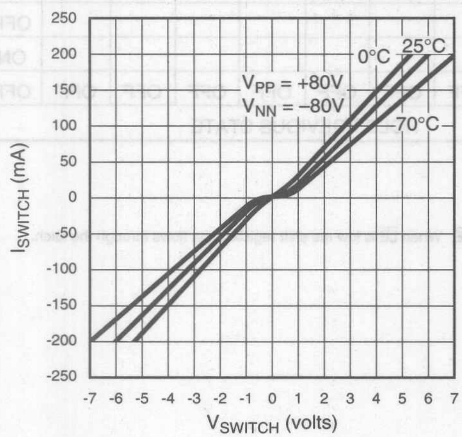
R_{ON} vs. V_{PP}/V_{NN}



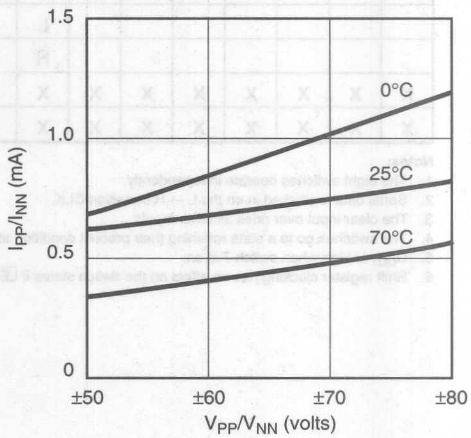
R_{ON} vs. V_{PP}/V_{NN}



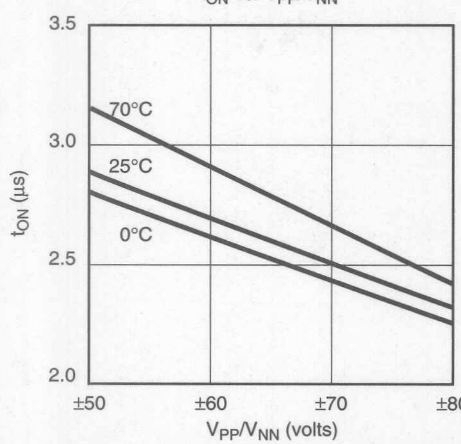
Switch Current vs. Switch Voltage



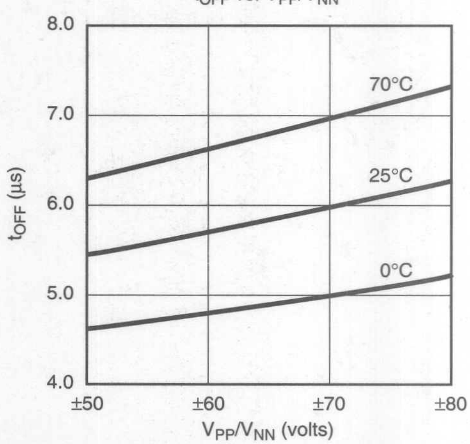
I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



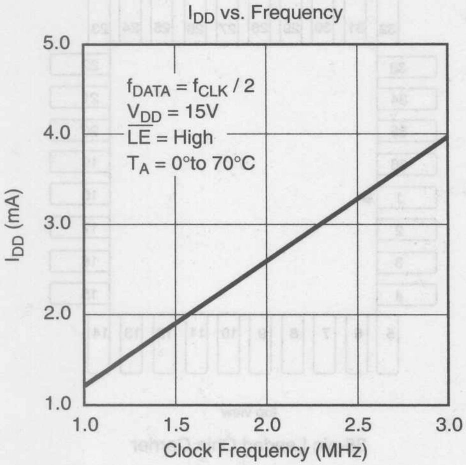
t_{ON} vs. V_{PP}/V_{NN}

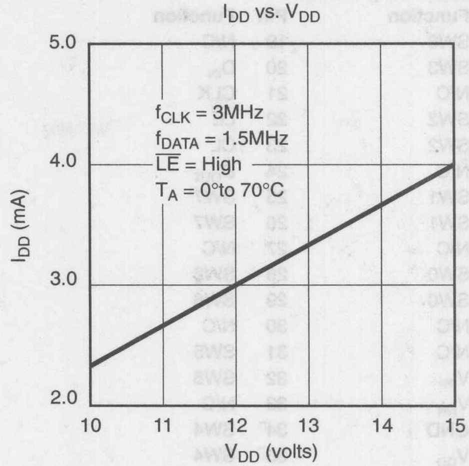


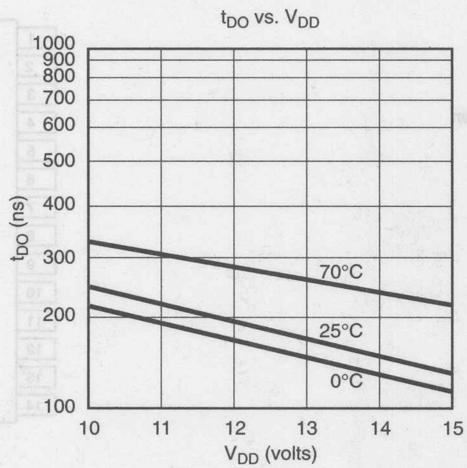
t_{OFF} vs. V_{PP}/V_{NN}



Typical Performance Curves







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Pin Configurations

36-Pin Leaded Chip Carrier

Pin	Function	Pin	Function
1	SW3	19	N/C
2	SW3	20	D_{IN}
3	N/C	21	CLK
4	SW2	22	$\overline{LE}$
5	SW2	23	CL
6	N/C	24	D_{OUT}
7	SW1	25	SW7
8	SW1	26	SW7
9	N/C	27	N/C
10	SW0	28	SW6
11	SW0	29	SW6
12	N/C	30	N/C
13	N/C	31	SW5
14	V_{PP}	32	SW5
15	V_{NN}	33	N/C
16	GND	34	SW4
17	V_{DD}	35	SW4
18	N/C	36	N/C

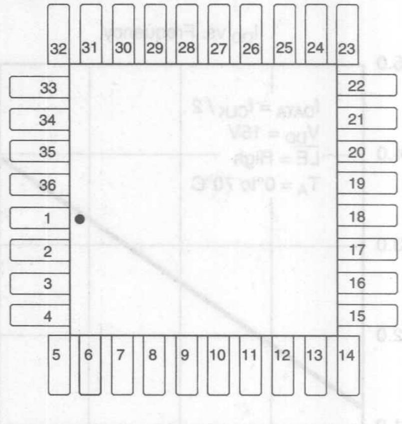
28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

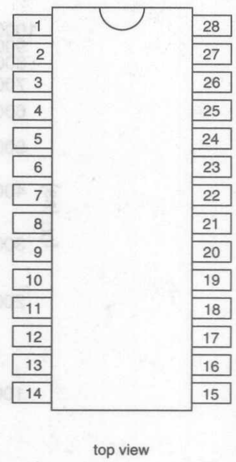
28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

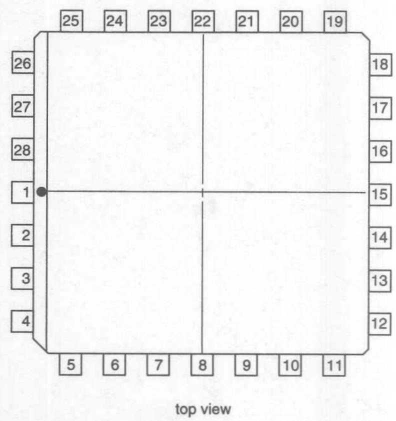
Package Outlines



36-pin Leaded Chip Carrier



28-pin DIP



28-pin J-lead Package

Supertex inc.

8-Channel High Voltage Analog Switch

Ordering Information

$V_{PP} - V_{NN}$	Package Options			
	24-pin ceramic*† side-brazed DIP	Die in waffle pack	24-pin plastic DIP	28-lead plastic chip carrier
140V	HV2114C	HV2114X	HV2114P	HV2114PJ
160V	HV2116C	HV2116X	HV2116P	HV2116PJ

* Consult factory for Cerdip and Ceramic LCC availability.
† Consult factory for MIL-STD-883 processing. See page 5-3 for process flow.

Features

- HVCMOS® technology for high performance
- Very low quiescent power dissipation – 10µA
- Output On-resistance typically 22 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 50dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- On-chip shift register, and latch logic circuitry
- Flexible high voltage supplies
- Surface mount package available

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +160V†
V_{NN} Negative high voltage supply	+0.5V to -160V†
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	Plastic Package 0.8W Ceramic Package 2.0W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.
† For HV2116

General Description

This device is an 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

This IC is suitable for various combinations of high voltage supplies, e.g., for HV2116 +40V/-120V, or +80V/-80V or +150V/-10V.

Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)*

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions	
Small Signal Switch (ON) Resistance	R_{ONS}		30		26	32		35	ohms	$I_{SIG} = 5mA$	$V_{PP} = 40V$,
			25		22	27		32		$I_{SIG} = 200mA$	$V_{NN} = -120V$
			25		22	27		30		$I_{SIG} = 5mA$	$V_{PP} = 80V$,
			18		18	20		23		$I_{SIG} = 200mA$	$V_{NN} = -80V$
			23		20	25		30		$I_{SIG} = 5mA$	$V_{PP} = 150V$,
			22		16	25		27		$I_{SIG} = 200mA$	$V_{NN} = -10V$
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	$I_{SW} = 5mA$, $V_{PP} = 80V$, $V_{NN} = -80V$	
Large Signal Switch (ON) Resistance	R_{ONL}				13	22			ohms	$V_{SIG} = V_{PP}-10V$, $I_{SIG} = 1A$	
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	$V_{SIG} = V_{PP}-10V$ and $V_{NN}+10V$	
DC Offset Switch Off			300		100	300		300	mV	$R_L = 100K\Omega$	
DC Offset Switch On			500		100	500		500	mV	$R_L = 100K\Omega$	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS OFF	
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	ALL SWS OFF	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS ON $I_{SW} = 5mA$	
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	ALL SWS ON $I_{SW} = 5mA$	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	$V_{SIG} \le 0.1\%$ duty cycle	
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%	
I_{PP} Supply Current	I_{PP}		6.5			7.0		8.0	mA	$V_{PP} = 40V$, $V_{NN} = -120V$	50KHz Output Switching Frequency with no load
			4.0			5.0		5.5		$V_{PP} = 80V$, $V_{NN} = -80V$	
			4.0			5.0		5.5		$V_{PP} = 150V$, $V_{NN} = -10V$	
I_{NN} Supply Current	I_{NN}		6.5			7.0		8.0	mA	$V_{PP} = 40V$, $V_{NN} = -120V$	
			4.0			5.0		5.5		$V_{PP} = 80V$, $V_{NN} = -80V$	
			4.0			5.0		5.5		$V_{PP} = 150V$, $V_{NN} = -10V$	
Logic Supply Average Current	I_{DD}		6.0		4.0	6.0		6.0	mA	$f_{CLK} = 3MHz$,	
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA		
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	$V_{OUT} = V_{DD} - 0.7V$	
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	$V_{OUT} = 0.7V$	

Note:

* For HV2116. For HV2114: $V_{PP} = 40V$, $V_{NN} = -100V$; $V_{PP} = 70V$, $V_{NN} = -70$; $V_{PP} = 130V$, $V_{NN} = -10V$.

Electrical Characteristics

AC Characteristics (over operating conditions V_{DD} = 15V, unless otherwise noted)*

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Time to Turn Off V_{SIG}**	$t_{SIG(OFF)}$			200					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		300		150	330		350	ns	
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_h	35		35			35		ns	
Clock Freq	f_{CLK}		3.0			3.0		3.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Turn On Time			2.0			2.0		2.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ
Turn Off Time			3.0			3.0		3.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ
Maximum V_{SIG} Slew Rate	dv/dt		10			10		10	V/ns	V_{PP} = 150V, V_{NN} =-10V
			10			10		10		V_{PP} = 80V, V_{NN} = -80V
			10			10		10		V_{PP} = 40V, V_{NN} = -120V
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5MHz, 1KΩ//15pF load
		-45		-45	-50		-45		dB	f = 5MHz, 50Ω load
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}		300			300		300	mA	300ns pulse width, 2.0% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz

Note:

* For HV2116. For HV2114: V_{PP} = 40V, V_{NN} = -100V; V_{PP} = 70V, V_{NN} = -70V; V_{PP} = 130V, V_{NN} = -10V.

**Time required for analog signal to turn off before output switch turns off (critical timing).

Electrical Characteristics

AC Characteristics (over operating conditions V_{DD} = 15V, unless otherwise noted)*

Characteristics	Sym	+25°C			Units	Test Conditions
		min	typ	max		
Output Voltage Spike	$+V_{SPK}$		1.0		V	V_{PP} = 40V, V_{NN} = -120V
	$-V_{SPK}$		3.5			R_L = 50Ω
	$+V_{SPK}$		12			V_{PP} = 80V, V_{NN} = -80V
	$-V_{SPK}$		18			R_L = 50Ω
	$+V_{SPK}$		6.0			V_{PP} = 150V, V_{NN} = -10V
	$-V_{SPK}$		9.0			R_L = 50Ω
Charge Injection	Q		1700		pC	V_{PP} = 80V, V_{NN} = -80V, V_{SIG} = 0V
			850			V_{PP} = 80V, V_{NN} = -80V, V_{SIG} = 70V
			600			V_{PP} = 80V, V_{NN} = -80V, V_{SIG} = -70V

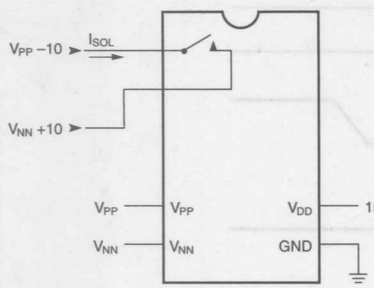
Note:
* For HV2116. For HV2114: V_{PP} = 40V, V_{NN} = -100V; V_{PP} = 70V, V_{NN} = -70V; V_{PP} = 130V, V_{NN} = -10V.

Operating Conditions*

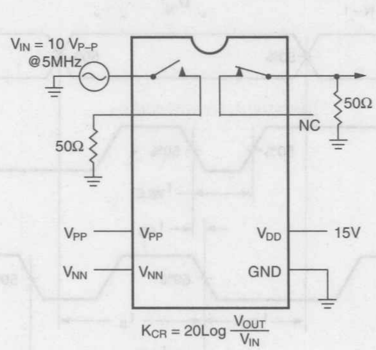
Symbol	Parameter	Device		Value
		HV2114	HV2116	
V_{DD}	Logic power supply voltage	X	X	10.0 V to 15.5 V
V_{PP}	Positive high voltage supply	X		40V to V_{NN}+ 140V
			X	40V to V_{NN}+ 160V
V_{NN}	Negative high voltage supply	X		-10.0V to -100V
			X	-10.0V to -120V
V_{IH}	High-level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0V to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +10V to V_{PP} -10
T_A	Operating free air-temperature	X	X	0°C to 70°C

Note:
* Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transistion.
Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.

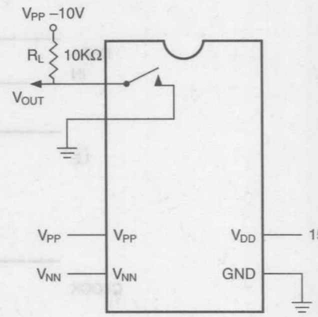
Test Circuits



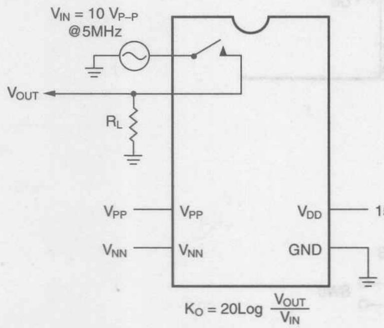
Switch OFF Leakage



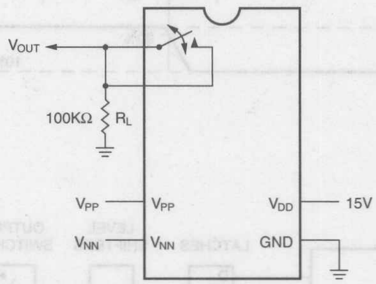
Crosstalk



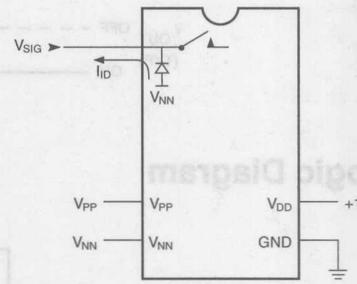
T_{ON}/T_{OFF} Test Circuit



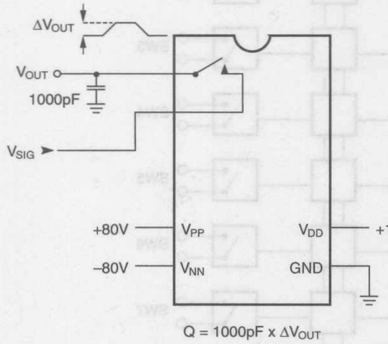
OFF Isolation



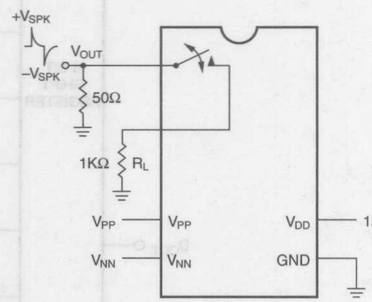
DC Offset ON/OFF



Isolation Diode Current

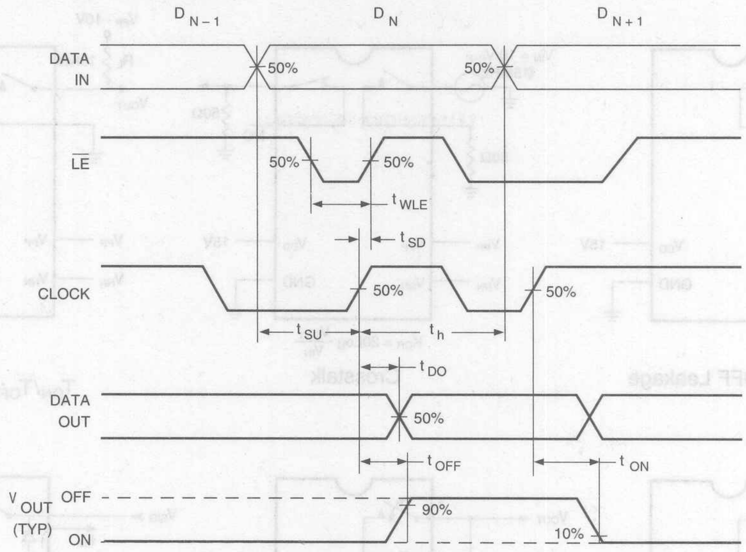


Charge Injection

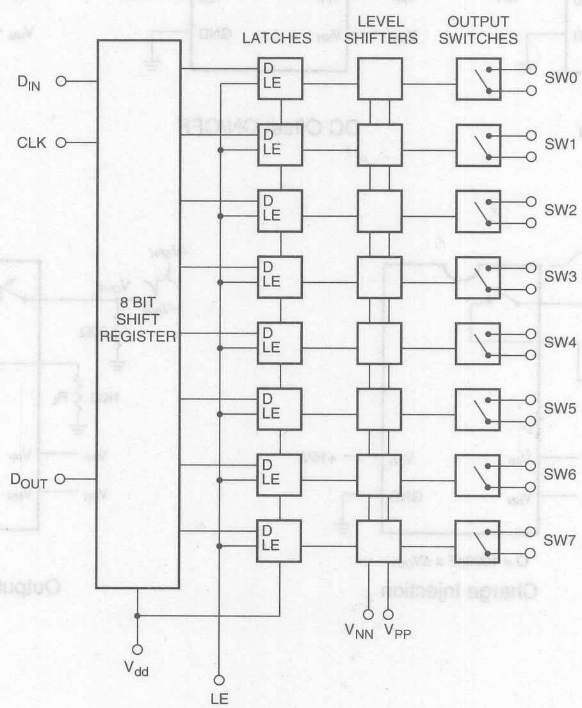


Output Voltage Spike

Logic Timing Waveforms



Logic Diagram



Truth Table

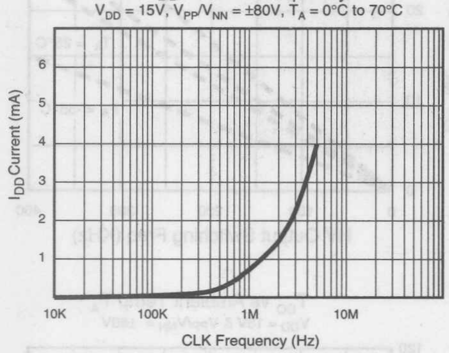
D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

Notes:

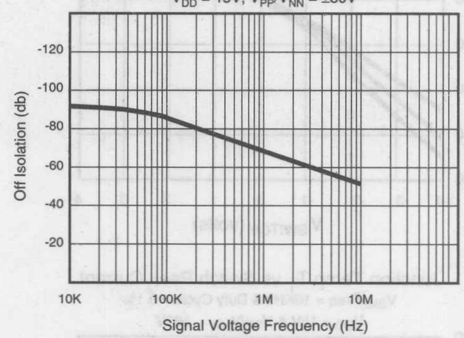
1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clockng has no effect on the switch states if $\overline{LE}$ is H.

Typical Performance Curves

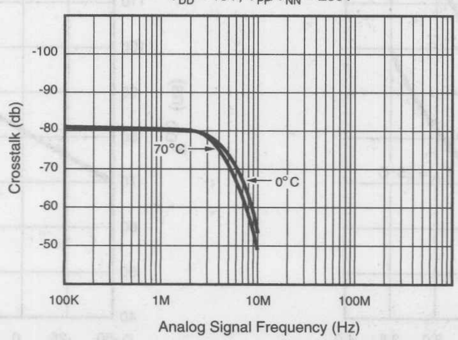
I_{DD} vs CLK Frequency
V_{DD} = 15V, V_{PP}/V_{NN} = ±80V, T_A = 0°C to 70°C



Off Isolation vs Signal Voltage Frequency
V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



Crosstalk vs Analog Signal Frequency
V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



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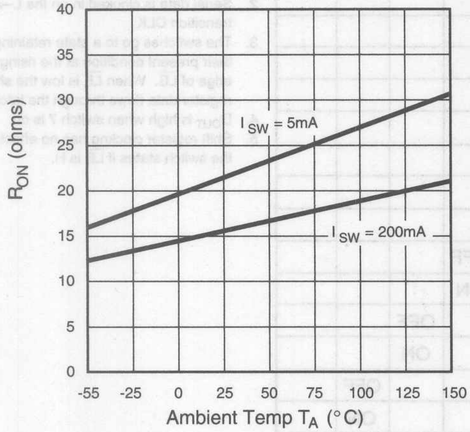
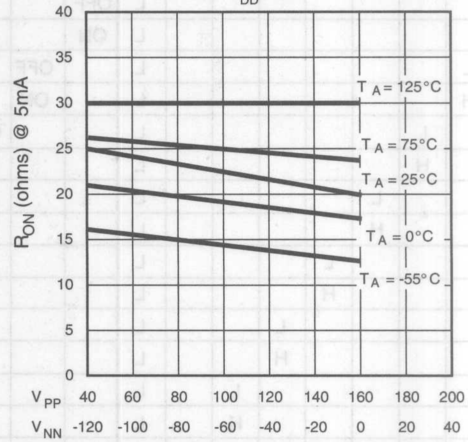
Typical Performance Curves

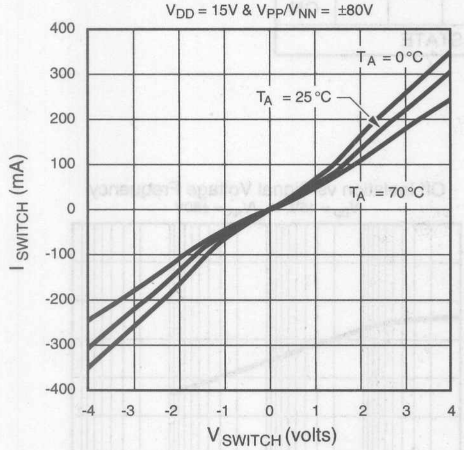
R_{ON} vs Ambient Temp T_A
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



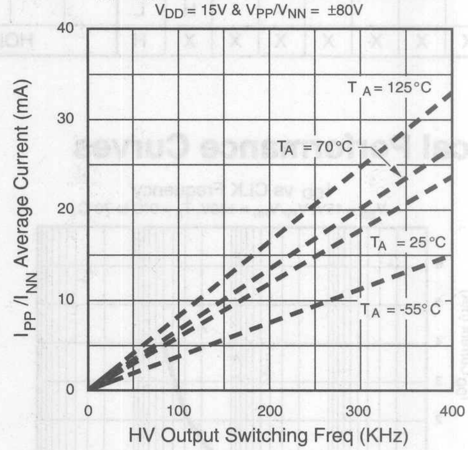
R_{ON} vs V_{PP}/V_{NN}
V_{DD} = 15V



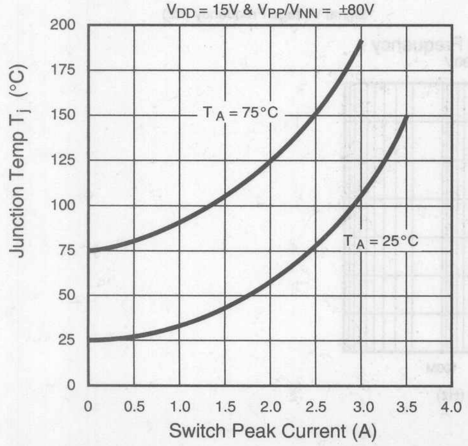
Switch Current vs Switch Voltage Drop
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



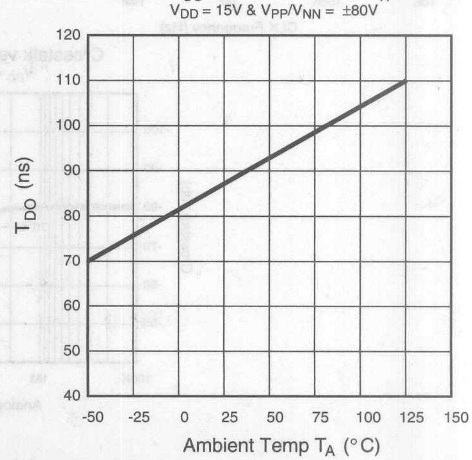
I_{PP}/I_{NN} vs Output Switching Frequency
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Junction Temp T_j vs Switch Peak Current
V_{SIG} Freq = 10KHz & Duty Cycle = 0.1%
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



T_{DO} vs Ambient Temp T_A
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Pin Configurations

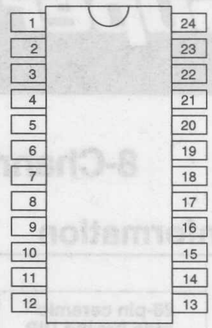
24-Pin DIP

Pin	Function	Pin	Function
1	SW3	13	D_{IN}
2	SW3	14	CLK
3	SW2	15	$\overline{LE}$
4	SW2	16	D_{OUT}
5	SW1	17	SW7
6	SW1	18	SW7
7	SW0	19	SW6
8	SW0	20	SW6
9	V_{PP}	21	SW5
10	V_{NN}	22	SW5
11	GND	23	SW4
12	V_{DD}	24	SW4

28-Pin J-Lead

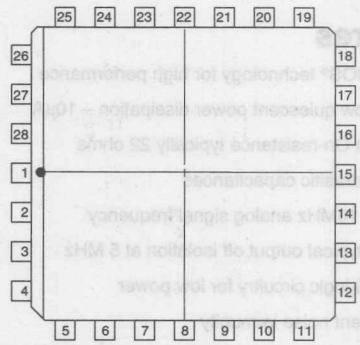
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	N/C	19	D_{OUT}
6	N/C	20	SW7
7	SW1	21	SW7
8	SW1	22	SW6
9	SW0	23	SW6
10	SW0	24	N/C
11	V_{PP}	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

Package Outlines



top view

24-pin DIP



top view

28-pin J-lead Package

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8-Channel High Voltage Analog Switch

Ordering Information

$V_{PP} - V_{NN}$	Package Options			
	28-pin ceramic*† side-brazed DIP	Die in waffle pack	28-pin plastic DIP	28-lead plastic chip carrier
140V	HV2214C	HV2214X	HV2214P	HV2214PJ
160V	HV2216C	HV2216X	HV2216P	HV2216PJ

* Consult factory for Cerdip and Ceramic LCC availability.
† Consult factory for MIL-STD-883 processing.

Features

- HVCMOS® technology for high performance
- Very low quiescent power dissipation – 10µA
- Output On-resistance typically 22 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- 50dB typical output off isolation at 5 MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- On-chip shift register, latch and clear logic circuitry
- Flexible high voltage supplies
- Surface mount package available

General Description

This device is an 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

This IC is suitable for various combinations of high voltage supplies, e.g., for HV2216 +40V/-120V, or +80V/-80V or +150V/-10V.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} Supply voltage	174V†
V_{PP} Positive high voltage supply	-0.5V to +160V†
V_{NN} Negative high voltage supply	+0.5V to -160V†
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog Signal Range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	Plastic Package 0.8W Ceramic Package 2.0W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.
† For HV2216

Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)*

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions	
		min	max	min	typ	max	min	max			
Small Signal Switch (ON) Resistance	R_{ONS}		30		26	32		35	ohms	I_{SIG} = 5mA	V_{PP} = 40V,
			25		22	27		32		I_{SIG} = 200mA	V_{NN} = −120V
			25		22	27		30		I_{SIG} = 5mA	V_{PP} = 80V,
			18		18	20		23		I_{SIG} = 200mA	V_{NN} = −80V
			23		20	25		30		I_{SIG} = 5mA	V_{PP} = 150V,
			22		16	25		27		I_{SIG} = 200mA	V_{NN} = −10V
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	I_{SW} = 5mA, V_{PP} = 80V, V_{NN} = −80V	
Large Signal Switch (ON) Resistance	R_{ONL}				13	22			ohms	V_{SIG} = V_{PP}−10V, I_{SIG} = 1A	
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	V_{SIG} = V_{PP}−10V and V_{NN} +10V	
DC Offset Switch Off			300		100	300		300	mV	R_L = 100KΩ	
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS OFF	
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	ALL SWS OFF	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS ON I_{SW} = 5mA	
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	ALL SWS ON I_{SW} = 5mA	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V_{SIG} ≤ 0.1% duty cycle	
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%	
I_{PP} Supply Current	I_{PP}		6.5			7.0		8.0	mA	V_{PP} = 40V, V_{NN} = −120V	50KHz Output Switching Frequency with no load
			4.0			5.0		5.5		V_{PP} = 80V, V_{NN} = −80V	
			4.0			5.0		5.5		V_{PP} = 150V, V_{NN} = −10V	
I_{NN} Supply Current	I_{NN}		6.5			7.0		8.0	mA	V_{PP} = 40V, V_{NN} = −120V	
			4.0			5.0		5.5		V_{PP} = 80V, V_{NN} = −80V	
			4.0			5.0		5.5		V_{PP} = 150V, V_{NN} = −10V	
Logic Supply Average Current	I_{DD}		6.0		4.0	6.0		6.0	mA	f_{CLK} = 3MHz,	
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA		
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	V_{OUT} = V_{DD} - 0.7V	
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V	

Note:

* For HV2216. For HV2214: V_{PP} = 40V, V_{NN} = -100V; V_{PP} = 70V, V_{NN} = -70; V_{PP} = 130V, V_{NN} = -10V.

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Electrical Characteristics

AC Characteristics (over operating conditions V_{DD} = 15V, unless otherwise noted)*

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Time to Turn Off V_{SIG}**	$t_{SIG(OFF)}$			200					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		300		150	330		350	ns	
Time Width of CL	t_{WCL}	150		150			150		ns	
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_h	35		35			35		ns	
Clock Freq	f_{CLK}		3.0			3.0		3.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Turn On Time			2.0			2.0		2.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ
Turn Off Time			3.0			3.0		3.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ
			10			10		10		V_{PP} = 150V, V_{NN} = -10V
Maximum V_{SIG} Slew Rate	dv/dt		10			10		10	V/ns	V_{PP} = 80V, V_{NN} = -80V
			10			10		10		V_{PP} = 40V, V_{NN} = -120V
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5MHz, 1KΩ//15pF load
		-45		-45	-50		-45		dB	f = 5MHz, 50Ω load
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}		300			300		300	mA	300ns pulse width, 2.0% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz

Note:

* For HV2216. For HV2214: V_{PP} = 40V, V_{NN} = -100V; V_{PP} = 70V, V_{NN} = -70V; V_{PP} = 130V, V_{NN} = -10V.

**Time required for analog signal to turn off before output switch turns off (critical timing).

Electrical Characteristics

AC Characteristics (over operating conditions V_{DD} = 15V, unless otherwise noted)*

Characteristics	Sym	+25°C			Units	Test Conditions
		min	typ	max		
Output Voltage Spike	$+V_{SPK}$		1.0		V	V_{PP} = 40V, V_{NN} = -120V
	$-V_{SPK}$		3.5			$R_L = 50\Omega$
	$+V_{SPK}$		12			V_{PP} = 80V, V_{NN} = -80V
	$-V_{SPK}$		18			$R_L = 50\Omega$
	$+V_{SPK}$		6.0			V_{PP} = 150V, V_{NN} = -10V
	$-V_{SPK}$		9.0			$R_L = 50\Omega$
Charge Injection	Q		1700		pC	V_{PP} = 80V, V_{NN} = -80V, V_{SIG} = 0V
			850			V_{PP} = 80V, V_{NN} = -80V, V_{SIG} = 70V
			600			V_{PP} = 80V, V_{NN} = -80V, V_{SIG} = -70V

Note:
* For HV2216. For HV2214: V_{PP} = 40V, V_{NN} = -100V; V_{PP} = 70V, V_{NN} = -70V; V_{PP} = 130V, V_{NN} = -10V.

Operating Conditions*

Symbol	Parameter	Device		Value
		HV2214	HV2216	
V_{DD}	Logic power supply voltage	X	X	10.0 V to 15.5 V
V_{PP}	Positive high voltage supply	X		40V to V_{NN}+ 140V
			X	40V to V_{NN}+ 160V
V_{NN}	Negative high voltage supply	X		-10.0V to -100V
			X	-10.0V to -120V
V_{IH}	High-level input voltage	X	X	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	X	X	0V to 2.0V
V_{SIG}	Analog signal voltage peak to peak	X	X	V_{NN} +10V to V_{PP} -10
T_A	Operating free air-temperature	X	X	0°C to 70°C

Note:
* Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transistion.
Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.

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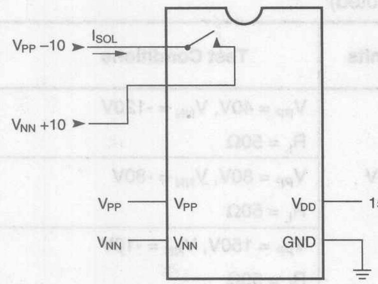
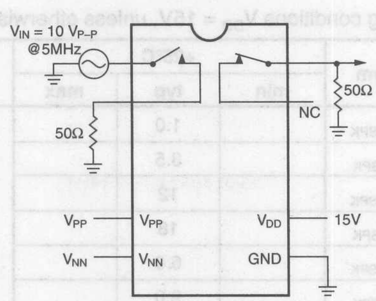
Test Circuits

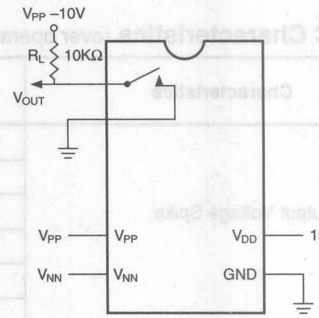


Switch OFF Leakage

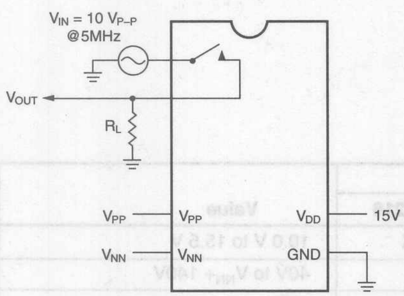


$K_{CR} = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

Crosstalk

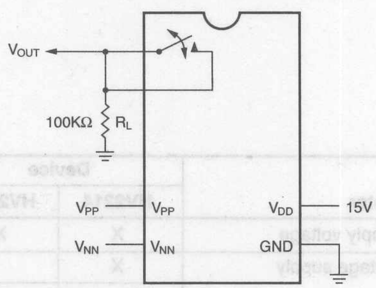


T_{ON}/T_{OFF} Test Circuit

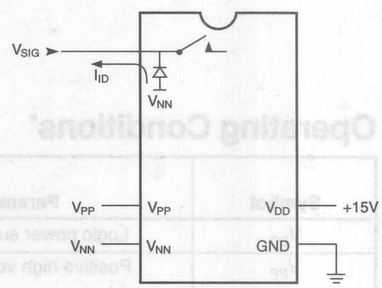


$K_O = 20\text{Log}\,\frac{V_{OUT}}{V_{IN}}$

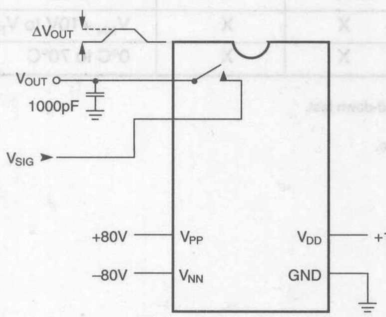
OFF Isolation



DC Offset ON/OFF

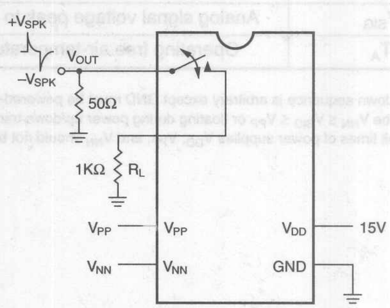


Isolation Diode Current



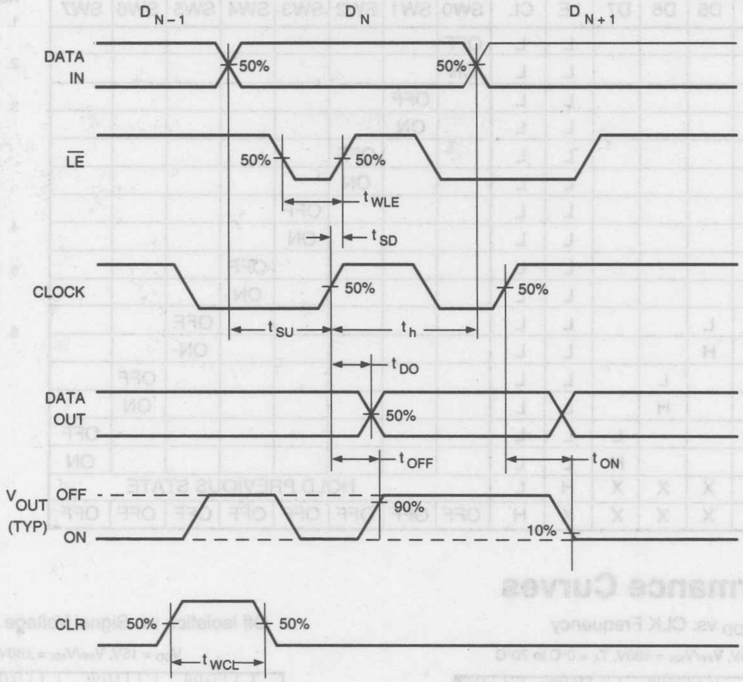
$Q = 1000\text{pF} \times \Delta V_{OUT}$

Charge Injection

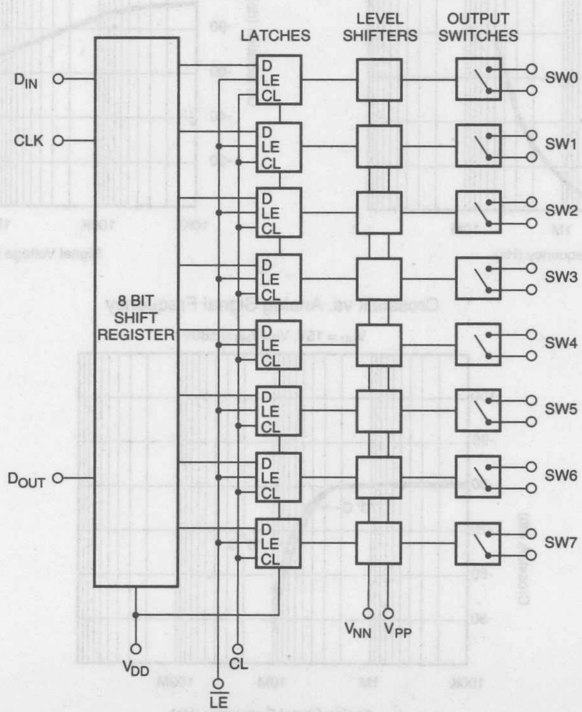


Output Voltage Spike

Logic Timing Waveforms



Logic Diagram



Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

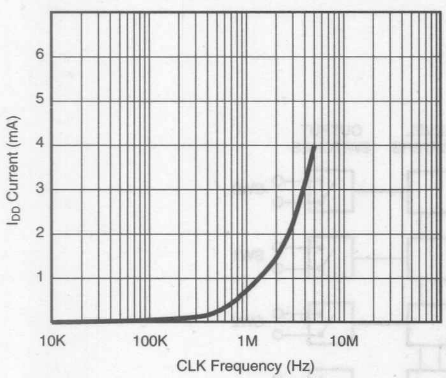
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

Typical Performance Curves

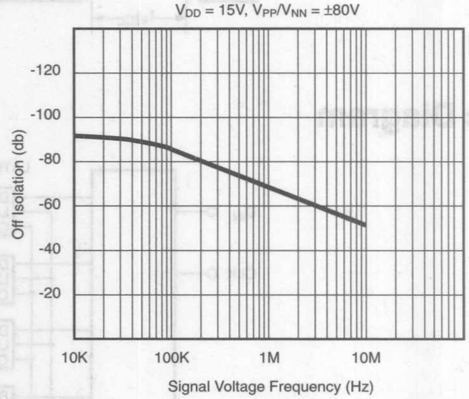
I_{DD} vs. CLK Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V, T_A = 0°C to 70°C



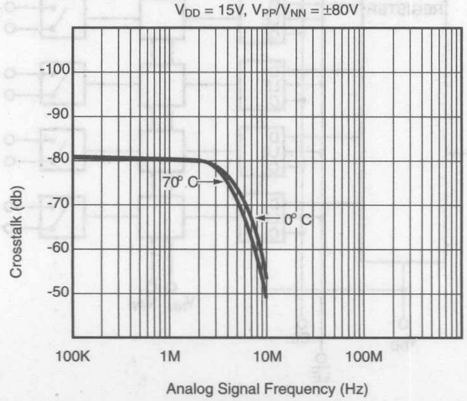
Off Isolation vs. Signal Voltage Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



Crosstalk vs. Analog Signal Frequency

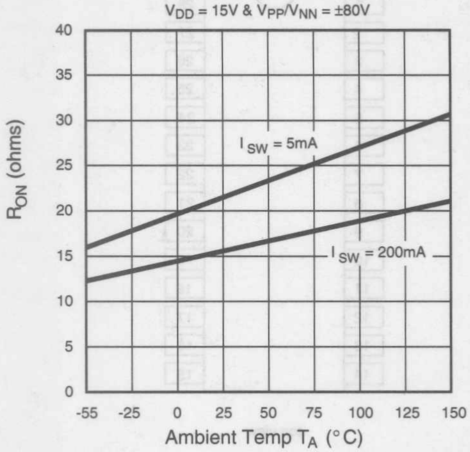
V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



Typical Performance Curves

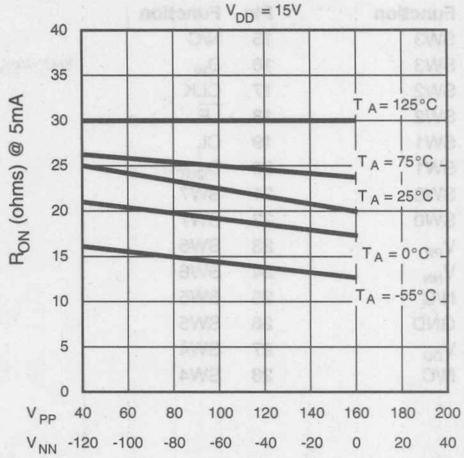
R_{ON} vs Ambient Temp T_A

V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



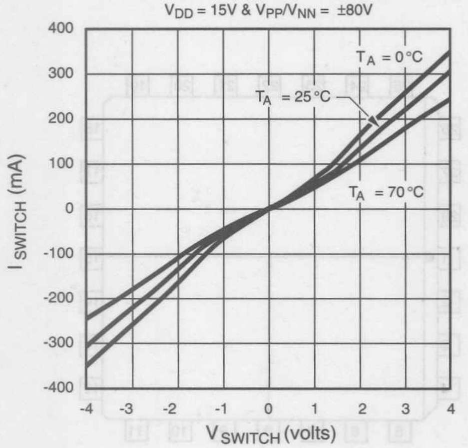
R_{ON} vs V_{PP}/V_{NN}

V_{DD} = 15V



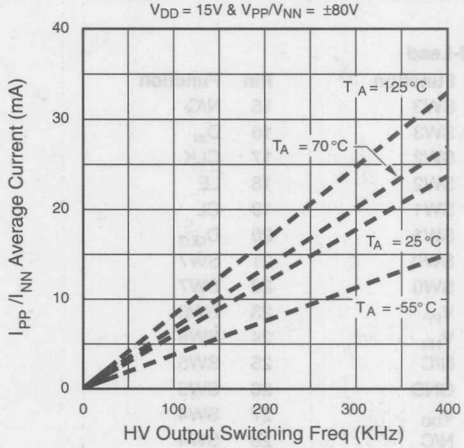
Switch Current vs Switch Voltage Drop

V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



I_{PP}/I_{NN} vs Output Switching Frequency

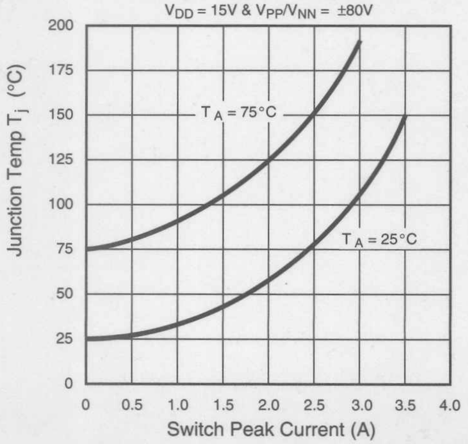
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Junction Temp T_j vs Switch Peak Current

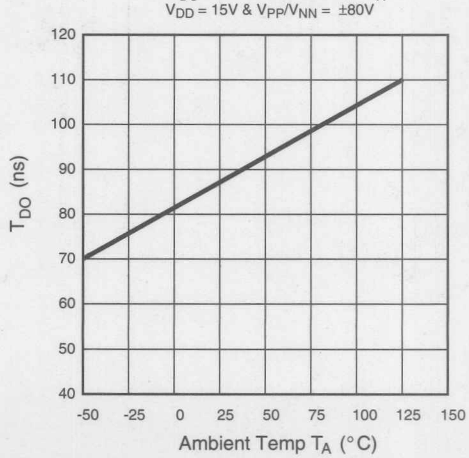
V_{SIG} Freq = 10KHz & Duty Cycle = 0.1%

V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



T_{DO} vs Ambient Temp T_A

V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Pin Configurations

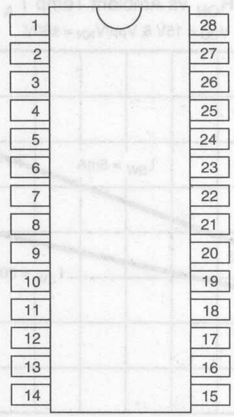
28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

28-Pin J-Lead

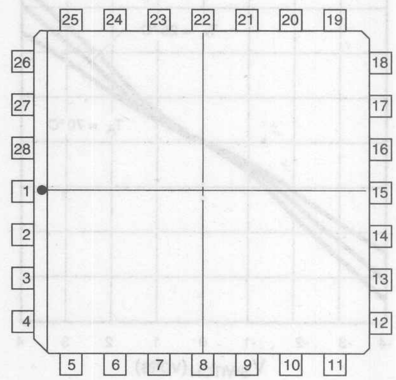
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

Package Outlines



top view

28-pin DIP



top view

28-pin J-lead Package

Supertex inc.

Objective

Low Charge Injection
8-Channel High Voltage Analog Switch

Ordering Information

$V_{PP} - V_{NN}$	Package Options			
	28-pin ceramic*† side-brazed DIP	Die in waffle pack	28-pin plastic DIP	28-lead plastic chip carrier
200V	HV20420C	HV20420X	HV20420P	HV20420PJ

* Consult factory for Cerdip and Ceramic LCC availability.
† Consult factory for MIL-STD-883 processing.

Features

- ☐ HVCMOS® technology for high performance
- ☐ Low charge injection
- ☐ Very low quiescent power dissipation – 10µA
- ☐ Output On-resistance typically 22 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 60dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power
- ☐ Excellent noise immunity
- ☐ On-chip shift register, latch and clear logic circuitry
- ☐ Flexible high voltage supplies
- ☐ Surface mount package available

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} Supply voltage	220V
V_{PP} Positive high voltage supply	-0.5V to V_{NN} +200V
V_{NN} Negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog Signal Range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	Plastic Package 0.8W Ceramic Package 2.0W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

General Description

This device is a low charge injection 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

This IC is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +50V/–150V, or +100V/–100V.

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Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions	
Small Signal Switch (ON) Resistance	R_{ONS}		30		26	32		35	ohms	I_{SIG} = 5mA	V_{PP} = +50V,
			25		22	27		32		I_{SIG} = 200mA	V_{NN} = -150V
			25		22	27		30		I_{SIG} = 5mA	V_{PP} = +100V,
			18		18	20		23		I_{SIG} = 200mA	V_{NN} = -100V
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	I_{SW} = 5mA, V_{PP} = +100V, V_{NN} = -100V	
Large Signal Switch (ON) Resistance	R_{ONL}				15				ohms	V_{SIG} = V_{PP} -10V, I_{SIG} = 1.0A	
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	V_{SIG} = V_{PP}−10V to V_{NN} +10V	
DC Offset Switch Off			300		100	300		300	mV	R_L = 100KΩ	
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS OFF	
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	ALL SWS OFF	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS ON I_{SW} = 5mA	
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	ALL SWS ON I_{SW} = 5mA	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V_{SIG} duty cycle ≤ 0.1%	
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%	
I_{PP} Supply Current	I_{PP}		8.1			8.8		10.0	mA	V_{PP} = +50V, V_{NN} = -150V	50KHz Output Switching Frequency with no load
			5.0			6.3		6.9	mA	V_{PP} = +100V, V_{NN} = -100V	
I_{NN} Supply Current	I_{NN}		8.1			8.8		10.0	mA	V_{PP} = +50V, V_{NN} = -150V	
			5.0			6.3		6.9	mA	V_{PP} = +100V, V_{NN} = -100V	
Logic Supply Average Current	I_{DD}		6.0		4.0	6.0		6.0	mA	f_{CLK} = 3MHz	
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA		
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	V_{OUT} = V_{DD} - 0.7V	
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V	

Electrical Characteristics

AC Characteristics (over operating conditions V_{DD} = 15V, unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Time to Turn Off V_{SIG}*	$t_{SIG(OFF)}$			0					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		175			175		190	ns	
Time Width of CL	t_{WCL}	150		150			150		ns	
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_h	35		35			35		ns	
Clock Freq	f_{CLK}		5.0			5.0		5.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Turn On Time			5.0			5.0		5.0	µs	$V_{SIG} = V_{PP}$ -10V
Turn Off Time			5.0			5.0		5.0	µs	$V_{SIG} = V_{PP}$ -10V
Maximum V_{SIG} Slew Rate	dv/dt					13			V/ns	V_{PP} = +50V, V_{NN} = -150V
						13				V_{PP} = +100V, V_{NN} = -100V
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5.0MHz, 1KΩ//15pF load
		-45		-45	-60		-45		dB	f = 5.0MHz, 50Ω load
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5.0MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}		300			300		300	mA	300ns pulse width, 2.0% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz
Output Voltage Spike	$+V_{SPK}$				150				mV	V_{PP} = +100V, V_{NN} = -100V, R_L = 50Ω
	$-V_{SPK}$				150					

*Time required for analog signal to turn off before output switch turns off.

Operating Conditions*

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	10.0 V to 15.5 V
V_{PP}	Positive high voltage supply	50V to V_{NN}+ 200V
V_{NN}	Negative high voltage supply	-100V to -150V
V_{IH}	High-level input voltage	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	0V to 2.0V
V_{SIG}	Analog signal voltage peak to peak	V_{NN} +10V to V_{PP} -10
T_A	Operating free air-temperature	0°C to 70°C

Note:

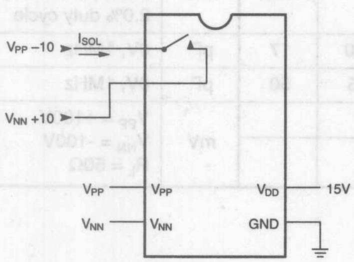
* Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transistion.
Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.

Truth Table

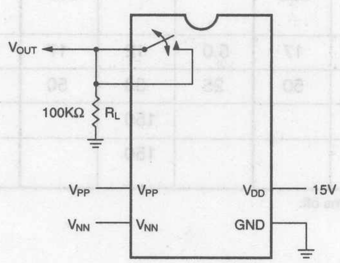
D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes:
1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

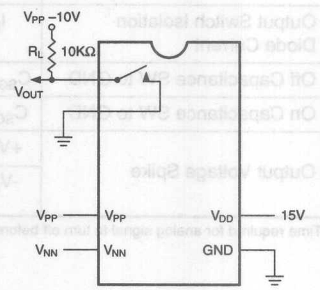
Test Circuits



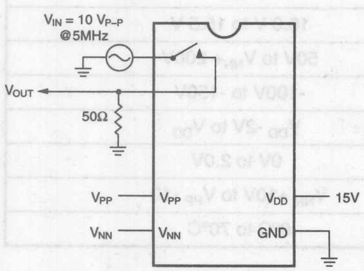
Switch OFF Leakage



DC Offset ON/OFF

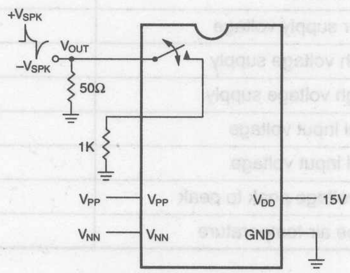


T_{ON} / T_{OFF}

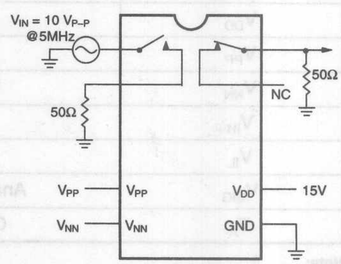


$KO = 20Log\frac{V_{OUT}}{V_{IN}}$

OFF Isolation



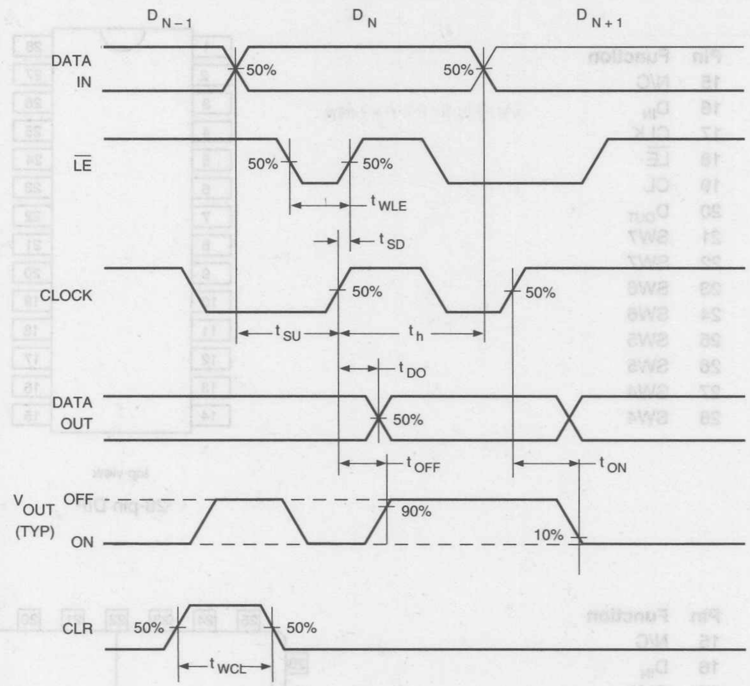
Output Voltage Spike



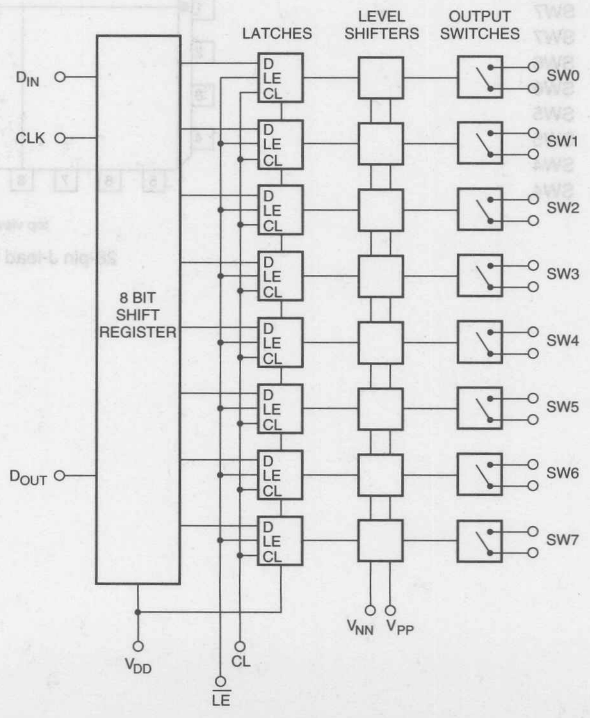
$K_{CR} = 20Log\frac{V_{OUT}}{V_{IN}}$

Crosstalk

Logic Timing Waveforms



Logic Diagram



Pin Configurations

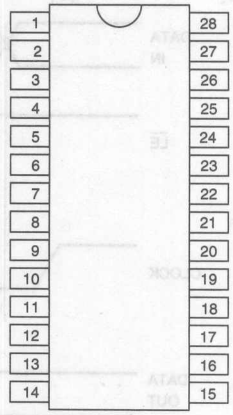
28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	V_{PP}	24	SW6
11	N/C	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

28-Pin J-Lead

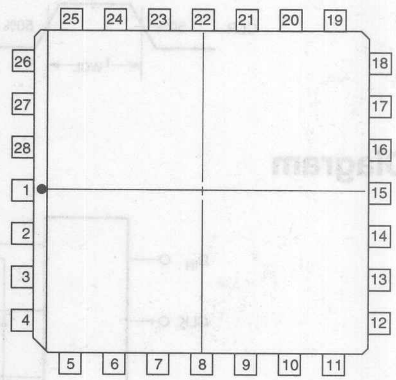
Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	V_{PP}	24	SW6
11	N/C	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

Package Outlines



top view

28-pin DIP



top view

28-pin J-lead Package

Supertex inc.

HV217
HV218

Low Charge Injection
8-Channel High Voltage Analog Switch

Ordering Information

Operating V_{PP}	$V_{PP} - V_{NN}$	Package Options: 24-pin ceramic*† side-brazed DIP	Die in waffle pack	24-pin plastic DIP	28-lead plastic chip carrier	28-lead SOW
40V to 80V	140V	HV21714C	HV21714X	HV21714P	HV21714PJ	HV21714WG
	160V	HV21716C	HV21716X	HV21716P	HV21716PJ	HV21716WG
80V to 150V	140V	HV21814C	HV21814X	HV21814P	HV21814PJ	HV21814WG
	160V	HV21816C	HV21816X	HV21816P	HV21816PJ	HV21816WG

* Consult factory for Cerdip and Ceramic LCC availability.
† Consult factory for MIL-STD-883 processing.

Features

- ☐ HVCMOS® technology for high performance
- ☐ Low charge injection
- ☐ Very low quiescent power dissipation – 10µA
- ☐ Output On-resistance typically 22 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 50dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power
- ☐ Excellent noise immunity
- ☐ On-chip shift register and latch logic circuitry
- ☐ Flexible high voltage supplies
- ☐ Surface mount package available

General Description

This device is a low charge injection 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bi-lateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

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Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +160V†
V_{NN} negative high voltage supply	+0.5V to -160V†
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	Plastic Package 0.8W Ceramic Package 2.0W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV21716 and HV21816

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD}= 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Small Signal Switch (ON)	R_{ONS}		24		22	25		28	ohms	I_{SIG} = 5mA
Resistance	R_{ONS}		18		18	20		23	ohms	I_{SIG} = 200mA
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	I_{SW} = 5mA
Large Signal Switch (ON) Resistance	R_{ONL}				13	22			ohms	V_{SIG} = V_{PP} -10V, I_{SIG} = 1.0A
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	V_{SIG} = V_{PP} -10V and V_{NN} +10V
DC Offset Switch Off			300		100	300		300	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS ON I_{SW} = 5mA
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V_{SIG} ≤ 0.1% Duty Cycle
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%
I_{PP} Supply Current	I_{PP}		4.0		3.5	5.0		5.5	mA	HV output switching frequency = 50KHz
I_{NN} Supply Current	I_{NN}		4.0		3.5	5.0		5.5	mA	
Logic Supply Average Current	I_{DD}		6.0		4.0	6.0		6.0	mA	f_{CLK} = 3MHz
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA	
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V

AC Characteristics

Characteristics	Sym	0°C min	0°C max	+25°C min	+25°C typ	+25°C max	+70°C min	+70°C max	Units	Test Conditions
Time to Turn Off V_{SIG}**	$t_{SIG\ (OFF)}$			0					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		175			175		190	ns	
Turn On Time	t_{ON}		3.0			3.0		3.0	µs	$R_L = 10K\Omega$
Turn Off Time	t_{OFF}		5.0			5.0		5.0	µs	$R_L = 10K\Omega$
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5MHz, 1KΩ// 15pF load
		-45		-45	-50		-45		dB	f = 5MHz, 50Ω load
Clock Freq	f_{CLK}		5.0			5.0		5.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_H	35		35			35		ns	
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5MHz, 50Ω load
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz
Output Voltage Spike	$+V_{SPK}$				150				mV	V_{PP} = +80V, V_{NN} = -80V, R_L = 50Ω
	$-V_{SPK}$				150					

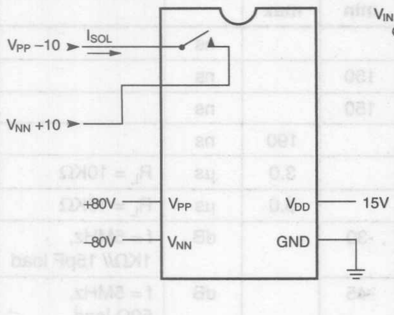
* For HV21716 and HV21816. For HV21714 and HV21814: V_{PP} = 70V, V_{NN} = -70V and V_{DD} = 15V.
** Time required for analog signal to turn off before output switch turns off (critical timing).

Operating Conditions*

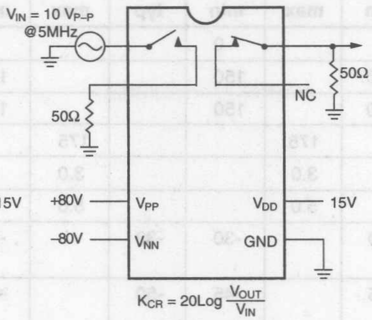
Symbol	Device HV21714	HV21716	HV21814	HV21816	Value
V_{PP}	X				40V to 70V
		X			40V to 80V
			X		70V to 130V
				X	80V to 150V
V_{NN}	X		X		-10V to V_{PP} -140V
		X		X	-10V to V_{PP} -160V
V_{DD}	X	X	X	X	10V to 15.5V
V_{IH}	X	X	X	X	V_{DD} -2.0V to V_{DD}
V_{IL}	X	X	X	X	0V to 2.0V
V_{SIG}	X	X	X	X	V_{NN} +10V to V_{PP} -10
T_A	X	X	X	X	0°C to 70°C

Note: Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
* V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transistion.
Rise and fall times of power supplies, V_{DD}, V_{PP}, and V_{NN} should not exceed 1.0msec.

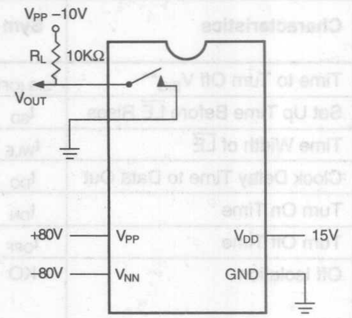
Test Circuits



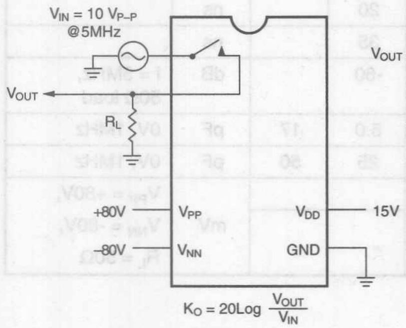
Switch OFF Leakage



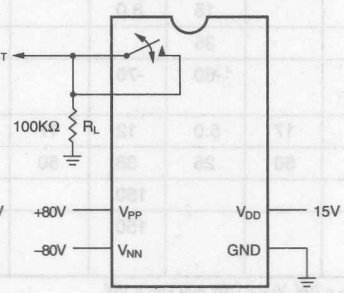
Crosstalk



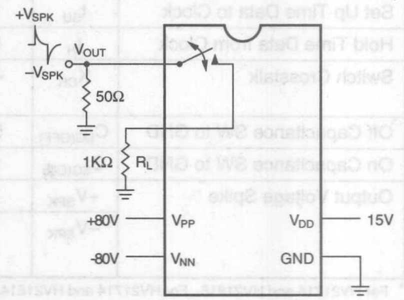
T_{ON}/T_{OFF}



OFF Isolation

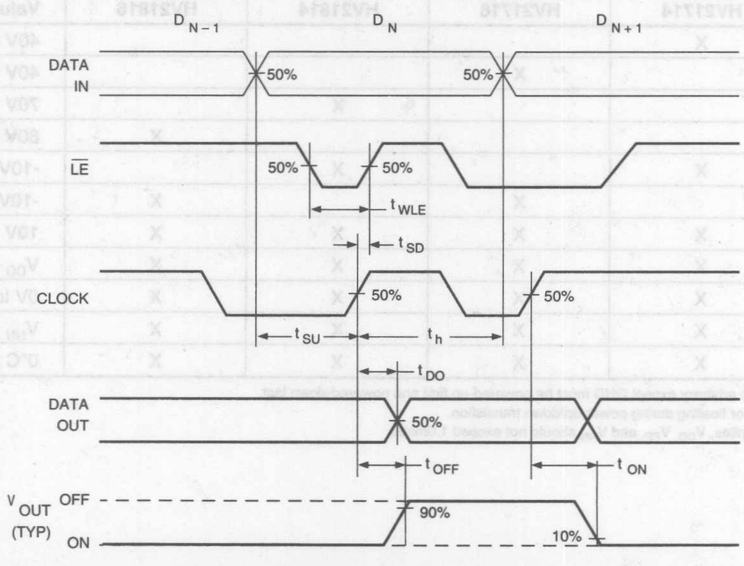


DC Offset ON/OFF

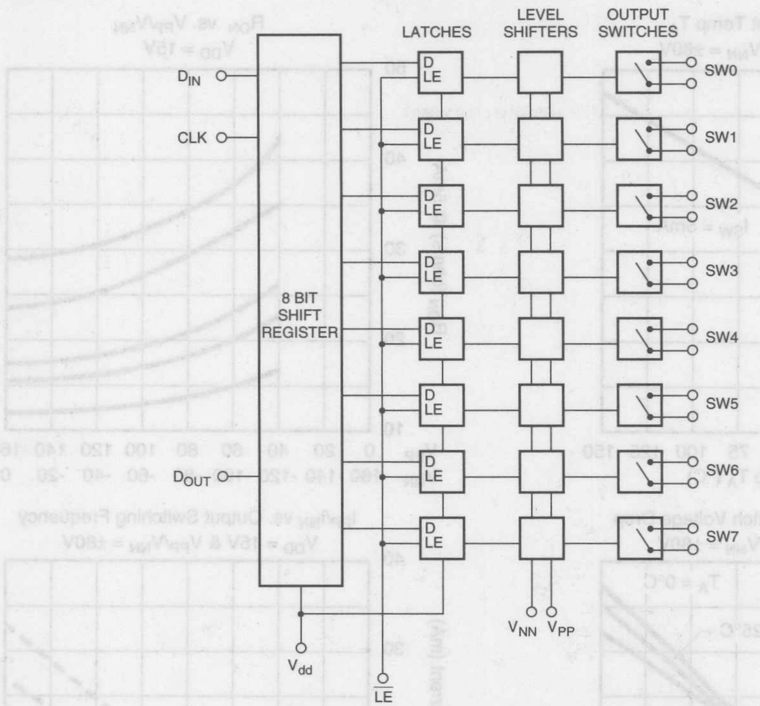


Output Voltage Spike

Logic Timing Waveforms



Logic Diagram



Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clockng has no effect on the switch states if $\overline{LE}$ is H.

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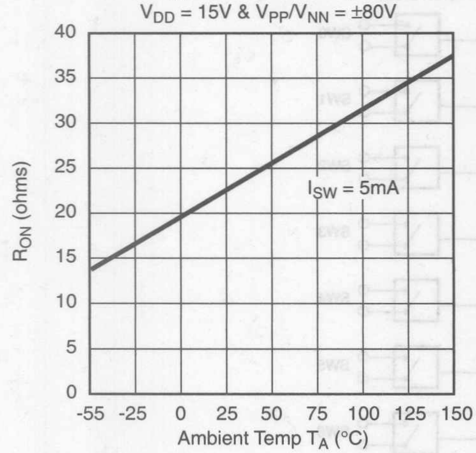
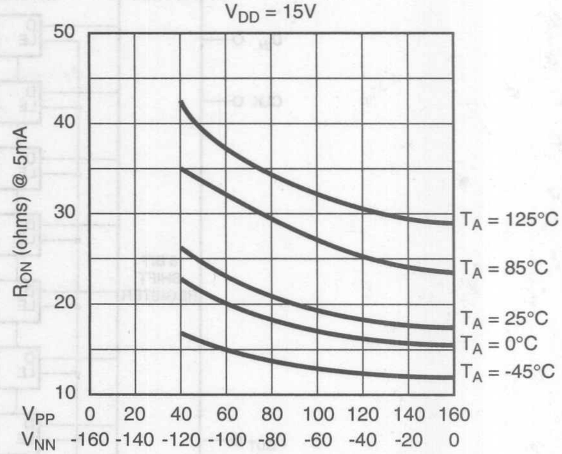
Typical Performance Curves

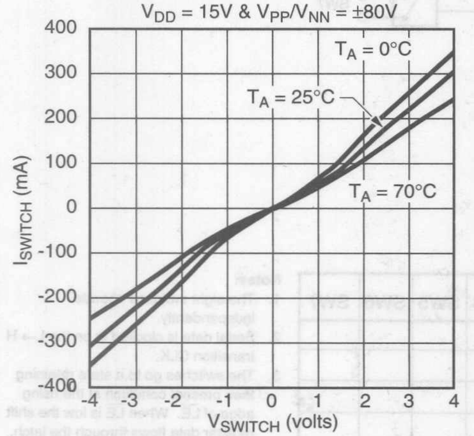
R_{ON} vs. Ambient Temp T_A
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



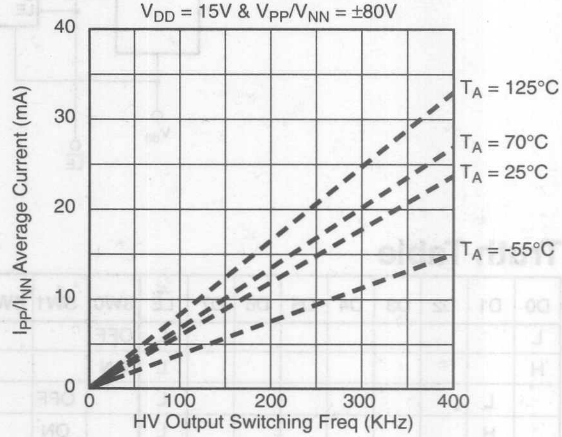
R_{ON} vs. V_{PP}/V_{NN}
V_{DD} = 15V



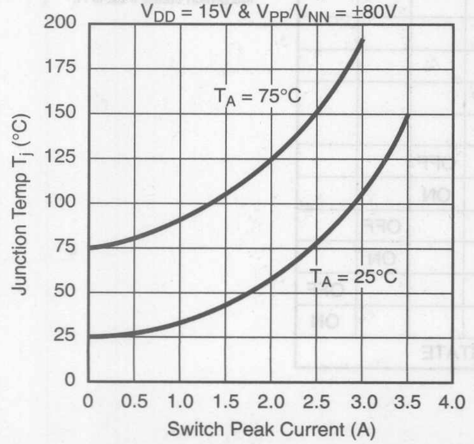
Switch Current vs. Switch Voltage Drop
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



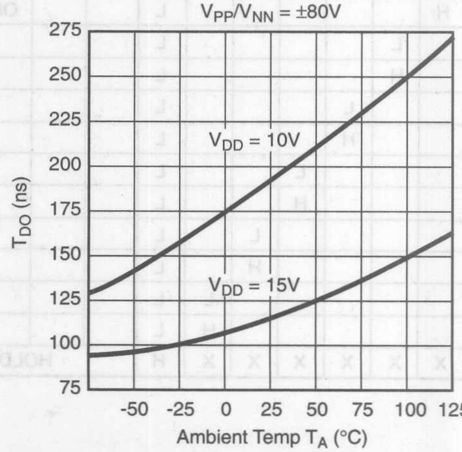
I_{PP}/I_{NN} vs. Output Switching Frequency
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Junction Temp T_j vs. Switch Peak Current
V_{SIG} Freq = 10KHz & Duty Cycle = 0.1%
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V

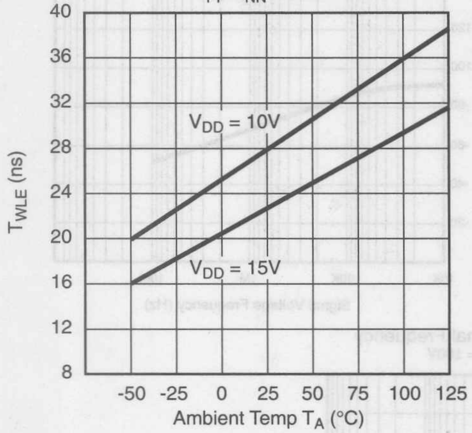


T_{DO} vs. Ambient Temp T_A
V_{PP}/V_{NN} = ±80V

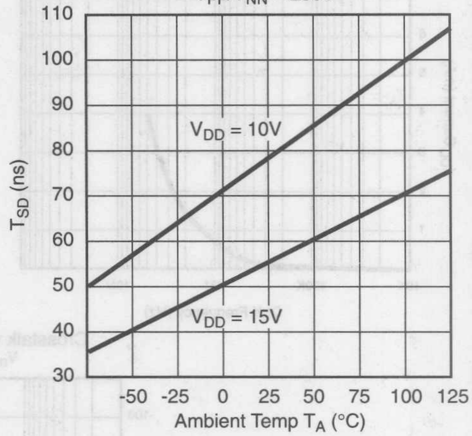


Typical Performance Curves

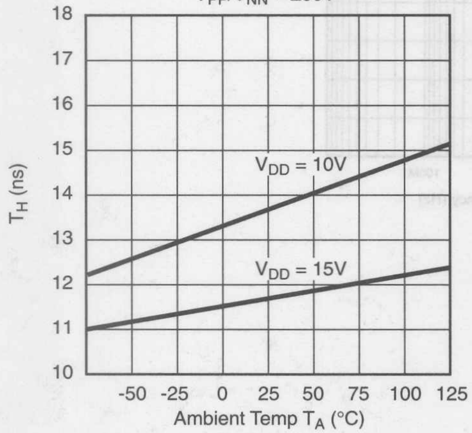
T_{WLE} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



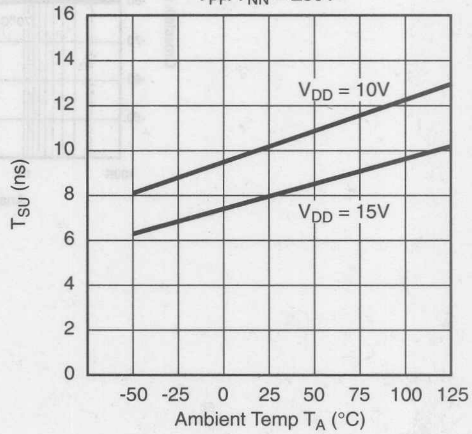
T_{SD} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



T_H vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$

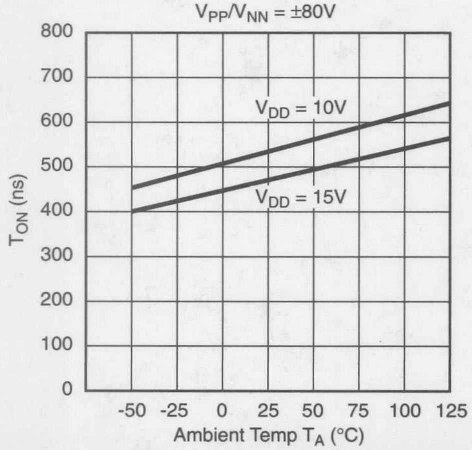


T_{SU} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$

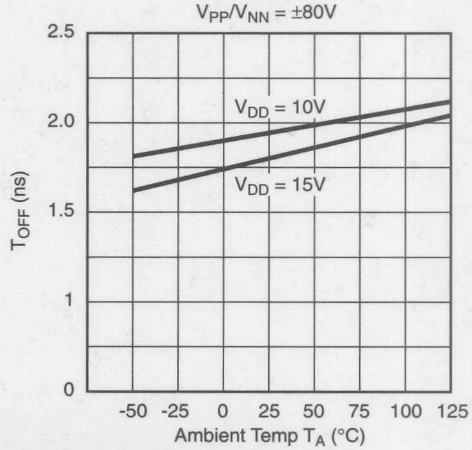


12

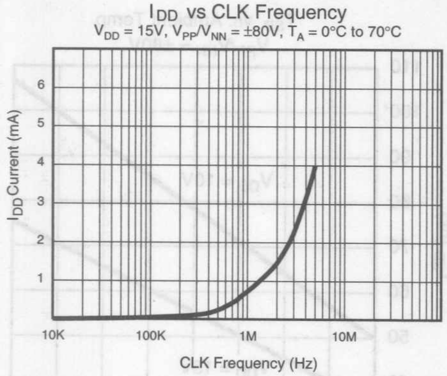
T_{ON} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$

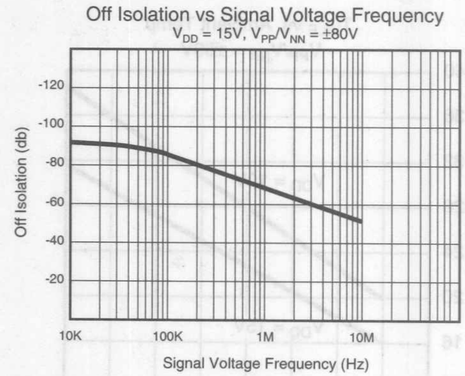


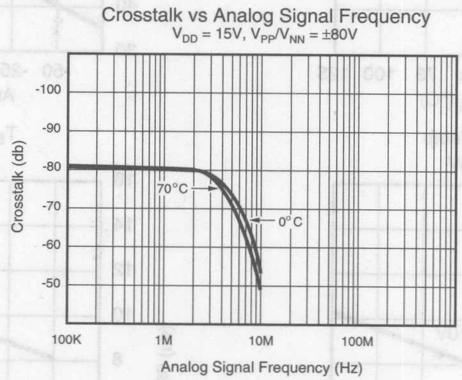
T_{OFF} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



Typical Performance Curves







Pin Configurations

24-Pin DIP

Pin	Function	Pin	Function
1	SW3	13	D_{IN}
2	SW3	14	CLK
3	SW2	15	$\overline{LE}$
4	SW2	16	D_{OUT}
5	SW1	17	SW7
6	SW1	18	SW7
7	SW0	19	SW6
8	SW0	20	SW6
9	V_{PP}	21	SW5
10	V_{NN}	22	SW5
11	GND	23	SW4
12	V_{DD}	24	SW4

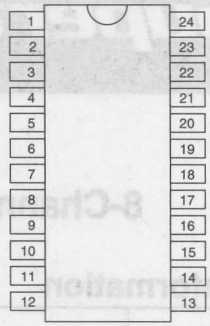
28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	N/C	19	D_{OUT}
6	N/C	20	SW7
7	SW1	21	SW7
8	SW1	22	SW6
9	SW0	23	SW6
10	SW0	24	N/C
11	V_{PP}	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

28-Lead SOW

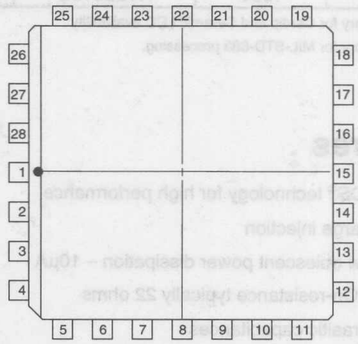
Pin	Function	Pin	Function
1	N/C	15	SW0
2	SW6	16	SW0
3	SW6	17	N/C
4	SW5	18	V_{PP}
5	SW5	19	V_{NN}
6	SW4	20	GND
7	SW4	21	V_{DD}
8	SW3	22	D_{IN}
9	SW3	23	CLK
10	SW2	24	$\overline{LE}$
11	SW2	25	N/C
12	SW1	26	D_{OUT}
13	SW1	27	SW7
14	N/C	28	SW7

Package Outlines



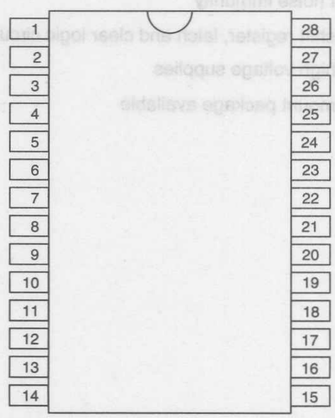
top view

24-pin DIP



top view

28-pin J-lead Package



top view

28-pin SOW

12

Supertex inc.

HV227
HV228

Low Charge Injection 8-Channel High Voltage Analog Switch

Ordering Information

Operating V_{PP}	$V_{PP} - V_{NN}$	Package Options 28-pin ceramic*† side-brazed DIP	Die in waffle pack	28-pin plastic DIP	28-lead plastic chip carrier	28-lead SOW
40V to 80V	140V	HV22714C	HV22714X	HV22714P	HV22714PJ	HV22714WG
	160V	HV22716C	HV22716X	HV22716P	HV22716PJ	HV22716WG
80V to 150V	140V	HV22814C	HV22814X	HV22814P	HV22814PJ	HV22814WG
	160V	HV22816C	HV22816X	HV22816P	HV22816PJ	HV22816WG

* Consult factory for Cerdip and Ceramic LCC availability.

† Consult factory for MIL-STD-883 processing.

Features

- ☐ HVCMOS® technology for high performance
- ☐ Low charge injection
- ☐ Very low quiescent power dissipation – 10µA
- ☐ Output On-resistance typically 22 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ 50dB typical output off isolation at 5 MHz
- ☐ CMOS logic circuitry for low power
- ☐ Excellent noise immunity
- ☐ On-chip shift register, latch and clear logic circuitry
- ☐ Flexible high voltage supplies
- ☐ Surface mount package available

General Description

This device is a low charge injection 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V†
V_{PP} positive high voltage supply	-0.5V to +160V†
V_{NN} Negative high voltage supply	+0.5V to -160V†
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	Plastic Package 0.8W
	Ceramic Package 2.0W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

† For HV22716 and HV22816

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD}= 15V unless otherwise noted)*

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Small Signal Switch (ON)	R_{ONS}		24		22	25		28	ohms	I_{SIG} = 5mA
Resistance	R_{ONS}		18		18	20		23	ohms	I_{SIG} = 200mA
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	I_{SW} = 5mA
Large Signal Switch (ON) Resistance	R_{ONL}				13	22			ohms	V_{SIG} = V_{PP} -10V, I_{SIG} = 1.0A
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	V_{SIG} = V_{PP} -10V and V_{NN} +10V
DC Offset Switch Off			300		100	300		300	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS ON
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	I_{SW} = 5mA
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V_{SIG} ≤ 0.1% Duty Cycle
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%
I_{PP} Supply Current	I_{PP}		4.0		3.5	5.0		5.5	mA	HV output switching frequency = 50KHz
I_{NN} Supply Current	I_{NN}		4.0		3.5	5.0		5.5	mA	
Logic Supply Average Current	I_{DD}		6.0		4.0	6.0		6.0	mA	f_{CLK} = 3MHz
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA	
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	V_{OUT} = V_{DD} - 0.7V
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Time to Turn Off V_{SIG}**	$t_{SIG\ (OFF)}$			0					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		175			175		190	ns	
Turn On Time	t_{ON}		3.0			3.0		3.0	µs	$R_L = 10K\Omega$
Turn Off Time	t_{OFF}		5.0			5.0		5.0	µs	$R_L = 10K\Omega$
Time Width of CL	t_{WCL}	150		150			150		ns	
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5MHz, 1KΩ// 15pF load
		-45		-45	-50		-45		dB	f = 5MHz, 50Ω load
Clock Freq	f_{CLK}		5.0			5.0		5.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_H	35		35			35		ns	
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5MHz, 50Ω load
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz
Output Voltage Spike	$+V_{SPK}$				150					$V_{PP} = +80V$,
	$-V_{SPK}$				150				mV	$V_{NN} = -80V$, $R_L = 50\Omega$

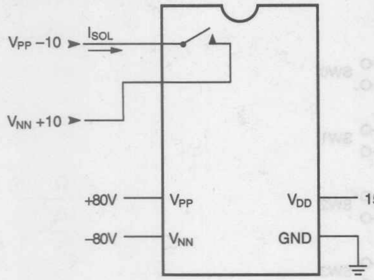
* For HV22716 and HV22816. For HV22714 and HV22814: $V_{PP} = 70V$, $V_{NN} = -70V$ and $V_{DD} = 15V$.
** Time required for analog signal to turn off before output switch turns off (critical timing).

Operating Conditions*

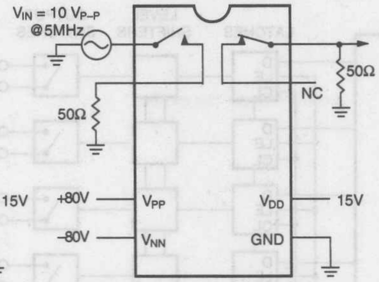
Symbol	Device				Value
	HV22714	HV22716	HV22814	HV22816	
V_{PP}	X				40V to 70V
		X			40V to 80V
			X		70V to 130V
				X	80V to 150V
V_{NN}	X		X		-10V to V_{PP} -140V
		X		X	-10V to V_{PP} -160V
V_{DD}	X	X	X	X	10V to 15.5V
V_{IH}	X	X	X	X	V_{DD} -2.0V to V_{DD}
V_{IL}	X	X	X	X	0V to 2.0V
V_{SIG}	X	X	X	X	V_{NN} +10V to V_{PP} -10
T_A	X	X	X	X	0°C to 70°C

Note: Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
* V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.
Rise and fall times of power supplies, V_{DD}, V_{PP}, and V_{NN} should not exceed 1.0msec.

Test Circuits

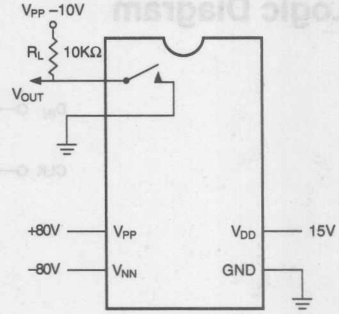


Switch OFF Leakage

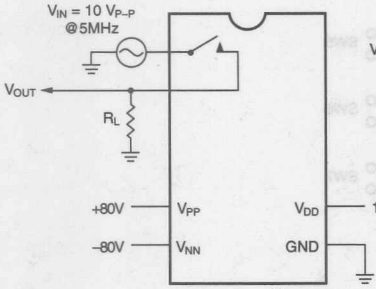


$K_{CR} = 20\text{Log}\ \frac{V_{OUT}}{V_{IN}}$

Crosstalk

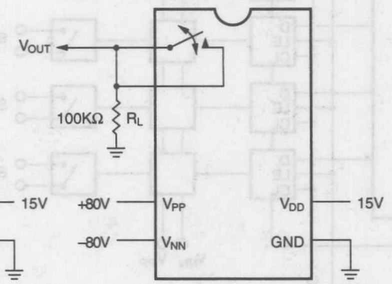


T_{ON}/T_{OFF}

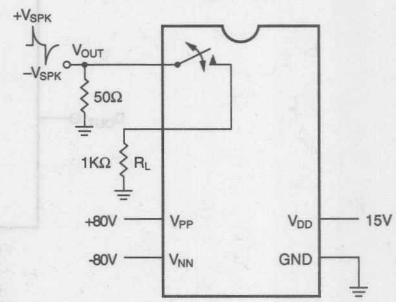


$K_O = 20\text{Log}\ \frac{V_{OUT}}{V_{IN}}$

OFF Isolation

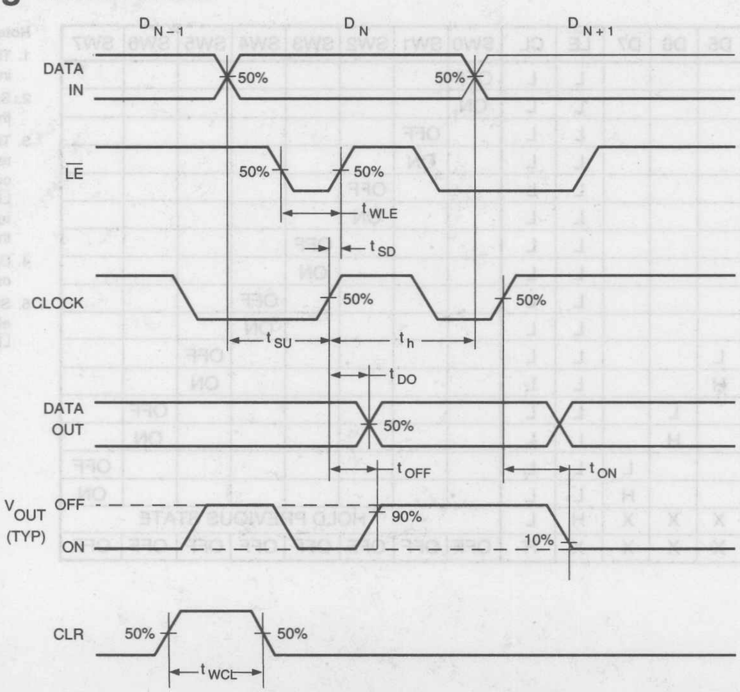


DC Offset ON/OFF

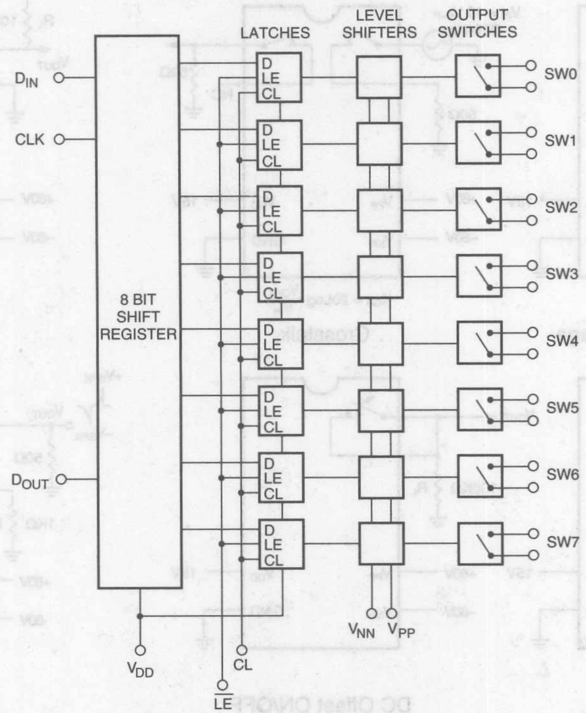


Output Voltage Spike

Logic Timing Waveforms



Logic Diagram



Truth Table

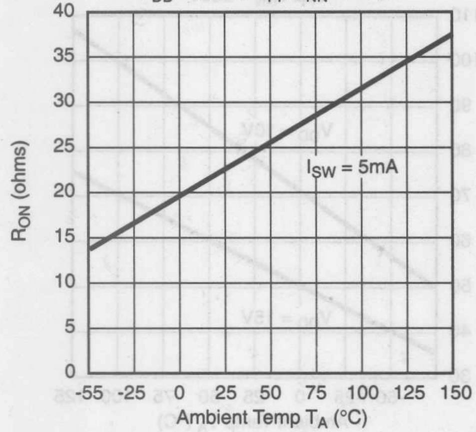
D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes:

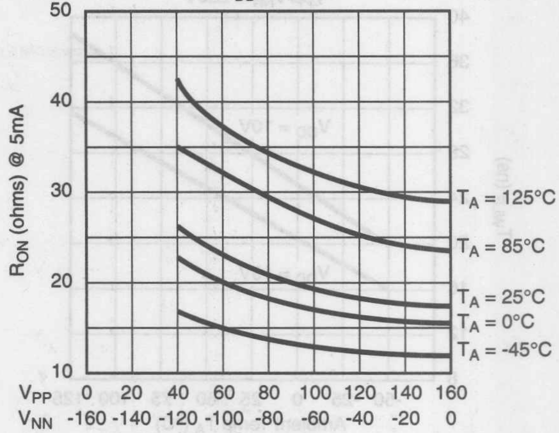
1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.

Typical Performance Curves

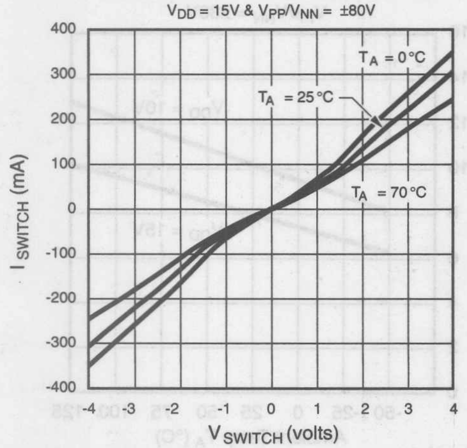
R_{ON} vs. Ambient Temp T_A
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



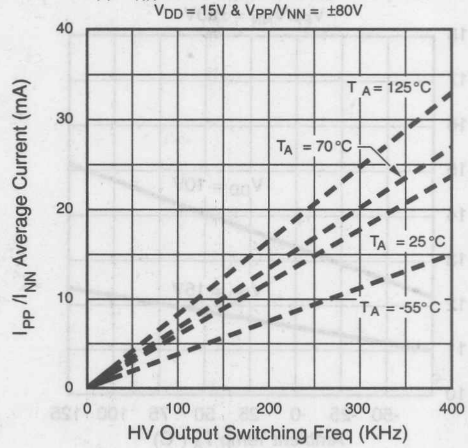
R_{ON} vs. V_{PP}/V_{NN}
V_{DD} = 15V



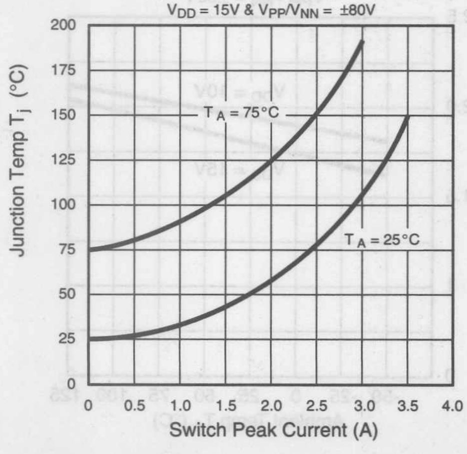
Switch Current vs Switch Voltage Drop
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



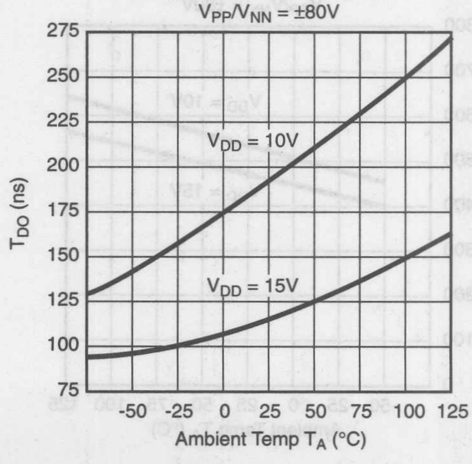
I_{PP}/I_{NN} vs Output Switching Frequency
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Junction Temp T_j vs Switch Peak Current
V_{SIG} Freq = 10KHz & Duty Cycle = 0.1%
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



T_{DO} vs. Ambient Temp T_A
V_{PP}/V_{NN} = ±80V



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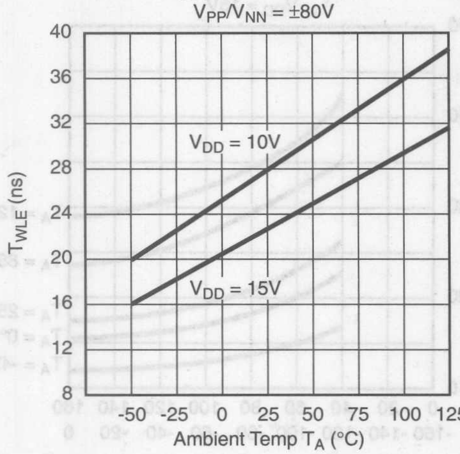
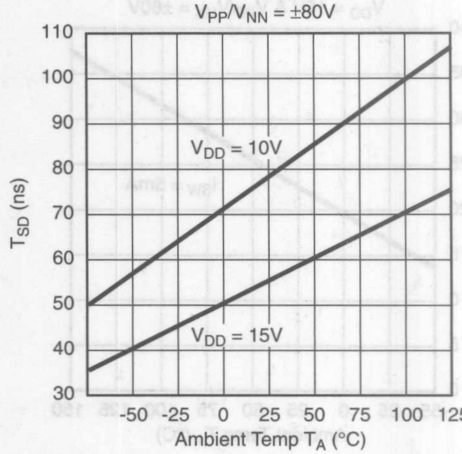
Typical Performance Curves

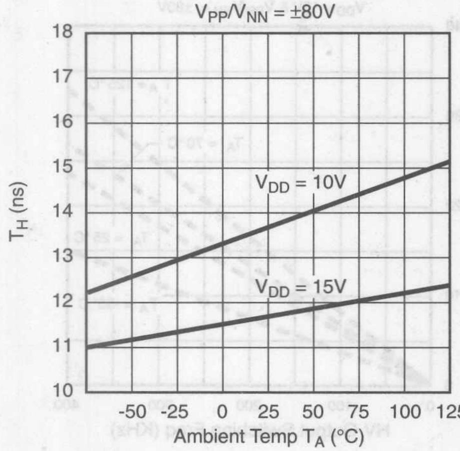
T_{WLE} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



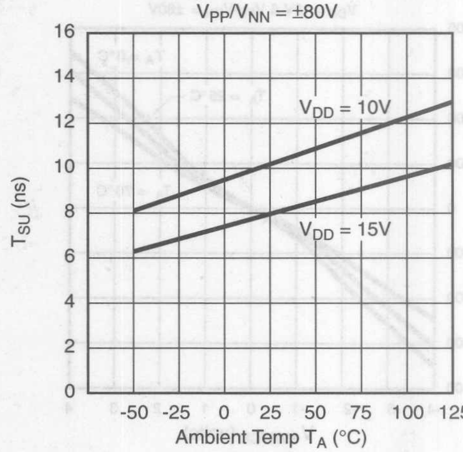
T_{SD} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



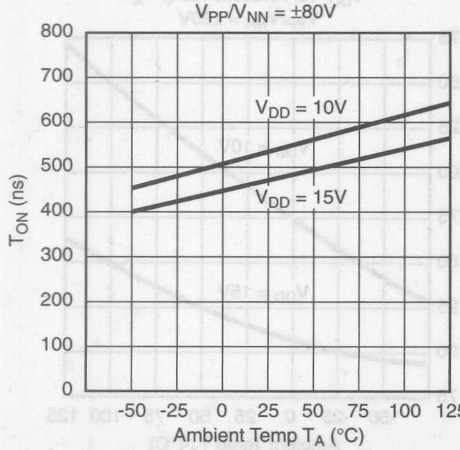
T_H vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



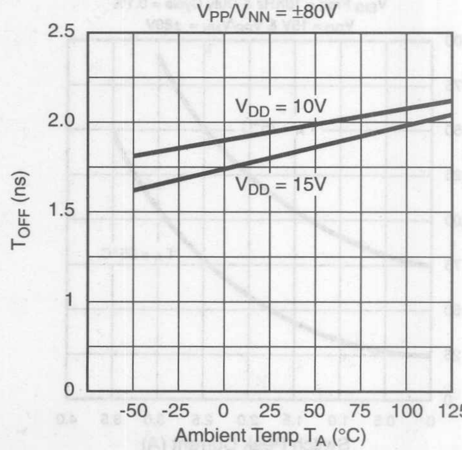
T_{SU} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



T_{ON} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



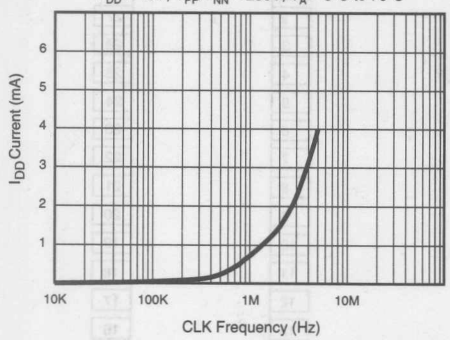
T_{OFF} vs. Ambient Temp
$V_{PP}/V_{NN} = \pm 80V$



Typical Performance Curves

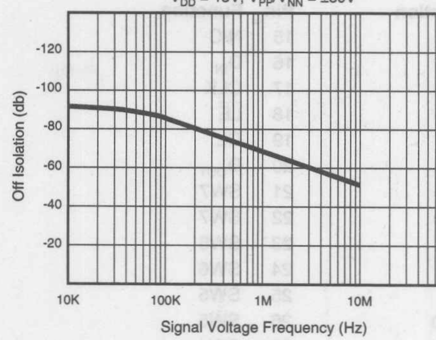
I_{DD} vs CLK Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V, T_A = 0°C to 70°C



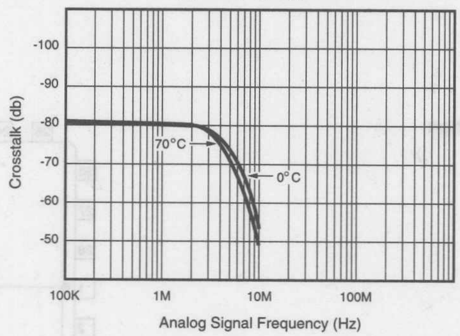
Off Isolation vs Signal Voltage Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



Crosstalk vs Analog Signal Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



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Pin Configurations

28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

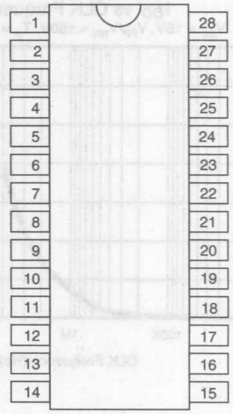
28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	SW1	19	CL
6	SW1	20	D_{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V_{PP}	23	SW6
10	V_{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V_{DD}	27	SW4
14	N/C	28	SW4

28-Lead SOW

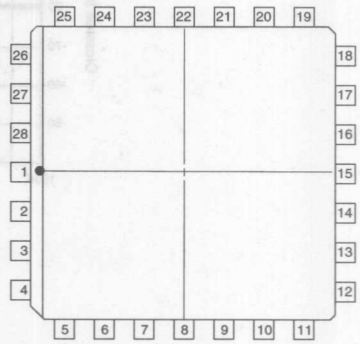
Pin	Function	Pin	Function
1	N/C	15	SW0
2	SW6	16	SW0
3	SW6	17	N/C
4	SW5	18	V_{PP}
5	SW5	19	V_{NN}
6	SW4	20	GND
7	SW4	21	V_{DD}
8	SW3	22	D_{IN}
9	SW3	23	CLK
10	SW2	24	$\overline{LE}$
11	SW2	25	CL
12	SW1	26	D_{OUT}
13	SW1	27	SW7
14	N/C	28	SW7

Package Outlines



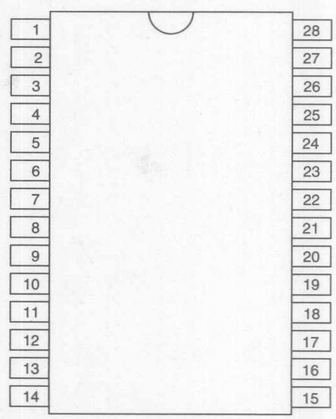
top view

28-pin DIP



top view

28-pin J-lead package



top view

28-pin SOW

Supertex inc.

HV341/HV343
HV345/HV348

High Voltage Analog Switches

Ordering Information

Function			Dual SPST	Dual SPDT	Dual DPST	Dual SPST
Analog Signal Range			V_{NN} to V_{PP}	V_{NN} to V_{PP}	V_{NN} to V_{PP}	V_{NN} to V_{PP}
$RDS_{(ON)}$			110 ohms	110 ohms	110 ohms	55 ohms
	Package Type	**Temp Range**				
Order No. and Part Type	16-lead ceramic, Hi-Rel†	-55°C to +125°C	RBHV341C	RBHV343C	RBHV345C	RBHV348C
	16-lead ceramic, Mil-Temp	-55°C to +125°C	HV341C	HV343C	HV345C	HV348C
	16-lead ceramic	-20°C to + 85°C	HV341MC	HV343MC	HV345MC	HV348MC
	16-lead small outline*	-20°C to + 85°C	HV341MWG	HV343MWG	HV345MWG	HV348MWG
	16-lead small outline*	0°C to + 70°C	HV341WG	HV343WG	HV345WG	HV348WG
	16-lead plastic DIP	0°C to + 70°C	HV341P	HV343P	HV345P	HV348P
	Die in waffle pack	0°C to + 70°C	HV341X	HV343X	HV345X	HV348X

* 300 mil wide SO package

† For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ☐ ±20V to ±50V single and dual supply operation
- ☐ R_{ON} less than 55Ω (HV348)
- ☐ Signal switching from positive to negative rail
- ☐ -50db OFF isolation at 5MHz
- ☐ Withstand +80V to -100 spikes
- ☐ Withstand V_{SIG} with power supply off

Applications

- ☐ Test equipment and instruments
- ☐ Diagnostic systems
- ☐ 48 volt telecom systems
- ☐ Military electronics

Absolute Maximum Ratings[1]

Supply voltage, V_{PP}		-0.3V to +65V
Supply voltage, V_{NN}		+0.3V to -65V
Data input voltage		V_{NN} to V_{PP}
Input current	Switches	±200mA
	Logic inputs	±30mA
Continuous total power dissipation[2]	Plastic Packages	500mW
	Ceramic Packages	750mW
Storage temperature range		-65°C to +150°C

Notes:
1. All voltages are referenced to V_{SS}.
2. For operation above 25°C ambient, derate linearly to 85°C at 8mW/°C.

General Description

These CMOS/DMOS high voltage analog switches are designed to handle high voltage analog signals. They may be used when analog voltages are low and high voltage immunity is desired. The signal handling capability extends from positive to negative supply voltage; i.e., 100V peak to peak with ±50V power supplies.

Inputs are compatible with CMOS logic, with a zero level turning the switches ON.

Operating supply voltage ranges from ±20V to ±50V with dual output power supplies, with the positive supply current below 300μA and negative supply not exceeding 100μA.

When a single output power supply is used, operating voltage ranges from +20V to +50V, with less than 20μA operating current when logic input signal equals the supply voltage.

With the addition of series diodes on the power supply and ground inputs, the HV341 series drivers will withstand +80V to -100V excursion on the inputs or switch pins without damage, or will withstand signal input with the power supplies OFF.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
V_{SIG}	Analog signal range		V_{NN}		V_{PP}	V	
R_{ON}	HV341/343/345	25°C		80	110	Ω	$V_{SIG} = \pm 50V$, $I_{SIG} = 10mA$
		Over temp			160		
	HV348	25°C		35	55	Ω	
		Over temp			80		
R_{ON}	ON-Resistance matching			7		%	
V_{IL}	Input low threshold				3.5	V	
V_{IH}	Input high threshold		12			V	
I_{SOL}	Switch OFF leakage	25°C		10	50	nA	$V_{SIG} = \pm 50V$
		Over temp		1	5	µA	
I_{PP}	V_{PP} quiescent current			200	600	µA	
I_{NN}	V_{NN} quiescent current			15	200	µA	
I_{IN}	Logic input current			0.1	10	µA	$V_{IN} = 0$ to $15V$
I_{SON}	Switch ON leakage	25°C		10	60	nA	$V_{SIG} \pm 50V$
		Over temp		1	5	µA	

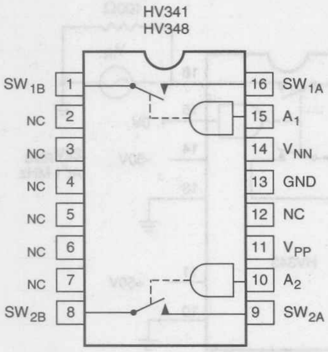
AC Characteristics (@ $V_{DD} = 12V$, $V_{PP} = 60V$, $T_C = 25°C$)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
t_{ON}	Turn-ON time	25°C		0.5	1.0	µs	
		Over temp			1.5		
t_{OFF}	Turn-OFF time	25°C		0.4	0.75	µs	
		Over temp			1.0		
K_O	OFF isolation			-70		dB	25°C, 1MHz
K_{CR}	Switch crosstalk			-75		dB	25°C, 1MHz
$C_{SW(OFF)}$	OFF capacitance across switch			1		pF	$T_A = 25°C$, $V_S = 0V$
$C_{SG(OFF)}$	OFF capacitance SW to GND			17		pF	
$C_{SG(ON)}$	ON capacitance SW to GND			38		pF	
Q	Charge injection				100	pC	$V_{SIG} = +50V$
					240	pC	$V_{SIG} = 0V$
					480	pC	$V_{SIG} = -50V$

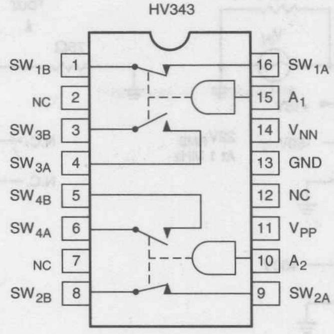
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{NN}	Negative high voltage supply		-50		0	V
V_{PP}	High voltage supply		+20		+50	V
V_{IH}	High-level input voltage		+12		+50	V
V_{IL}	Low-level input voltage		-50		+3.5	V
Operating temperature range		Commercial	0		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

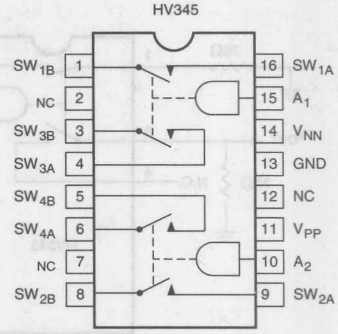
Functional Block Diagrams and Pin Configurations



Dual SPST

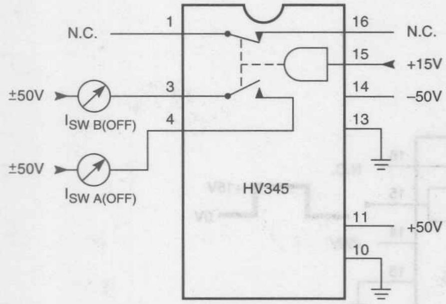


Dual SPDT

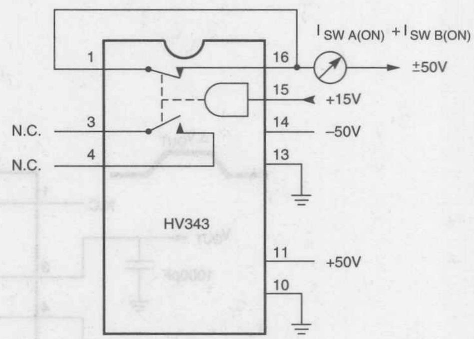


Dual DPST

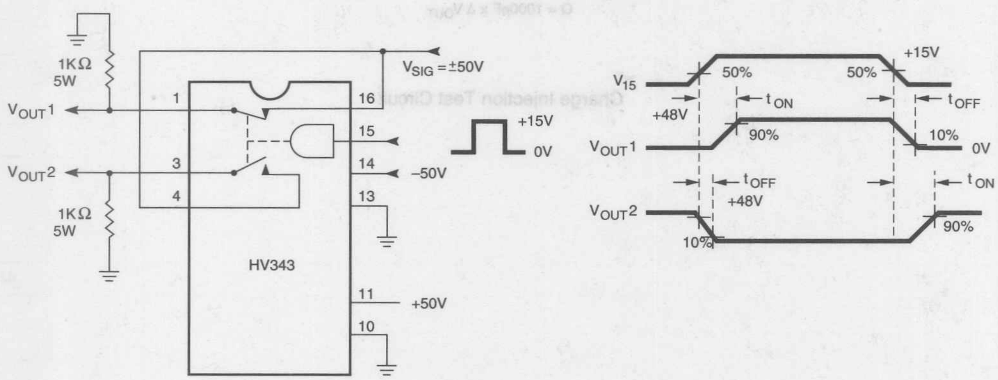
Test Circuits



OFF Leakage Test Circuit

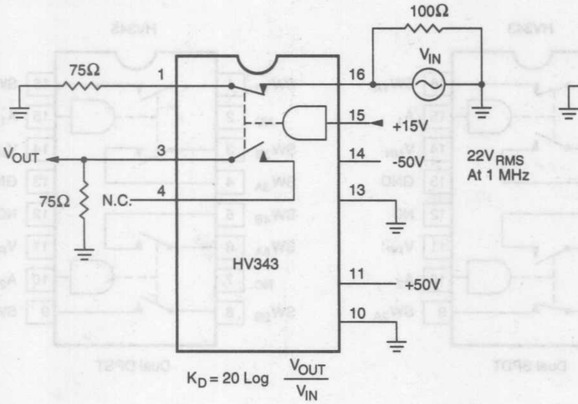


ON Leakage Test Circuit

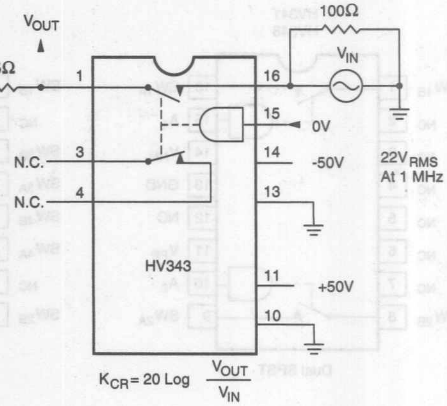


Switching Time Test Circuit

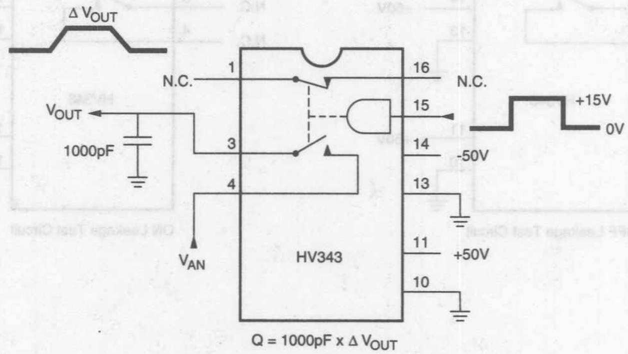
Test Circuits



Channel–Channel Crosstalk Circuit



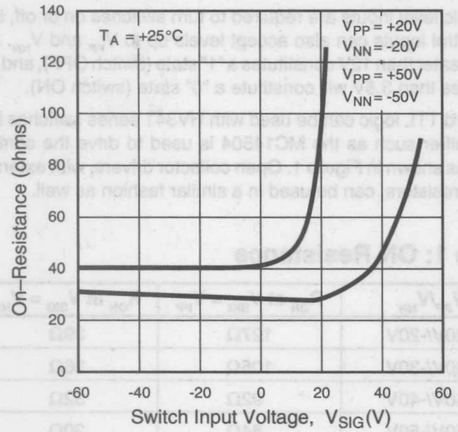
OFF Isolation Test Circuit



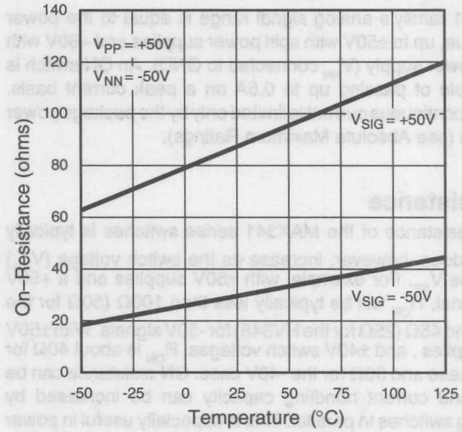
Charge Injection Test Circuit

Typical Operating Characteristics

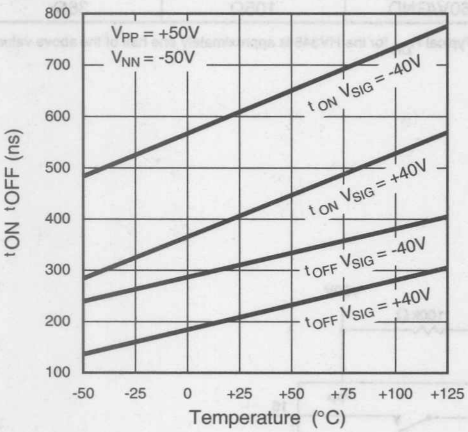
On–Resistance vs. Switch Input Voltage



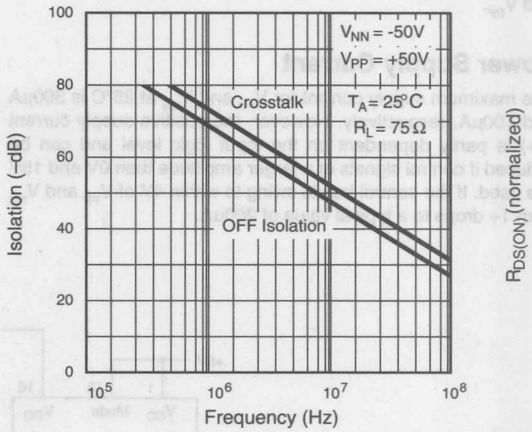
On–Resistance vs. Temperature



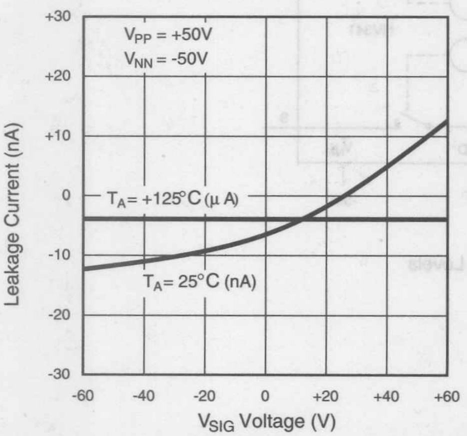
Switching Time vs. Temperature



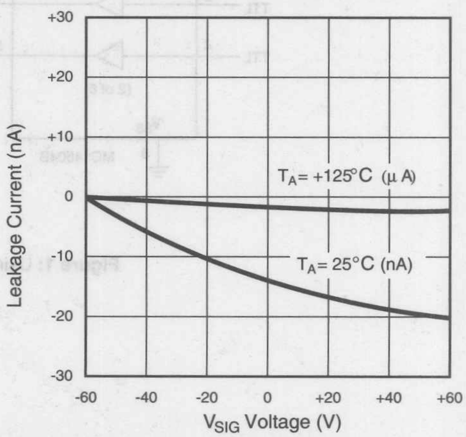
OFF Isolation And Crosstalk vs. Frequency



OFF Leakage vs. Switch Voltage



ON Leakage vs. Switch Voltage



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Applications Information

Analog Signal Range

The HV341 family's analog signal range is equal to the power supply value, up to ±50V with split power supplies and +60V with a single power supply (V_{NN} connected to GND). An ON switch is also capable of passing up to 0.5A on a peak current basis. Maximum continuous current is limited only by the package power dissipation (see Absolute Maximum Ratings).

ON Resistance

The ON resistance of the MAX341 series switches is typically 40Ω. R_{ON} does, however, increase as the switch voltage (V_{SIG}) approaches V_{PP}. For example, with ±50V supplies and a +50V analog signal, R_{ON} will be typically less than 100Ω (50Ω for the HV348), and 45Ω (25Ω for the HV348) for -50V signals. With ±50V power supplies , and ±40V switch voltages, R_{ON} is about 40Ω for the +40V case and 30Ω for the -40V case. ON resistance can be reduced and current handling capacity can be increased by connecting switches in parallel. This is especially useful in power switching applications. Table 1 and the graph in the Typical Characteristics section further describe the relation between R_{ON} and V_{PP}.

Power Supply Current

The maximum supply current for V_{PP} and V_{NN} at 25°C is 300µA and 100µA, respectively. However, the positive supply current (1+) is partly dependent on the input logic level and can be reduced if control signals of a larger amplitude than 0V and 15V are used. If the control inputs swing to within 4V of V_{PP} and V_{NN} then 1+ drops to a typical value of 200µA.

Control Inputs

15V logic level inputs are required to turn switches on or off, but the control inputs can also accept levels up to V_{PP} and V_{NN}. An input greater than 12V constitutes a "1" state (switch OFF), and an input less than 3.5V will constitute a "0" state (switch ON).

Standard TTL logic can be used with HV341 series switches if a level shifter such as the MC14504 is used to drive the control inputs as shown in Figure 1. Open collector drivers, with external pull-up resistors, can be used in a similar fashion as well.

Table 1: ON Resistance

V_{PP}/V_{NN}	R_{ON} at $V_{SIG} = V_{PP}$	R_{ON} at $V_{SIG} = V_{NN}$
+20V/-20V	127Ω	39Ω
+30V/-30V	105Ω	36Ω
+40V/-40V	92Ω	32Ω
+50V/-50V	84Ω	30Ω
+40V/GND	127Ω	39Ω
+60V/GND	105Ω	36Ω

Note: Typical R_{ON} for the HV348 is approximately one half of the above values.

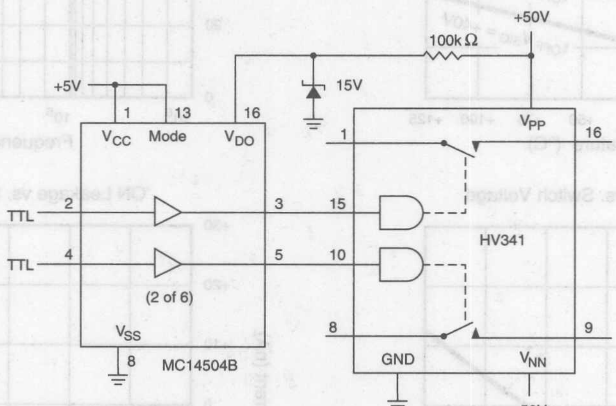

Figure 1: Using TTL Control Levels

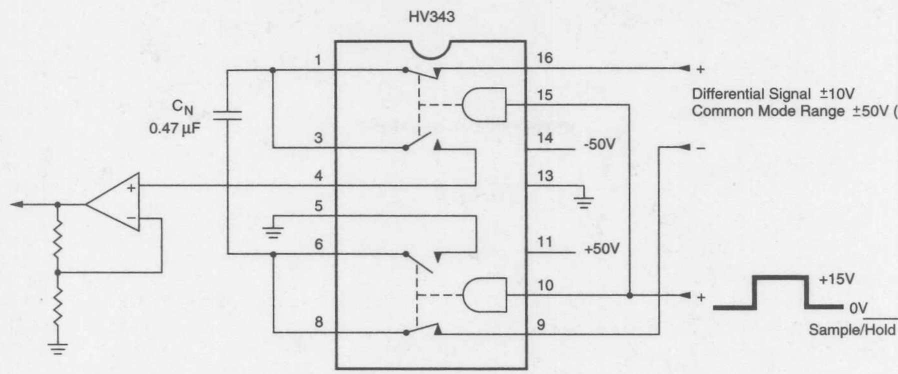

Figure 2: Flying Capacitor Differential to Single-Ended Converter With ±50V Common-Mode Range.

Flying Capacitor Input

A "flying capacitor" differential to single-ended converter takes advantage of the HV343's wide input voltage range, which allows large common mode inputs to be rejected. As shown in figure 2, a capacitor is alternately charged by the differential input signal and then is connected to an op-amp or A-to-D input. An instrumentation amplifier is not required since the output signal can be referenced to ground. Sample-hold operation is also built into the design and the HV343's break-before-make operation ensures that the output sees only the differential portion of the input signal. A similar approach can also be used for single-ended to differential signal conversion as well.

Parallel Switches

In designs where power switching ability is needed, any of the HV 341 series switches can be connected in parallel to increase current handling capability and reduce ON resistance. Applications such as ultrasonics, RF power, and DC motor drive are areas where this is often important. An HV348 is shown in a parallel configuration in Figure 3. The resulting SPST switch has a typical R_{ON} of 12Ω (5Ω for signals more than 10V below V_{PP}) and can handle pulsed loads of up to 0.5 Amps. With ±50V power supplies, the peak-to-peak signal range is still 100V, and 10MHz signals can be switched while maintaining typically -50dB of isolation.

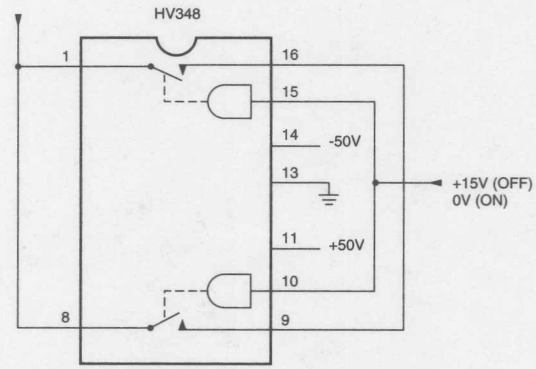

Figure 3: Minimum R_{ON} (5 to 10Ω typ.) High Voltage Switch.

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Chapter 13 – High Voltage Power Supply ICs

Supertex inc.

HV9100
HV9101
HV9102
HV9103

Preliminary

High-Voltage Switchmode Controllers with MOSFET

Ordering Information

$+V_{IN}$		Feedback Voltage	Max Duty Cycle	MOSFET Switch		Package Options		
Min	Max			BV_{DSS}	$R_{DS(ON)}$	14 Pin Plastic DIP	14 Pin Ceramic DIP	20 Pin Plastic PLCC
10V	70V	± 1%	49%	150V	5.0Ω	HV9100P	HV9100C	HV9100PJ
10V	70V	±10%	49%	150V	5.0Ω	HV9101P	—	HV9101PJ
10V	120V	± 1%	49%	200V	7.0Ω	HV9102P	HV9102C	HV9102PJ
10V	120V	±1%	99%	200V	7.0Ω	HV9103P	HV9103C	HV9103PJ

Features

- 10 to 120V input range
- 200V, 7Ω output MOSFET
- Current-Mode Control
- High Efficiency
- Up to 1MHz Internal Oscillator
- Internal Start-up Circuit

Applications

- DC/DC Converters
- Distributed Power Systems
- ISDN Equipment
- PBX Systems
- Modems

Absolute Maximum Ratings

$+V_{IN}$, Input Voltage	120V
V_{DS}	200V
V_{DD}, Logic Voltage	15.0V
Input Voltage Logic, Linear, FB and Sense	-0.3V to V_{DD}+0.3V
I_D (Peak)	2.5A
Storage Temperature	-65°C to 150°C
Power Dissipation, Plastic DIP	750mW
Power Dissipation, Ceramic DIP	1000mW
Power Dissipation, PLCC	1400mW

General Description

The Supertex HV9100 through HV9103 are a series of BiCMOS/DMOS single-output, pulse width modulator ICs intended for use in high-speed high-efficiency switchmode power supplies. They provide all the functions necessary to implement a single-switch current-mode PWM, in any topology, with a minimum of external parts.

Utilization of Supertex proprietary BiCMOS/DMOS technology results in a device with one tenth of the operating power of conventional bipolar PWM ICs, which can operate at more than twice their switching frequency. Dynamic range for regulation is also increased, to approximately 8 times that of similar bipolar parts. They start directly from any DC input voltage between 10 and 70VDC for the HV9100 and HV9101, or 10 to 120VDC for the HV9102 and HV9103, requiring no external power resistor. The output stage for the HV9100 and the HV9101 is a 150V, 5.0 ohm MOSFET and for the HV9102 and HV9103 is a 200V, 7.0 ohm MOSFET. The clock frequency is set with a single external resistor.

Accessory functions are included to permit fast remote shutdown (latching or nonlatching), and undervoltage shutdown.

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V_{REF}	Output Voltage	HV9100/02/03	3.92	4.00	4.08	V	$R_L = 10M\Omega$
		HV9101	3.60	4.00	4.40		
		HV9102/03	3.86	4.00	4.14	V	$IN = V_{IN}$, $R_L = 10M\Omega$ $T_A = -55°C$ to $125°C$
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			100	130	µA	$V_{REF} = -V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature			0.25		mV/°C	

Oscillator

f_{MAX}	Oscillator Frequency	1	3		MHz	$R_{OSC} = 0\Omega$
f_{OSC}	Initial Accuracy[2]	80	100	120	KHz	$R_{OSC} = 330K\Omega$
		160	200	240		$R_{OSC} = 150K\Omega$
	Voltage Stability			15	%	$9.5V < V_{DD} < 13.5V$
	Temperature Coefficient		170		ppm/°C	

PWM

D_{MAX}	Maximum Duty Cycle	HV9100/01/02	49.0	49.4	49.6	%	
		HV9103	99.0	99.4	99.6		
	Deadtime	HV9103		100		nsec	
D_{MIN}	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			110	175	nsec	

Error Amplifier

V_{FB}	Feedback Voltage	HV9100/02/03	3.96	4.00	4.04	V	V_{FB} Shorted to Comp
		HV9101	3.60	4.00	4.40		
I_{IN}	Input Bias Current			25	500	nA	$V_{FB} = 4.0V$
V_{OS}	Input Offset Voltage			nulled at trim		mV	Except 9101
A_{VOL}	Open Loop Voltage Gain[1]		60	80		dB	
gbw	Unity Gain Bandwidth[1]		1.0	1.3		MHz	
Z_{OUT}	Output Impedance[1]			See Fig. 2		Ω	
I_{SOURCE}	Output Source Current			-2.0	-1.4	mA	$V_{FB} = 3.4V$
I_{SINK}	Output Sink Current		0.12	0.15		mA	$V_{FB} = 4.5V$
PSRR	Power Supply Rejection			See Fig. 1			

Current Limit

V_{SOURCE}	Threshold Voltage	1.0	1.2	1.4	V	$V_{FB} = 0V$, $R_L = 100\Omega$
t_d	Delay to Output[1]			150	ns	$V_{SOURCE} = 1.5V$, $R_L = 100\Omega$

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin ≤5pF.

Electrical Characteristics (Continued)

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C, unless otherwise specified)

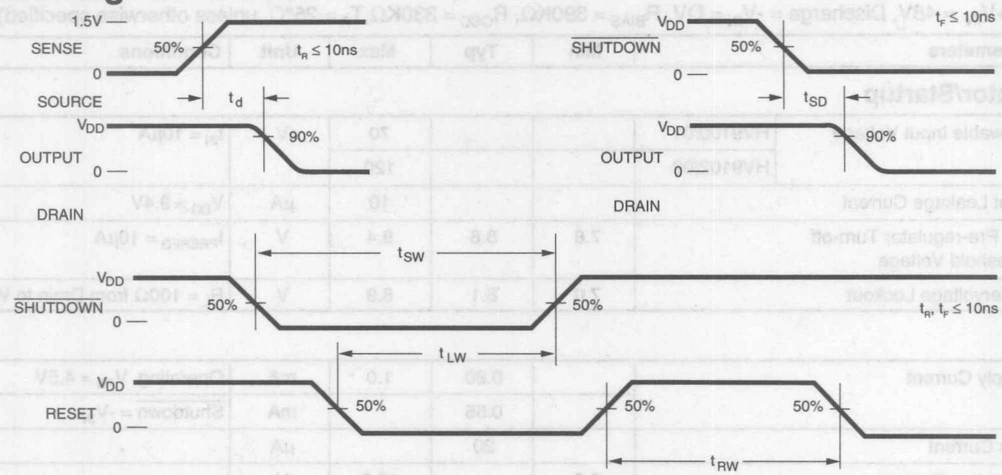
Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Pre-Regulator/Startup							
$+V_{IN}$	Allowable Input Voltage	HV9100/01			70	V	I_{IN} = 10µA
		HV9102/03			120		
	Input Leakage Current				10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		7.8	8.6	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	R_L = 100Ω from Drain to V_{DD}
Supply							
I_{DD}	Supply Current			0.60	1.0	mA	Operating, V_{FB} = 4.5V
				0.55		mA	$\overline{\text{Shutdown}}$ = $-V_{IN}$
I_{BIAS}	Bias Current			20		µA	
V_{DD}	Operating Range		9.0		13.5	V	
Logic							
t_{SD}	$\overline{\text{Shutdown}}$ Delay Time[1]			50	100	ns	V_{SOURCE} = $-V_{IN}$
t_{SW}	$\overline{\text{Shutdown}}$ Pulse Width[1]		50			ns	
t_{RW}	RESET Pulse Width[1]		50			ns	
t_{LW}	Latching Pulse Width[1]		25			ns	
V_{IL}	Input Low Voltage				2.0	V	
V_{IH}	Input High Voltage		7.0			V	
I_{IH}	Input High Current			1	5	µA	V_{IN} = 10V
I_{IL}	Input Low Current			-25	-35	µA	V_{IN} = 0V
MOSFET Switch							
BV_{DSS}	Breakdown Voltage	HV9100/01	150			V	V_{SOURCE} = $\overline{\text{Shutdown}}$ = OV,
		HV9102/03	200				I_D = 100µA, T_A = -55°C to 125°C
$R_{DS(ON)}$	Drain-to-Source	HV9100/01		3.5	5.0	Ω	V_{SOURCE} = OV, I_D = 100mA
	On-resistance	HV9102/03			7.0	Ω	
I_{DSS}	OFF State Drain Leakage Current				10	µA	V_{SOURCE} = $\overline{\text{Shutdown}}$ = OV, V_{DRAIN} = 100V
C_{DS}	Drain Capacitance			35		pF	V_{DS} = 25V, $\overline{\text{Shutdown}}$ = OV

Note:
1. Guaranteed by design. Not subject to production test.

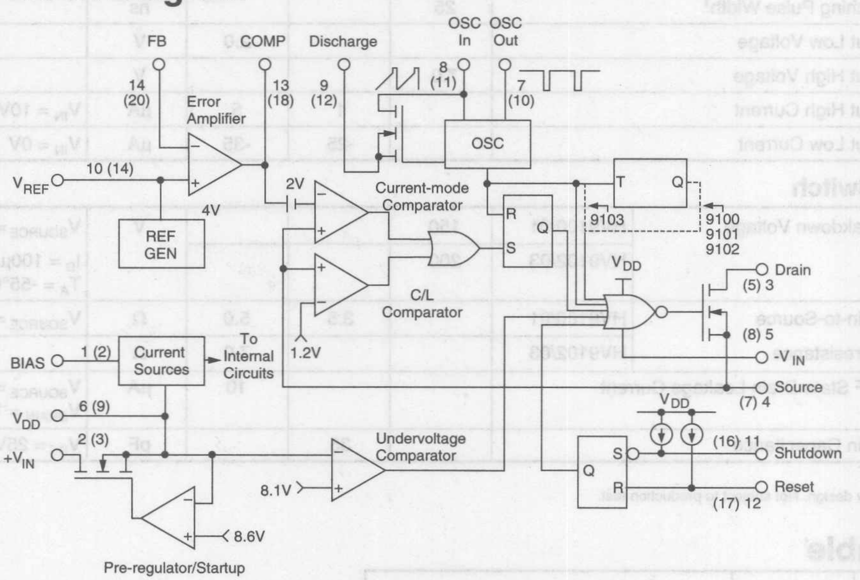
Truth Table

$\overline{\text{Shutdown}}$	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Switching Waveforms



Functional Block Diagram



Typical Performance Curves

Fig. 1 PSRR – Error Amplifier and Reference

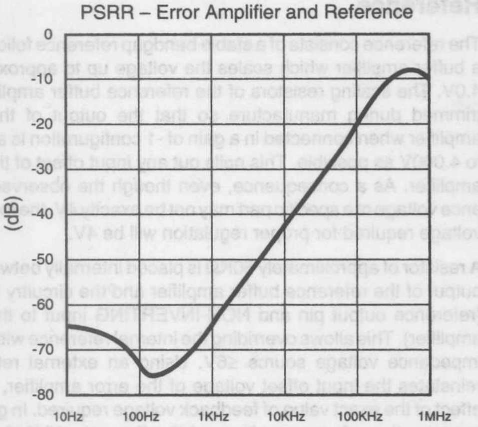


Fig. 3 Error Amplifier Open Loop Gain/Phase

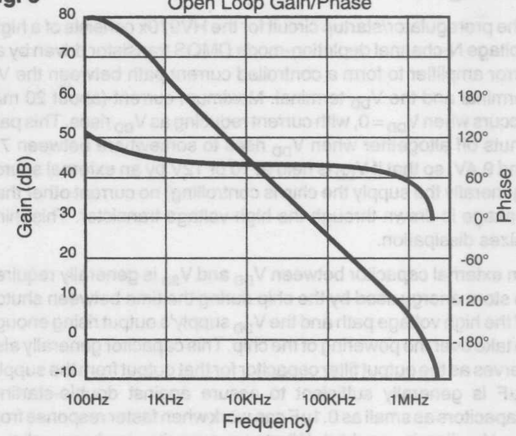


Fig. 2 Error Amplifier Output Impedance (Z_0)

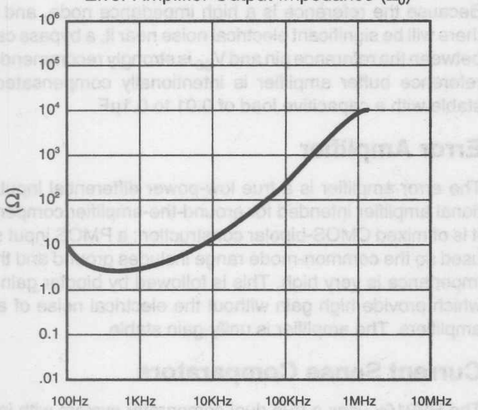
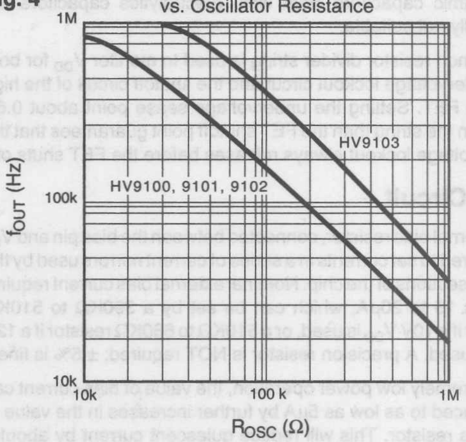
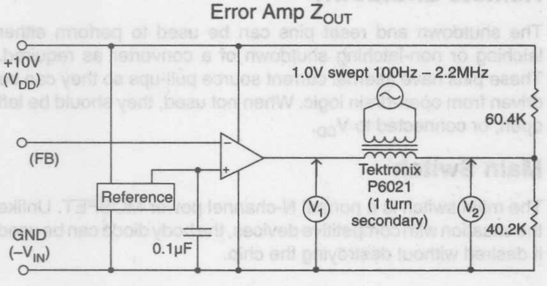


Fig. 4 Output Switching Frequency vs. Oscillator Resistance

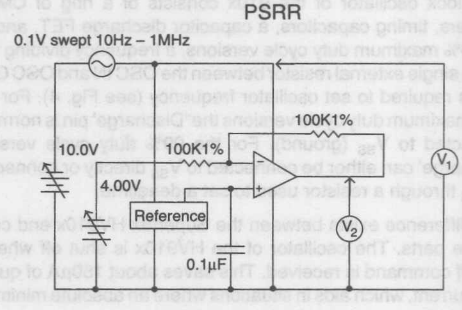


Test Circuits

Error Amp Z_{OUT}



PSRR



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

13

Technical Description

Preregulator

The preregulator/startup circuit for the HV910x consists of a high-voltage N-channel depletion-mode DMOS transistor driven by an error amplifier to form a controlled current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip during the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over the powering of the chip. This capacitor generally also serves as the output filter capacitor for that output from the supply. 1µF is generally sufficient to assure against double-starting. Capacitors as small as 0.1µF can work when faster response from the V_{DD} line is required. Whatever capacitor is chosen should have very good high frequency characteristics. Stacked polyester or ceramic capacitors work well. Electrolytics capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circut and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510KΩ to 680KΩ resistor if a 12V V_{DD} is used. A precision resistor is NOT required; ± 5% is fine.

For extremely low power operation, the value of bias current can be reduced to as low as 5µA by further increases in the value of the bias resistor. This will reduce quiescent current by about a third, reduce bandwidth of the error amp by about half, and slow the current sense comparator by about 30%.

Clock Oscillator

The clock oscillator of the 910x consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC IN and OSC OUT pins is required to set oscillator frequency (see Fig. 4). For the 50% maximum duty cycle versions the 'Discharge' pin is normally connected to V_{SS} (ground). For the 99% duty cycle version, 'Discharge' can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV910x and competitive parts. The oscillator of the HV910x is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in situations where an absolute minimum of quiescent power dissipation is required.

Reference

The reference consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of -1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be 4V.

A resistor of approximately 50KΩ is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and NON-INVERTING input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV910x is not noisy, as some previous devices have been, overriding the reference should seldom be necessary.

Because the reference is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Error Amplifier

The error amplifier is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: a PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV910x uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

Remote Shutdown

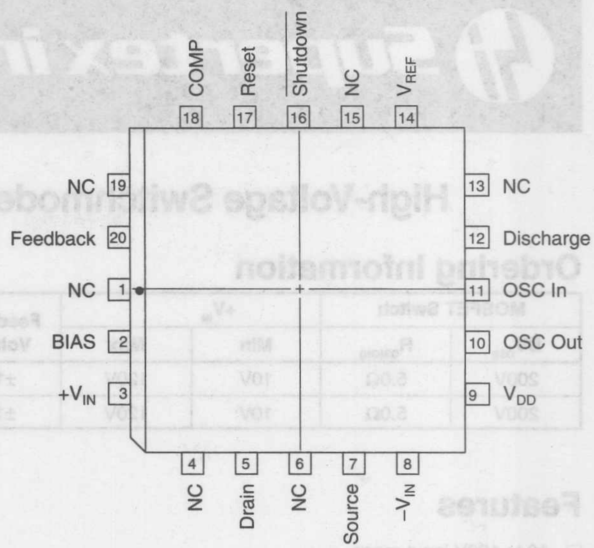
The shutdown and reset pins can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used, they should be left open, or connected to V_{DD}.

Main Switch

The main switch is a normal N-channel power MOSFET. Unlike the situation with competitive devices, the body diode can be used if desired without destroying the chip.

Pinout

14 Pin DIP Package



20-pin PJ Package
top view

Supertex inc.

HV9105
HV9108

Preliminary

High-Voltage Switchmode Controllers with MOSFET

Ordering Information

MOSFET Switch		$+V_{IN}$		Feedback Voltage	Max Duty Cycle	Package Outlines	
BV_{DSS}	$R_{DS(ON)}$	Min	Max			14 Pin Plastic DIP	20 Pin Plastic PLCC
200V	5.0Ω	10V	120V	±1%	49%	HV9105P	HV9105PJ
200V	5.0Ω	10V	120V	±1%	99%	HV9108P	HV9108PJ

Features

- 10 to 120V input range
- 200V, 5Ω output MOSFET
- Current-Mode Control
- High Efficiency
- CCITT Compatible
- Internal Start-up Circuit

Applications

- DC/DC Converters
- Distributed Power Systems
- ISDN Equipment
- PBX Systems
- Modems

Absolute Maximum Ratings

$+V_{IN}$, Input Voltage	120V
V_{DS}	200V
V_{DD}, Logic Voltage	15.0V
Control Inputs	-0.3V to V_{DD}+0.3V
I_D (Peak)	2.5A
Storage Temperature	-65°C to 150°C
Power Dissipation, Plastic DIP	750mW
Power Dissipation, PLCC	1400mW

General Description

The Supertex HV9105 and HV9108 are high-efficiency high voltage SMPS ICs intended for use in power converters requiring extreme efficiency at output power levels of 5W or less. The low supply current (0.5mA max) allows them to be used to build supplies which meet CCITT I.430 performance recommendations (60% efficiency at .025W out).

The HV9105/08 provides all the functions necessary to build a single-switch current-mode converter of any common topology, with a minimum of external parts.

In addition to high efficiency, because it uses Supertex's proprietary high voltage BiCMOS/DMOS technology, the HV9105/08 offers numerous performance advantages when compared to conventional PWM ICs. Dynamic range is approximately 8 times wider than with bipolar ICs, both response speed and maximum clock rate are faster, and no external power resistors or zeners are necessary for high voltage starting.

Accessory circuits are included to provide either latching or nonlatching shutdown. When shut down, device dissipation is less than 4mW.

The HV9105/08 is intended for operation with input voltages from 10 to 120VDC.

Electrical Characteristics

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 820KΩ, R_{OSC} = 910KΩ, T_A = 25°C, unless otherwise specified)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions

Reference

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
V_{REF}	Output Voltage		3.92	4.00	4.08	V	R_L = 10MΩ
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			100	130	µA	V_{REF} = $-V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature			0.25		mV/°C	

Oscillator

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
f_{MAX}	Maximum Oscillator Frequency		1	3		MHz	R_{OSC} = 0Ω
f_{OSC}	Initial Accuracy[2]		32	40	48	KHz	
	Voltage Stability				15	%	9.5V < V_{DD} < 13.5V
	Temperature Coefficient			170		ppm/°C	

PWM

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
D_{MAX}	Maximum Duty Cycle	HV9105	49.0	49.4	49.6	%	
		HV9108	99.0	99.4	99.6		
	Deadtime	HV9108		100		nsec	
D_{MIN}	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			110	175	nsec	

Error Amplifier

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
V_{FB}	Feedback Voltage		3.96	4.00	4.04	V	V_{FB} Shorted to Comp
I_{IN}	Input Bias Current			25	500	nA	V_{FB} = 4.0V
V_{OS}	Input Offset Voltage			nulled at trim		mV	
A_{VOL}	Open Loop Voltage Gain		60	80		dB	
gbw	Unity Gain Bandwidth		0.5	0.8		MHz	
Z_{OUT}	Output Impedance			See Fig. 2		Ω	
I_{SOURCE}	Output Source Current			-2.0	-1.4	mA	V_{FB} = 3.4V
I_{SINK}	Output Sink Current		80	120		µA	V_{FB} = 4.5V
PSRR	Power Supply Rejection			See Fig. 1			

Current Limit

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
V_{SOURCE}	Threshold Voltage		1.0	1.2	1.4	V	V_{FB} = 0V, R_L = 100Ω
t_d	Delay to Output[1]			150	200	ns	V_{SOURCE} = 1.5V, R_L = 100Ω

Pre-Regulator/Startup

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
$+V_{IN}$	Allowable Input Voltage				120	V	I_{IN} = 10µA
	Input Leakage Current				10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		7.8	8.6	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	R_L = 100Ω from Drain to V_{DD}

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin ≤5pF.

Electrical Characteristics (Continued)

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 820KΩ, R_{OSC} = 910KΩ, T_A = 25°C, unless otherwise specified)

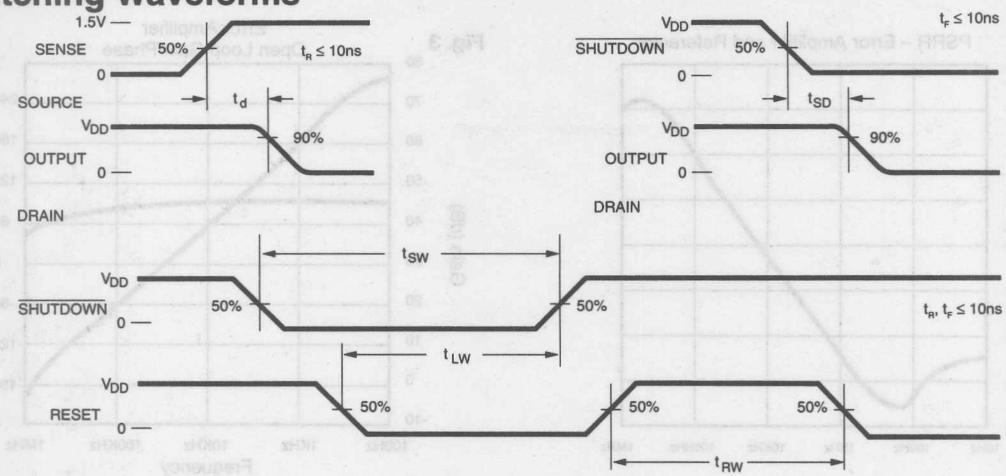
Symbol	Parameters	Min	Typ	Max	Unit	Conditions
Supply						
I_{DD}	Supply Current			0.5	mA	V_{FB} = 4.5 Volts Operating
			0.35		mA	$\overline{\text{Shutdown}} = -V_{IN}$
I_{BIAS}	Bias Current		7.5		µA	
V_{DD}	Operating Range	9.0		13.5	V	
Logic						
t_{SD}	Shutdown Delay Time[1]		50	100	ns	$V_{SOURCE} = -V_{IN}$
t_{SW}	Shutdown Pulse Width[1]	50			ns	
t_{RW}	RESET Pulse Width[1]	50			ns	
t_{LW}	Latching Pulse Width[1]	25			ns	
V_{IL}	Input Low Voltage			2.0	V	
V_{IH}	Input High Voltage	7.0			V	
I_{IH}	Input High Current		1	5	µA	V_{IN} = 10V
I_{IL}	Input Low Current		-25	-35	µA	V_{IN} = 0V
MOSFET Switch						
BV_{DSS}	Breakdown Voltage	200	240		V	$V_{SOURCE} = \overline{\text{Shutdown}}$ = OV, I_D = 100µA
$R_{DS(ON)}$	Drain-to-Source On-resistance		3.5	5.0	Ω	V_{SOURCE} = OV, I_D = 100mA
I_{DSS}	OFF State Drain Leakage Current			10	µA	$V_{SOURCE} = \overline{\text{Shutdown}}$ = OV, V_{DRAIN} = 100V
C_{DS}	Drain Capacitance		35		pF	V_{DS} = 25V, $\overline{\text{Shutdown}}$ = OV

Note:
1. Guaranteed by design. Not subject to production test.

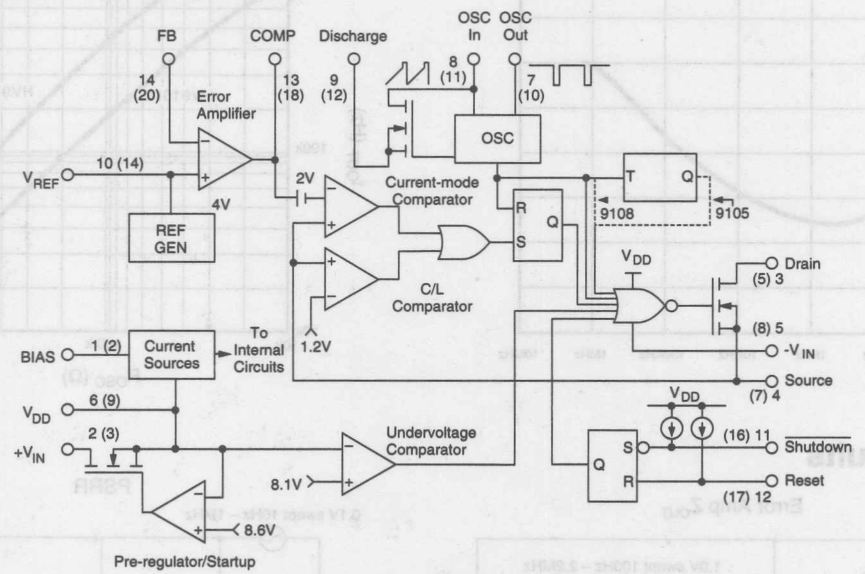
Truth Table

$\overline{\text{Shutdown}}$	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Switching Waveforms



Functional Block Diagram



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Typical Performance Curves

Fig. 1

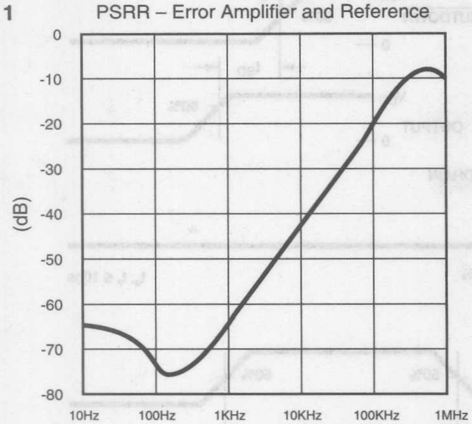


Fig. 3

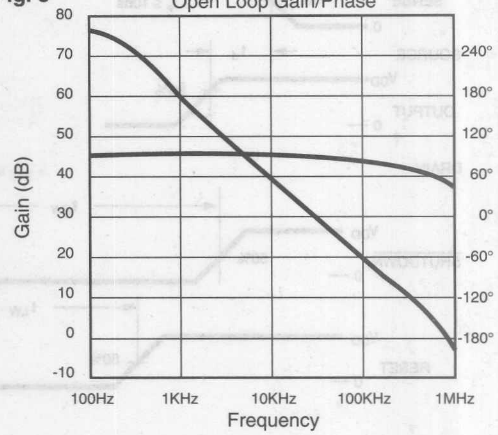


Fig. 2

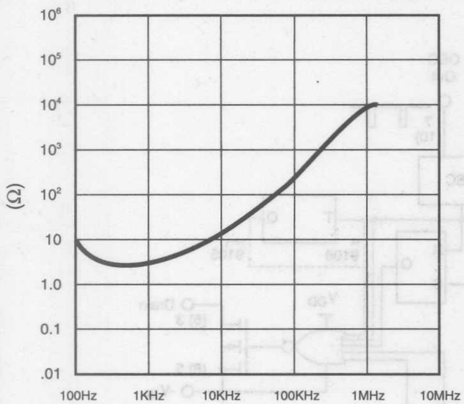
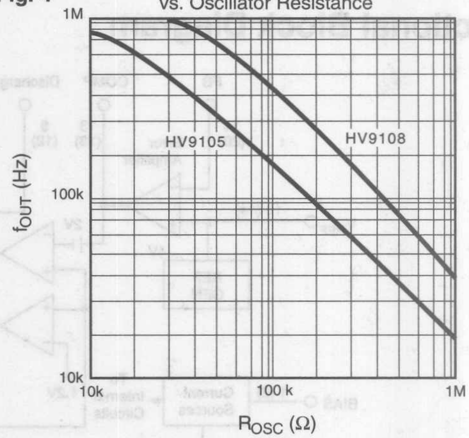
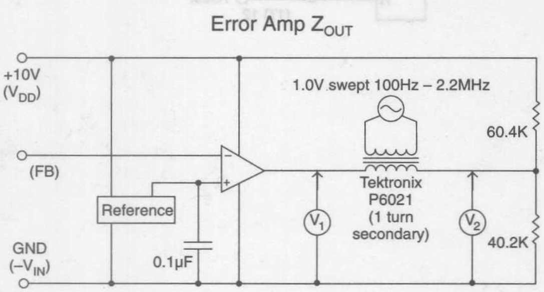
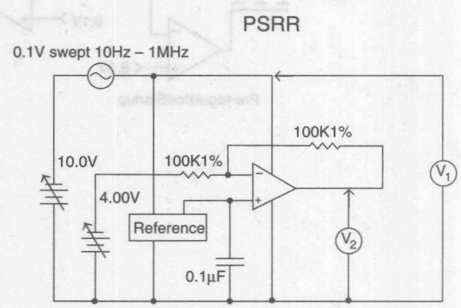


Fig. 4



Test Circuits





NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

Technical Description

Preregulator

The preregulator/startup circuit for the HV9105/08 consists of a high-voltage N-channel depletion-mode DMOS transistor driven by an error amplifier to form a controlled current path between the V_{IN} terminal and the V_{DD} terminal of the 9105/08. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip during the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over the powering of the chip. This capacitor generally also serves as the output filter capacitor for that output from the supply. 1µF is generally sufficient to assure against double-starting. Capacitors as small as 0.1µF can work when faster response from the V_{DD} line is required. The chosen capacitor should have very good high frequency characteristics and be mounted so that the sum of the lead length between capacitor and IC for both leads is less than 2.5 cm. Stacked polyester or ceramic capacitors work well. Electrolytic capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required by the HV9105/08 to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 7.5µA, which can be set by a 820KΩ to 1.3MΩ resistor if a 10V V_{DD} is used, or a 1.2MΩ to 2.0MΩ resistor if a 12V V_{DD} is used. A precision resistor is NOT required; ± 5% is fine.

For extremely low power operation, the value of bias current can be reduced to as low as 4µA by further increases in the value of the bias resistor.

Clock Oscillator

The clock oscillator of the 9105/08 consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle version, a frequency dividing flip-flop. A single external resistor between the OSC IN and OSC OUT pins is required to set oscillator frequency (see Fig. 4). For the 50% maximum duty cycle versions the 'Discharge' pin is normally connected to V_{SS} (ground). For the 99% duty cycle version, 'Discharge' can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV9105/08 and competitive 9105 parts. The oscillator of the Supertex HV9105/08 is shut off when a shutoff command is received. This saves about 100µA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I.430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The reference section of the HV9105/08 consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of -1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be 4V.

A resistor of approximately 50KΩ is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV9105/08 is not noisy, as some previous devices have been, overriding the reference should seldom be necessary.

Because the reference is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Error Amplifier

The error amplifier is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: a PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV9105/08 uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

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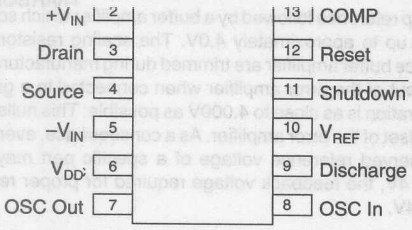
Remote Shutdown

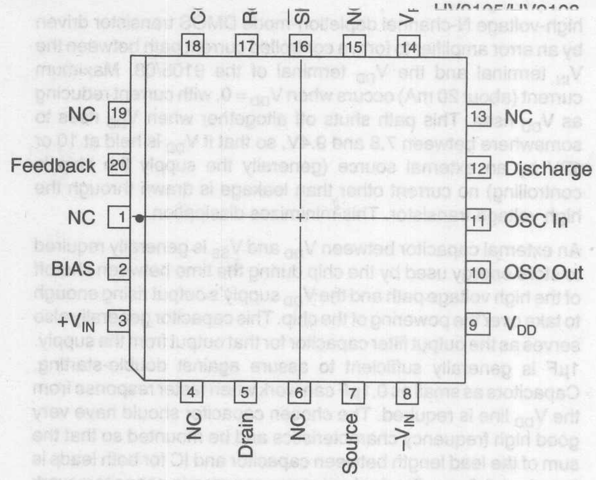
The shutdown and reset pins can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used, they should be left open, or connected to V_{DD}.

Main Switch

The main switch is a normal N-channel power MOSFET. Unlike the situation with competitive devices, the body diode can be used if desired without destroying the chip.



14 Pin DIP Package



20-pin PJ Package
top view

Supertex inc.

HV9106
HV9109

Objective

High-Voltage Switchmode Controllers with MOSFET

Ordering Information

MOSFET Switch		$+V_{IN}$		Feedback Voltage	Max Duty Cycle	Package Outlines	
BV_{DSS}	$R_{DS(ON)}$	Min	Max			16 Pin Plastic DIP	20 Pin Plastic PLCC
600V	20Ω	12V	450V	±1%	49%	HV9106P	HV9106PJ
600V	20Ω	12V	450V	±1%	99%	HV9109P	HV9109PJ

Features

- 12 to 450V input range
- 600V, 20Ω output MOSFET
- Current-mode control
- High efficiency
- Internal start-up circuit
- Wide dynamic range

Applications

- DC/DC converters
- Distributed power systems
- Plug-in-anywhere equipment
- Appliance power
- Small off-line power supplies

Absolute Maximum Ratings

$+V_{IN}$, Input Voltage	450V
V_{DS}	600V
V_{DD}, Logic Voltage	15.0V
Control Inputs	-0.3V to V_{DD}+0.3V
I_D (Peak)	0.5A
Storage Temperature	-65°C to 150°C
Power Dissipation, Plastic DIP	750mW
Power Dissipation, PLCC	1400mW

General Description

The Supertex HV9106 and HV9109 are high-efficiency high voltage SMPS ICs intended for use in power converters requiring extreme efficiency at output power levels of 15W or less.

The HV9106/09 provides all the functions necessary to build a single-switch current-mode converter of any common topology, with a minimum of external parts.

In addition to high efficiency, because it uses Supertex's proprietary high voltage BiCMOS/DMOS technology, the HV9106/09 offers numerous performance advantages when compared to conventional PWM ICs. Dynamic range is approximately 8 times wider than with bipolar ICs, both response speed and maximum clock rate are faster, and no external power resistors or zeners are necessary for high voltage starting.

Accessory circuits are included to provide either latching or nonlatching shutdown. When shut down, device dissipation is less than 10mW.

The HV9106/09 is intended for operation with input voltages from 12 to 450VDC.

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Electrical Characteristics

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C, unless otherwise specified)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Reference							
V_{REF}	Output Voltage		3.92	4.00	4.08	V	R_L = 10MΩ
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			100	130	µA	V_{REF} = $-V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature			0.25		mV/°C	
Oscillator							
f_{MAX}	Maximum Oscillator Frequency		1	3		MHz	R_{OSC} = 0Ω
f_{OSC}	Initial Accuracy[2]		80	100	120	KHz	R_{OSC} = 330K
			160	200	240	KHz	R_{OSC} = 150K
	Voltage Stability				15	%	9.5V < V_{DD} < 13.5V
	Temperature Coefficient			170		ppm/°C	
PWM							
D_{MAX}	Maximum Duty Cycle	HV9106	49.0	49.4	49.6	%	
		HV9109	99.0	99.4	99.6		
	Deadtime	HV9109		100		nsec	
D_{MIN}	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			110	175	nsec	
Error Amplifier							
V_{FB}	Feedback Voltage		3.96	4.00	4.04	V	V_{FB} Shorted to Comp
I_{IN}	Input Bias Current			25	500	nA	V_{FB} = 4.0V
V_{OS}	Input Offset Voltage			nulled at trim		mV	
A_{VOL}	Open Loop Voltage Gain[1]		60	80		dB	
gbw	Unity Gain Bandwidth[1]		1.0	1.3		MHz	
Z_{OUT}	Output Impedance[1]			See Fig. 2		Ω	
I_{SOURCE}	Output Source Current			-2.0	-1.4	mA	V_{FB} = 3.4V
I_{SINK}	Output Sink Current		0.12	0.15		mA	V_{FB} = 4.5V
PSRR	Power Supply Rejection			See Fig. 1			
Current Limit							
V_{SOURCE}	Threshold Voltage		1.0	1.2	1.4	V	V_{FB} = 0V, R_L = 100Ω
t_d	Delay to Output[1]				150	ns	V_{SOURCE} = 1.5V, R_L = 100Ω
Pre-Regulator/Startup							
$+V_{IN}$	Allowable Input Voltage				450	V	I_{IN} = 10µA
	Input Leakage Current				10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		7.8	8.6	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	R_L = 100Ω from Drain to V_{DD}

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin ≤5pF.

Electrical Characteristics (Continued)

(V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C, unless otherwise specified)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
Supply						
I_{DD}	Supply Current		0.6	1.0	mA	V_{FB} = 4.5 Volts, Operating
			0.55		mA	$\overline{\text{Shutdown}} = -V_{IN}$
I_{BIAS}	Bias Current		20		µA	
V_{DD}	Operating Range	9.0		13.5	V	
Logic						
t_{SD}	$\overline{\text{Shutdown}}$ Delay Time[1]		50	100	ns	$V_{SOURCE} = -V_{IN}$
t_{SW}	$\overline{\text{Shutdown}}$ Pulse Width[1]	50			ns	
t_{RW}	RESET Pulse Width[1]	50			ns	
t_{LW}	Latching Pulse Width[1]	25			ns	
V_{IL}	Input Low Voltage			2.0	V	
V_{IH}	Input High Voltage	7.0			V	
I_{IH}	Input High Current		1	5	µA	V_{IN} = 10V
I_{IL}	Input Low Current		-25	-35	µA	V_{IN} = 0V
MOSFET Switch						
BV_{DSS}	Breakdown Voltage	600			V	$V_{SOURCE} = \overline{\text{Shutdown}}$ = OV, I_D = 100µA
$R_{DS(ON)}$	Drain-to-Source On-resistance		15	20	Ω	V_{SOURCE} = OV, I_D = 100mA
I_{DSS}	OFF State Drain Leakage Current			10	µA	$V_{SOURCE} = \overline{\text{Shutdown}}$ = OV, V_{DRAIN} = 100V
C_{DS}	Drain Capacitance		25		pF	V_{DS} = 25V, $\overline{\text{Shutdown}}$ = OV

Note:
1. Guaranteed by design. Not subject to production test.

Truth Table

$\overline{\text{Shutdown}}$	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

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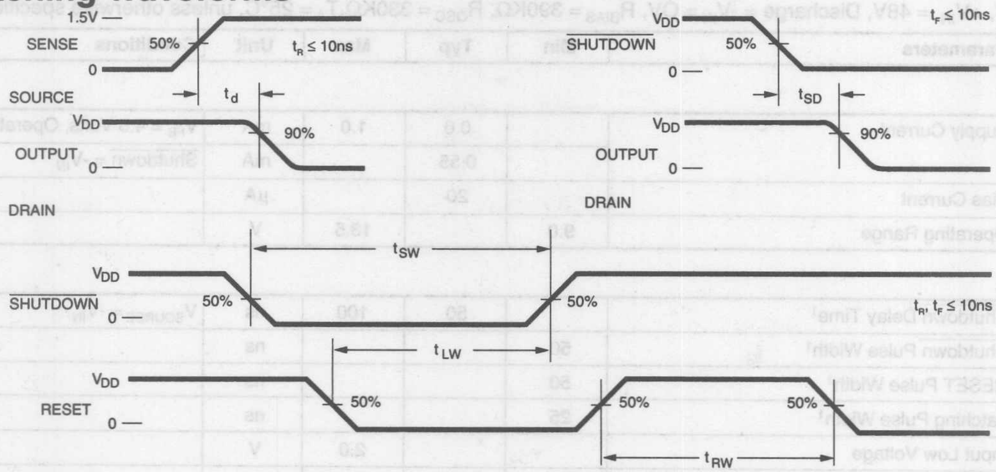
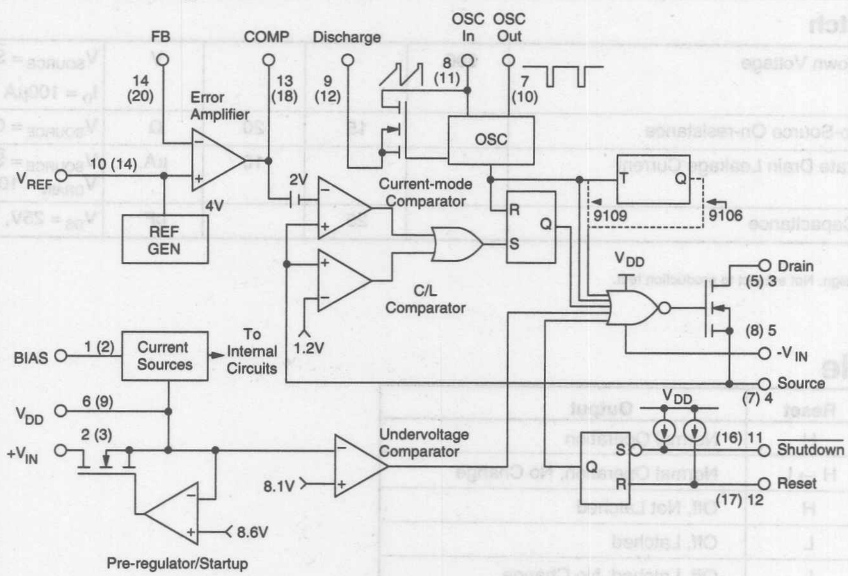
Switching Waveforms



Functional Block Diagram



Typical Performance Curves

Fig. 1 PSRR – Error Amplifier and Reference

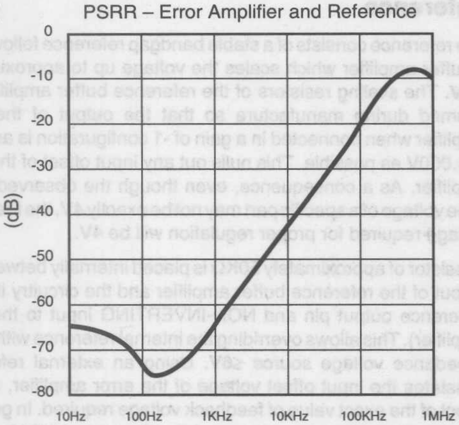


Fig. 3 Error Amplifier Open Loop Gain/Phase

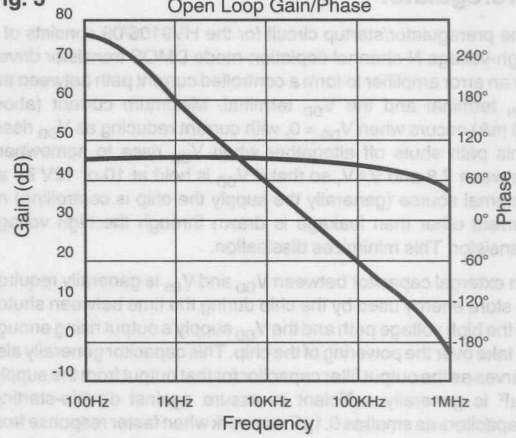


Fig. 2 Error Amplifier Output Impedance (Z_0)

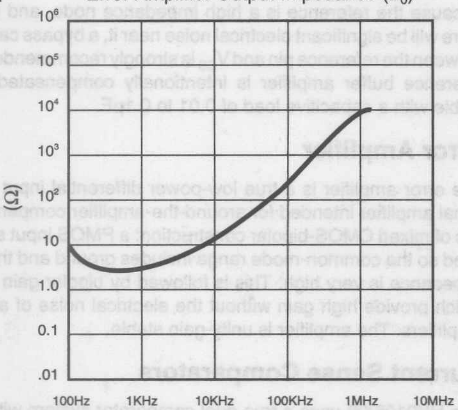
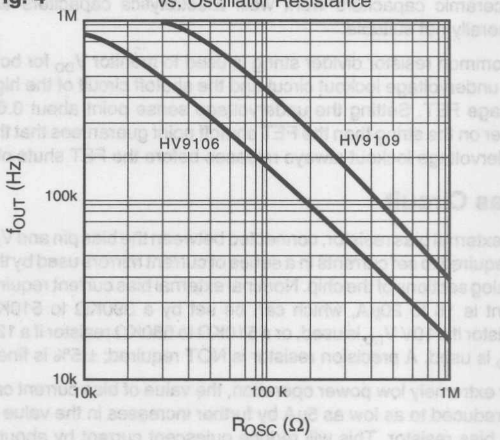
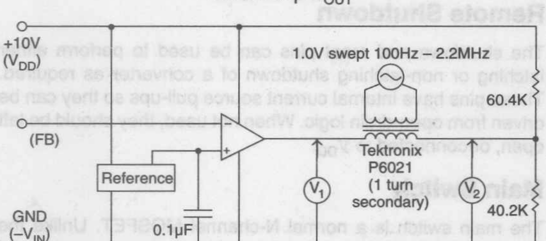


Fig. 4 Output Switching Frequency vs. Oscillator Resistance

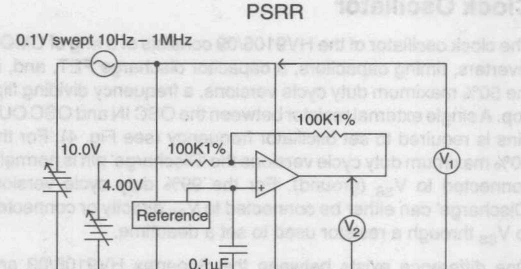


Test Circuits

Error Amp Z_{OUT}



PSRR



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

13

Technical Description

Preregulator

The preregulator/startup circuit for the HV9106/09 consists of a high-voltage N-channel depletion-mode DMOS transistor driven by an error amplifier to form a controlled current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip during the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over the powering of the chip. This capacitor generally also serves as the output filter capacitor for that output from the supply. 1µF is generally sufficient to assure against double-starting. Capacitors as small as 0.1µF can work when faster response from the V_{DD} line is required. Whatever capacitor is chosen should have very good high frequency characteristics. Stacked polyester or ceramic capacitors work well. Electrolytics capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circut and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510KΩ to 680KΩ resistor if a 12V V_{DD} is used. A precision resistor is NOT required; ± 5% is fine.

For extremely low power operation, the value of bias current can be reduced to as low as 5µA by further increases in the value of the bias resistor. This will reduce quiescent current by about a third, reduce bandwidth of the error amp by about half, and slow the current sense comparator by about 30%.

Clock Oscillator

The clock oscillator of the HV9106/09 consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC IN and OSC OUT pins is required to set oscillator frequency (see Fig. 4). For the 50% maximum duty cycle versions the 'Discharge' pin is normally connected to V_{SS} (ground). For the 99% duty cycle version, 'Discharge' can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV9106/09 and competitive parts. The oscillator of the HV9106/09 is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in situations where an absolute minimum of quiescent power dissipation is required.

Reference

The reference consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of -1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be 4V.

A resistor of approximately 50KΩ is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and NON-INVERTING input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV910x is not noisy, as some previous devices have been, overriding the reference should seldom be necessary.

Because the reference is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Error Amplifier

The error amplifier is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: a PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV9106/09 uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

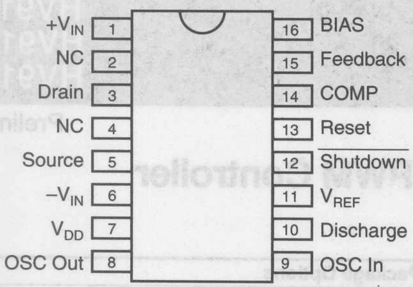
Remote Shutdown

The shutdown and reset pins can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used, they should be left open, or connected to V_{DD}.

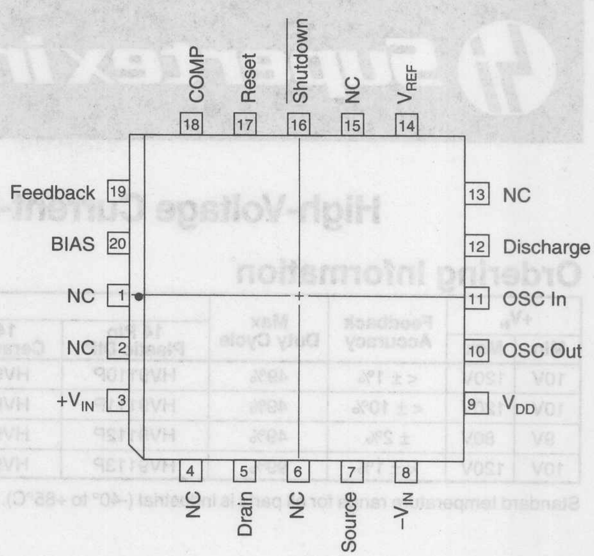
Main Switch

The main switch is a normal N-channel MOSFET. Unlike the situation with competitive devices, the body diode can be used if desired without destroying the chip.

Pinout



16 Pin DIP Package
top view



20-pin PJ Package
top view

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Supertex inc.

HV9110
HV9111
HV9112
HV9113

Preliminary

High-Voltage Current-Mode PWM Controller

Ordering Information

$+V_{IN}$		Feedback Accuracy	Max Duty Cycle	Package Options				
Min	Max			14 Pin Plastic DIP	14 Pin Ceramic DIP	20 Pin Plastic PLCC	14 Pin Narrow Body SOIC	DICE
10V	120V	< ± 1%	49%	HV9110P	HV9110C	HV9110PJ	HV9110NG	HV9110X
10V	120V	< ± 10%	49%	HV9111P	HV9111C	HV9111PJ	HV9111NG	HP9111X
9V	80V	± 2%	49%	HV9112P	HV9112C	HV9112PJ	HV9112NG	HV9112X
10V	120V	< ± 1%	99%	HV9113P	HV9113C	HV9113PJ	HV9113NG	HP9113X

Standard temperature range for all parts is industrial (-40° to +85°C). For military temperature range parts (-55° to +125°C) contact factory.

Features

- ☐ 10 to 120V input range
- ☐ Current-mode control
- ☐ High efficiency
- ☐ Up to 1MHz internal oscillator
- ☐ Internal start-up circuit
- ☐ Low internal noise

Applications

- ☐ DC/DC converters
- ☐ Distributed power systems
- ☐ ISDN equipment
- ☐ PBX systems
- ☐ Modems

Absolute Maximum Ratings

$+V_{IN}$, Input Voltage	HV9110/9111/9113	120V
	HV9112	80V
V_{DD}, Logic Voltage		15.5V
Logic Linear Input, FB and Sense Input Voltage		-0.3V to V_{DD}+0.3V
Storage Temperature		-65°C to 150°C
Power Dissipation, SOIC		750mW
Power Dissipation, Plastic DIP		1000mW
Power Dissipation, Ceramic DIP		1000mW
Power Dissipation PLCC		1400mW

General Description

The Supertex HV9110 through HV9113 are a series of BiCMOS/DMOS single-output, pulse width modulator ICs intended for use in high-speed high-efficiency switchmode power supplies. They provide all the functions necessary to implement a single-switch current-mode PWM, in any topology, with a minimum of external parts.

Because they utilize Supertex's proprietary BiCMOS/DMOS technology, they require less than one tenth of the operating power of conventional bipolar PWM ICs, and can operate at more than twice their switching frequency. Dynamic range for regulation is also increased, to approximately 8 times that of similar bipolar parts. They start directly from any DC input voltages between 10 and 120VDC, requiring no external power resistor. The output stage is push-pull CMOS and thus requires no clamping diodes for protection, even when significant lead length exists between the output and the external MOSFET. The clock frequency is set with a single external resistor.

Accessory functions are included to permit fast remote shutdown (latching or nonlatching) and undervoltage shutdown.

For similar ICs intended to operate directly from up to 450VDC input, please consult the data sheet for the HV9120/9123.

Electrical Characteristics

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Reference							
V_{REF}	Output Voltage	HV9110/13	3.92	4.00	4.08	V	R_L = 10MΩ
		HV9112	3.88	4.00	4.12		
		HV9111	3.60	4.00	4.40		
		HV9110/13	3.82	4.00	4.16		R_L = 10MΩ, T_A = -55°C to 125°C
		HV9111	3.50	4.00	4.48		
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			125	250	µA	$V_{REF} = -V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature			0.25		mV/°C	T_A = -55°C to 125°C
Oscillator							
f_{MAX}	Oscillator Frequency		1	3.0		MHz	R_{OSC} = 0Ω
f_{OSC}	Initial Accuracy[2]		80	100	120	KHz	R_{OSC} = 330KΩ
			160	200	240		R_{OSC} = 150KΩ
	Voltage Stability				15	%	9.5V < V_{DD} < 13.5V
	Temperature Coefficient			170		ppm/°C	T_A = -55°C to 125°C
PWM							
D_{MAX}	Maximum Duty Cycle	HV9110/11/12	49.0	49.4	49.6	%	
		HV9113	95	97	99		
	Deadtime	HV9113		225		nsec	
D_{MIN}	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			80	125	nsec	
Current Limit							
	Maximum Input Signal		1.0	1.2	1.4	V	V_{FB} = 0V
t_d	Delay to Output[1]			80	120	ns	V_{SENSE} = 1.5V, $V_{COMP} \leq$ 2.0V
Error Amplifier							
V_{FB}	Feedback Voltage	HV9110/13	3.96	4.00	4.04	V	V_{FB} Shorted to Comp
		HV9112	3.92	4.00	4.08		
		HV9111	3.60	4.00	4.40		
I_{IN}	Input Bias Current			25	500	nA	V_{FB} = 4.0V
V_{OS}	Input Offset Voltage			nulled during trim			except HV9111
A_{VOL}	Open Loop Voltage Gain[1]		60	80		dB	
GB	Unity Gain Bandwidth[1]		1.0	1.3		MHz	
Z_{OUT}	Output Impedance[1]			see Fig. 1		Ω	
I_{SOURCE}	Output Source Current		-1.4	-2.0		mA	V_{FB} = 3.4V
I_{SINK}	Output Sink Current		0.12	0.15		mA	V_{FB} = 4.5V
PSRR	Power Supply Rejection			see Fig. 2		dB	

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin must be ≤5pF.

Pre-regulator/Startup

$+V_{IN}$	Input Voltage	HV9110/11/13			120	V	$I_{IN} < 10\mu A$; $V_{CC} > 9.4V$
		HV9112			80		
$+I_{IN}$	Input Leakage Current				10	µA	$V_{DD} > 9.4V$
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		8.0	8.7	9.4	V	$I_{PREREG} = 10\mu A$
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	

Supply

I_{DD}	Supply Current			0.75	1.0	mA	$C_L < 75pF$
I_Q	Quiescent Supply Current			0.55		mA	$\overline{\text{Shutdown}} = -V_{IN}$
I_{BIAS}	Nominal Bias Current			20		µA	
V_{DD}	Operating Range		9.0		13.5	V	

Shutdown Logic

t_{SD}	$\overline{\text{Shutdown}}$ Delay[1]			50	100	ns	$C_L = 500pF$, $V_{SENSE} = -V_{IN}$
t_{SW}	$\overline{\text{Shutdown}}$ Pulse Width[1]		50			ns	
t_{RW}	RESET Pulse Width[1]		50			ns	
t_{LW}	Latching Pulse Width[1]		25			ns	$\overline{\text{Shutdown}}$ and reset low
V_{IL}	Input Low Voltage				2.0	V	
V_{IH}	Input High Voltage		7.0			V	
I_{IH}	Input Current, Input Voltage High			1	5	µA	$V_{IN} = V_{DD}$
I_{IL}	Input Current, Input Voltage Low			-25	-35	µA	$V_{IN} = 0V$

Output

V_{OH}	Output High Voltage	HV9110/11/13	V_{DD} -0.25			V	$I_{OUT} = 10mA$
		HV9112	V_{DD} -0.3				
		HV9110/11/13	V_{DD} -0.3				$I_{OUT} = 10mA$, $T_A = -55°C$ to 125°C
V_{OL}	Output Low Voltage				0.2	V	$I_{OUT} = -10mA$
		HV9110/11/13			0.3		$I_{OUT} = -10mA$, $T_A = -55°C$ to 125°C
R_{OUT}	Output Resistance	Pull Up		15	25	Ω	$I_{OUT} = \pm 10mA$
		Pull Down		8	20		
		Pull Up		20	30	Ω	$I_{OUT} = \pm 10mA$,
		Pull Down		10	30		$T_A = -55°C$ to 125°C
t_R	Rise Time[1]			30	75	ns	$C_L = 500pF$
t_F	Fall Time[1]			20	75	ns	$C_L = 500pF$

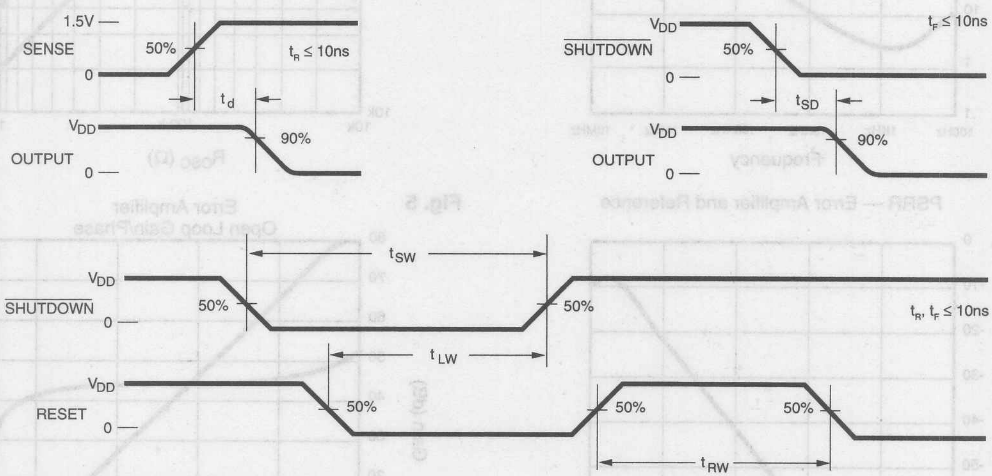
Note:

1. Guaranteed by design. Not subject to production test.

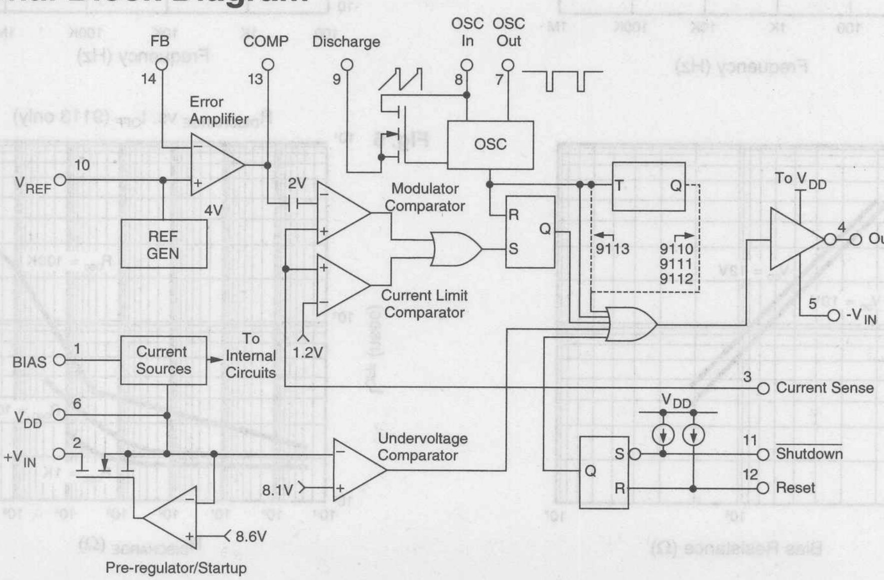
Truth Table

$\overline{\text{Shutdown}}$	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Shutdown Timing Waveforms



Functional Block Diagram



Typical Performance Curves

Fig. 1 Error Amplifier Output Impedance (Z_0)

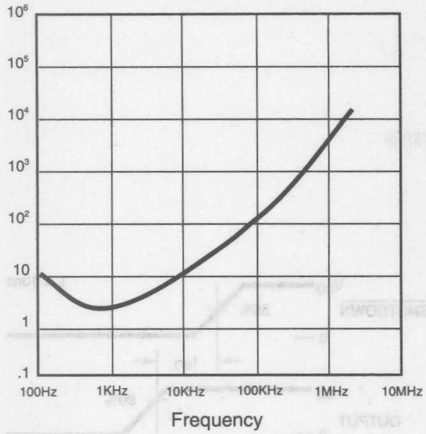


Fig. 2 PSRR — Error Amplifier and Reference

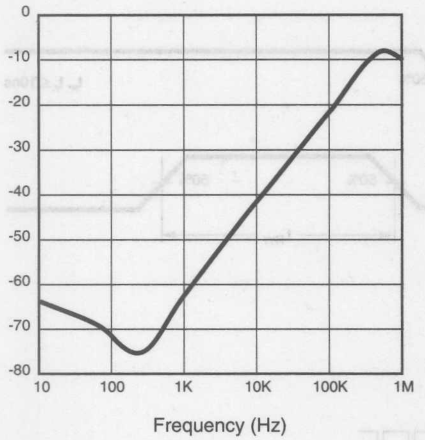


Fig. 3

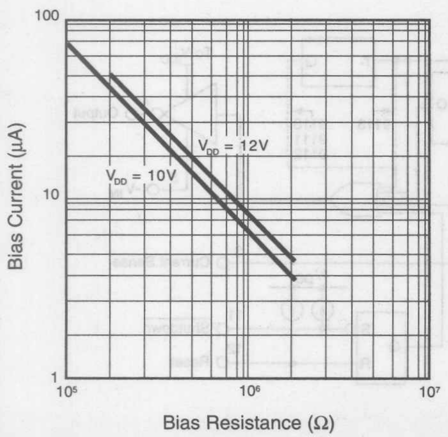


Fig. 4 Output Switching Frequency vs. Oscillator Resistance

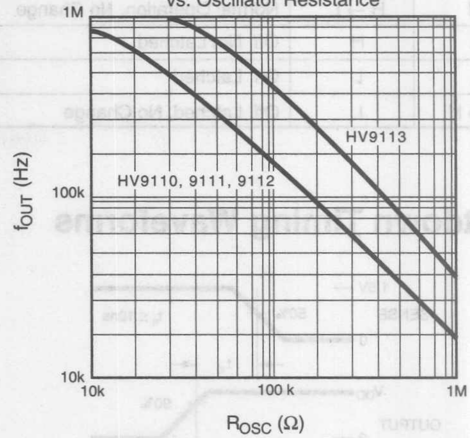


Fig. 5 Error Amplifier Open Loop Gain/Phase

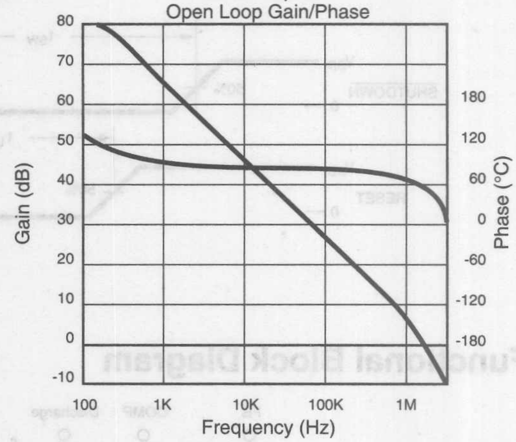
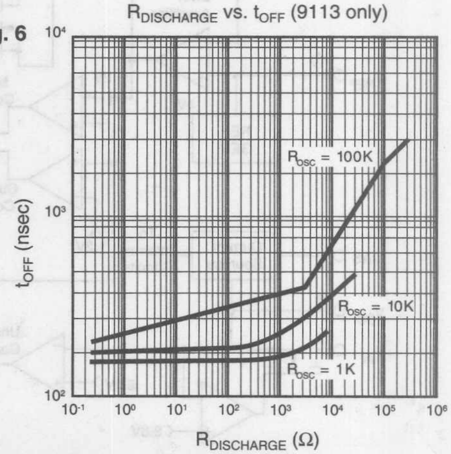
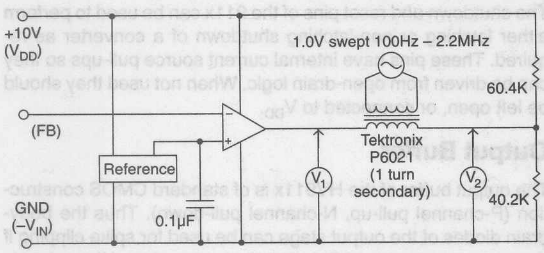


Fig. 6 $R_{DISCHARGE}$ vs. t_{OFF} (9113 only)



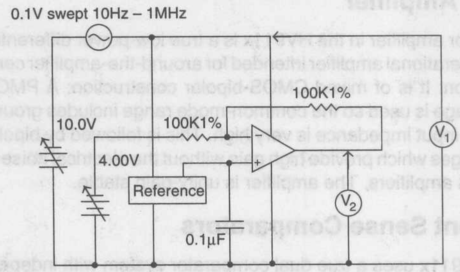
Test Circuits

Error Amp Z_{OUT}



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

PSRR



Detailed Description

Preregulator

The preregulator/startup circuit for the HV911x consists of a high-voltage n-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the *effective* gate capacitance of the MOSFET being driven, i.e.,

$C_{storage} \geq 100 \times$ (gate charge of FET at 10V ÷ 10V)

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytics capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required by the HV911x to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510kΩ to 680KΩ resistor if V_{DD} will be 12V. A precision resistor is *not* required; ± 5% is fine.

Clock Oscillator

The clock oscillator of the 911x consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC In and OSC Out pins is required to set oscillator frequency (see graph). For the 50% maximum duty cycle versions the Discharge pin is normally connected to V_{SS} (ground). For the 99% duty cycle version, Discharge can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV911x and competitive 911x's: The oscillator is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I-430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The Reference of the HV911x consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of –1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be.

A ≈50KΩ resistor is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV911x is not noisy, as some previous examples have been, overriding the reference should seldom be necessary.

Because the reference of the 911x is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

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Detailed Description (continued)

Error Amplifier

The error amplifier in the HV911x is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV911x uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

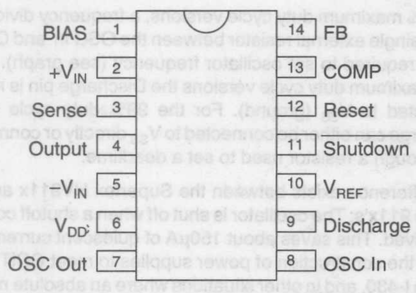
Remote Shutdown

The shutdown and reset pins of the 911x can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used they should be left open, or connected to V_{DD}.

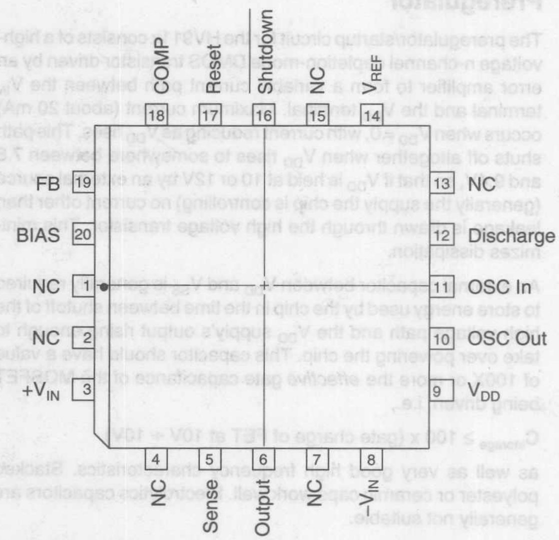
Output Buffer

The output buffer of the HV911x is of standard CMOS construction (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

Pinout



14 Pin SOIC/DIP Package



20-pin PJ Package
top view

Supertex inc.

HV9114
HV9117

Objective

High-Voltage Current-Mode PWM Controller

Ordering Information

Max Duty Cycle	Package Options			
	14 Pin Plastic DIP	14 Pin Ceramic DIP	14 Pin Narrow Body SOIC	DICE
49%	HV9114P	HV9114C	HV9114NG	HV9114X
99%	HV9117P	HV9117C	HV9117NG	HP9117X

Standard temperature range for all parts is industrial (-40° to +85°C).
For military temperature range parts (-55° to +125°C) contact factory.

Features

- ☐ Self-starting on inputs from 11V to 200V
- ☐ Extremely wide dynamic range
- ☐ Current mode control
- ☐ Leading edge spike suppression
- ☐ Practical operation to and above 1MHz
- ☐ High current totem-pole output (750mA peak)
- ☐ Wide bandwidth error amplifier
- ☐ Easy synchronization
- ☐ Accurate clock
- ☐ Programmable soft start
- ☐ Latching remote shutdown
- ☐ 1% accurate trimmed bandgap reference
- ☐ 1V typical undervoltage hysteresis
- ☐ Low operating supply current

Applications

- ☐ General-purpose controller for single-switch power supplies to 150W
- ☐ Low-volume high-efficiency power supplies
- ☐ Very high efficiency low-wattage power supplies
- ☐ Very compact power supplies
- ☐ Distributed power systems

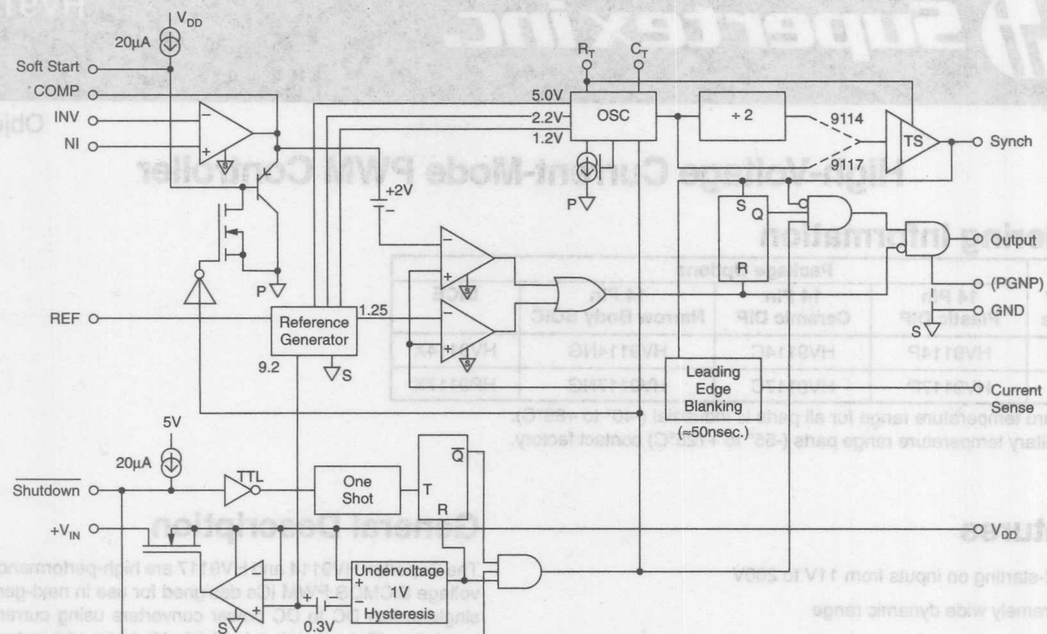
General Description

The Supertex HV9114 and HV9117 are high-performance, high-voltage BiCMOS PWM ICs designed for use in next-generation single-switch DC to DC power converters using current-mode regulation. They contain a loadable 1% trimmed bandgap reference; a wide bandwidth, low output impedance, error amplifier; a clock oscillator capable of running at well over 1MHz; a high speed current sensing comparator with leading-edge spike blanking; fully latching logic; and a large output buffer intended to drive an N-channel MOSFET.

Additional utility features include an input undervoltage lockout circuit with hysteresis, a TTL-compatible latching shutdown circuit, a programmable soft-start circuit, a system capable of achieving tri-state synchronization, and a separate ground terminal for the output (in some packages).

These parts have been designed to have a low quiescent current and an operating current of less than 3mA when running at 500KHz. They are available in plastic and ceramic dual-in-line packages and plastic surface-mount packages.

Functional Block Diagram



Supertex inc.

HV9120
HV9123

Preliminary

High-Voltage Current-Mode PWM Controller

Ordering Information

$+V_{IN}$		Feedback Accuracy	Max Duty Cycle	Package Options			
Min	Max			16 Pin Plastic DIP	16 Pin Ceramic DIP	20 Pin Plastic PLCC	DICE
10V	450V	<±2%	49%	HV9120P	HV9120C	HV9120PJ	HV9120X
10V	450V	<±2%	99%	HV9123P	HV9123C	HV9123PJ	HV9123X

Standard temperature range for all parts is industrial (-40° to +85°C).
For military temperature range parts (-55° to +125°C) contact factory.

Features

- ☐ 10 to 450V input acceptance range
- ☐ <1mA supply current
- ☐ >1MHz clock
- ☐ >20:1 dynamic range @ 500KHz
- ☐ Low internal noise

Applications

- ☐ Off-line high frequency power supplies
- ☐ Universal input power supplies
- ☐ High density power supplies
- ☐ Very high efficiency power supplies
- ☐ Extra wide load range power supplies

Absolute Maximum Ratings

Voltages are referenced to $-V_{IN}$

$+V_{IN}$ Input Voltage	450V
V_{DD} Device Supply Voltage	15.5V
Logic Input Voltages	-0.3 to V_{DD} + 0.3V
Linear Input Voltages	-0.03 to V_{DD} + 0.3V
I_{IN} Preregulator Input Current (continuous)	2.5mA
T_j Operating Junction Temperature	150° C
Storage Temperature	-65°C to 150°C
Power Dissipation, PDIP	1000mW
Power Dissipation, Ceramic DIP	1000mW
Power Dissipation PLCC	1400mW

General Description

The Supertex HV9120 and HV9123 are Switch Mode Power Supply (SMPS) controller subsystems that can start and run directly from almost any DC input, from a 12V battery to a rectified and filtered 240V AC line. They contain all the elements required to build a single-switch converter except for the switch, magnetic assembly, output rectifier(s) and filter(s).

A unique input circuit allows the 912x to self-start directly from a high voltage input, and subsequently take the power to operate from one of the outputs of the converter it is controlling, allowing very efficient operation while maintaining input-to-output galvanic isolation limited in voltage only by the insulation system of the associated magnetic assembly. A ±2% internal bandgap reference, internal operational amplifier, very high speed comparator, and output buffer allow production of rugged, high performance, high efficiency power supplies of 50 watts or more, which can still be over 80% efficient at outputs of 1W or less. The wide dynamic range of the controller system allows designs with extremely wide line and load variations with much less difficulty and much higher efficiency than usual. The exceptionally wide input voltage acceptance range also allows much better usage of energy stored in input dropout capacitors than with other PWM ICs. Remote on/off controls allow either latching or nonlatching remote shutdown. During shutdown, power required is under 6mW.

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Electrical Characteristics

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

Reference

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
V_{REF}	Output Voltage		3.92	4.00	4.08	V	R_L = 10MΩ
			3.84	4.00	4.16		R_L = 10MΩ, T_A = -55°C to 125°C
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			125	250	µA	$V_{REF} = -V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature			0.25		mV/°C	T_A -55°C to 125°C

Oscillator

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
f_{MAX}	Oscillator Frequency		1	3.0		MHz	R_{OSC} = 0Ω
f_{OSC}	Initial Accuracy[2]		80	100	120	KHz	R_{OSC} = 330KΩ
			160	200	240		R_{OSC} = 150KΩ
	Voltage Stability				15	%	9.5V < V_{DD} <13.5V
	Temperature Coefficient			170		ppm/°C	T_A = -55°C to 125°C

PWM

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
D_{MAX}	Maximum Duty Cycle	HV9120	49.0	49.4	49.6	%	
		HV9123	95	97	99		
	Deadtime	HV9123		225		nsec	
D_{MIN}	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			80	125	nsec	

Current Limit

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
	Maximum Input Signal		1.0	1.2	1.4	V	V_{FB} = 0V
t_d	Delay to Output			80	120	ns	V_{SENSE} = 1.5V, $V_{COMP} \leq$ 2.0V

Error Amplifier

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
V_{FB}	Feedback Voltage		3.92	4.00	4.08	V	V_{FB} Shorted to Comp
I_{IN}	Input Bias Current			25	500	nA	V_{FB} = 4.0V
V_{OS}	Input Offset Voltage			nulled during trim			
A_{VOL}	Open Loop Voltage Gain[1]		60	80		dB	
GB	Unity Gain Bandwidth[1]		1.0	1.3		MHz	
Z_{OUT}	Output Impedance[1]			see Fig. 1		Ω	
I_{SOURCE}	Output Source Current		-1.4	-2.0		mA	V_{FB} = 3.4V
I_{SINK}	Output Sink Current		0.12	0.15		mA	V_{FB} = 4.5V
PSRR	Power Supply Rejection			see Fig. 2		dB	

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin must be ≤5pF.

Electrical Characteristics (continued)

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = OV, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

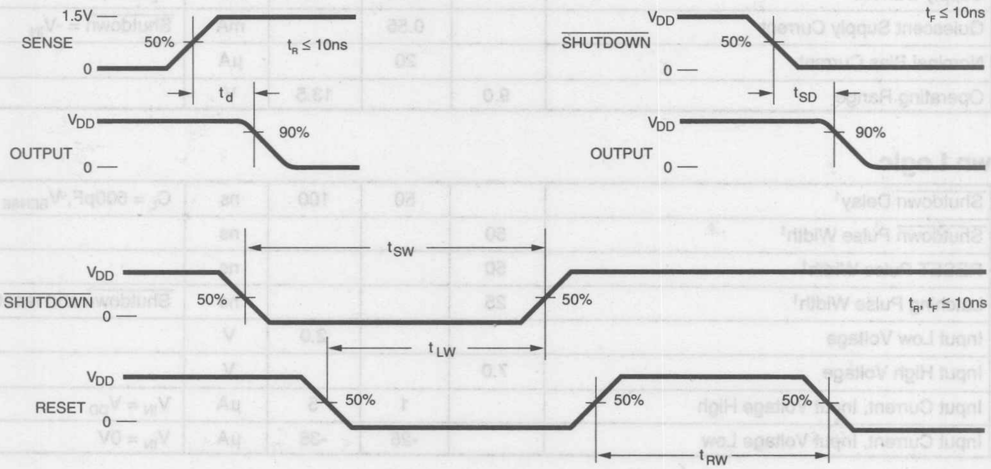
Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Pre-regulator/Startup							
$+V_{IN}$	Input Voltage				450	V	I_{IN} < 10µA; V_{CC} > 9.4V
$+I_{IN}$	Input Leakage Current				10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		8.0	8.7	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	
Supply							
I_{DD}	Supply Current			0.75	1.0	mA	C_L < 75pF
I_Q	Quiescent Supply Current			0.55		mA	$\overline{\text{Shutdown}}$ = $-V_{IN}$
I_{BIAS}	Nominal Bias Current			20		µA	
V_{DD}	Operating Range		9.0		13.5	V	
Shutdown Logic							
t_{SD}	$\overline{\text{Shutdown}}$ Delay[1]			50	100	ns	C_L = 500pF, V_{SENSE} = $-V_{IN}$
t_{SW}	$\overline{\text{Shutdown}}$ Pulse Width[1]		50			ns	
t_{RW}	RESET Pulse Width[1]		50			ns	
t_{LW}	Latching Pulse Width[1]		25			ns	$\overline{\text{Shutdown}}$ and reset low
V_{IL}	Input Low Voltage				2.0	V	
V_{IH}	Input High Voltage		7.0			V	
I_{IH}	Input Current, Input Voltage High			1	5	µA	V_{IN} = V_{DD}
I_{IL}	Input Current, Input Voltage Low			-25	-35	µA	V_{IN} = 0V
Output							
V_{OH}	Output High Voltage		V_{DD} -0.25			V	I_{OUT} = 10mA
			V_{DD} -0.3				I_{OUT} = 10mA, T_A = -55°C to 125°C
V_{OL}	Output Low Voltage				0.2	V	I_{OUT} = -10mA
					0.3		I_{OUT} = -10mA, T_A = -55°C to 125°C
R_{OUT}	Output Resistance	Pull Up		15	25	Ω	I_{OUT} = ±10mA
		Pull Down		8	20		
		Pull Up		20	30	Ω	I_{OUT} = ±10mA, T_A = -55°C to 125°C
		Pull Down		10	30		
t_R	Rise Time[1]			30	75	ns	C_L = 500pF
t_F	Fall Time[1]			20	75	ns	C_L = 500pF

Note:
1. Guaranteed by design. Not subject to production test.

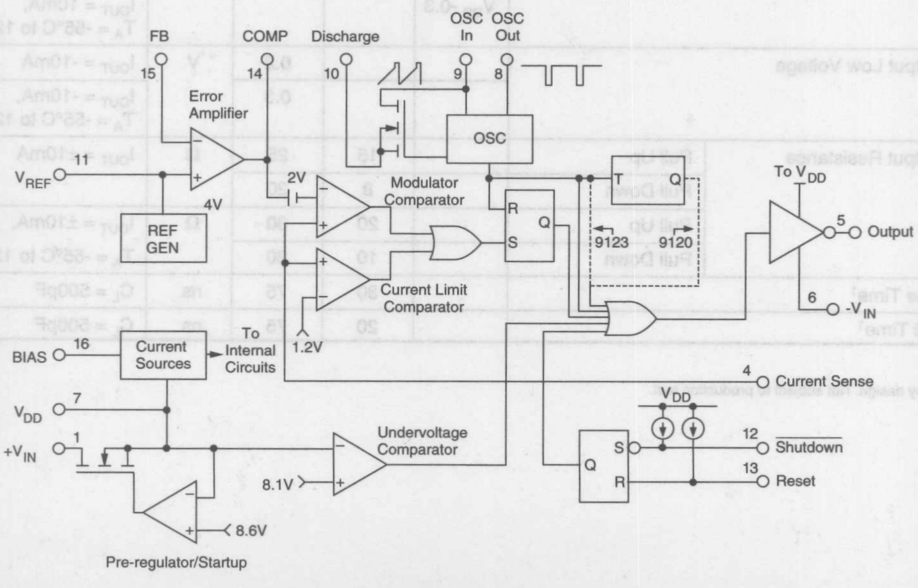
13

L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Shutdown Timing Waveforms



Functional Block Diagram



Typical Performance Curves

Fig. 1 Error Amplifier Output Impedance (Z_0)

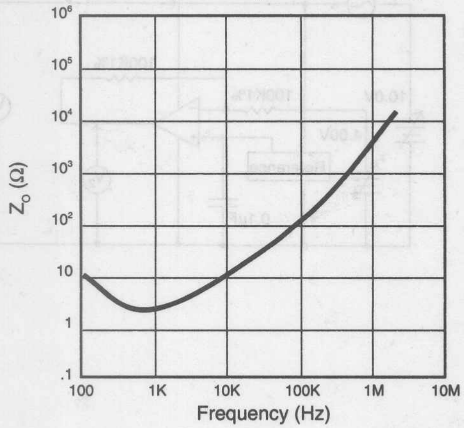


Fig. 4 Output Switching Frequency vs. Oscillator Resistance

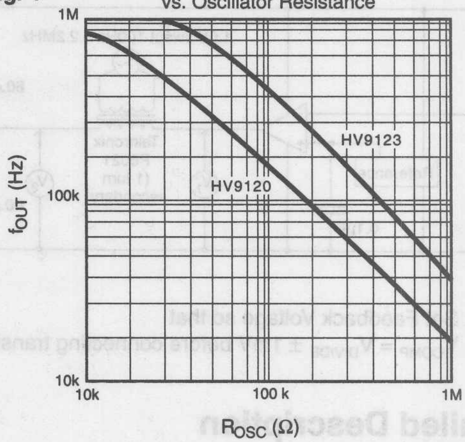


Fig. 2 PSRR — Error Amplifier and Reference

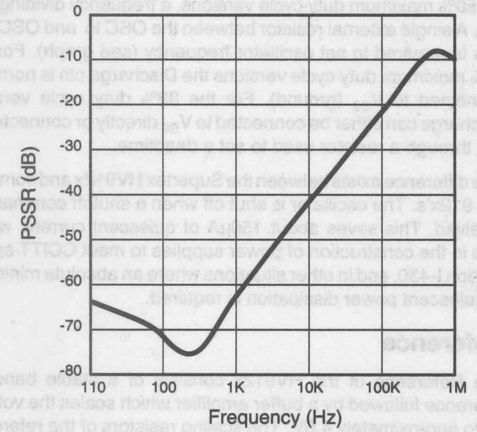


Fig. 5 Error Amplifier Open Loop Gain/Phase

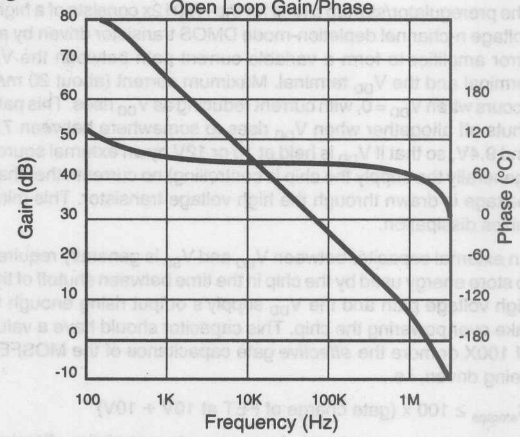


Fig. 3

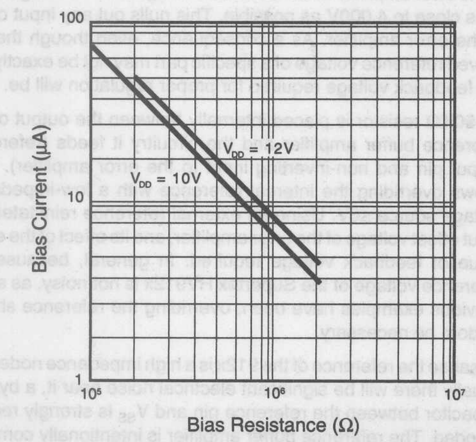
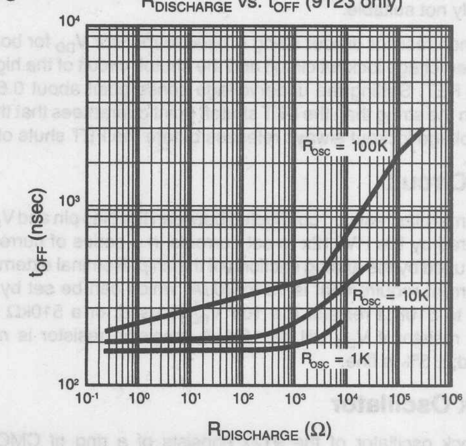


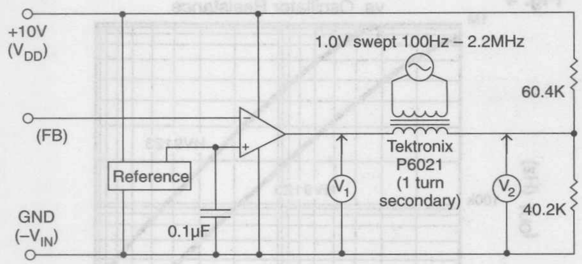
Fig. 6 $R_{DISCHARGE}$ vs. t_{OFF} (9123 only)



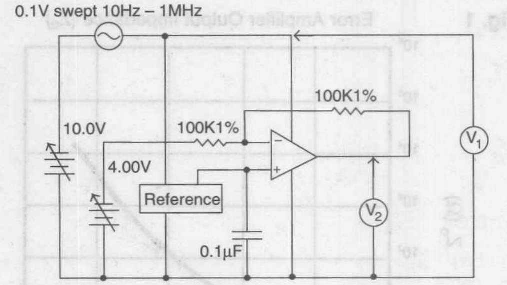
13

Test Circuits

Error Amp Z_{OUT}



PSRR



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

Detailed Description

Preregulator

The preregulator/startup circuit for the HV912x consists of a high-voltage n-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the *effective* gate capacitance of the MOSFET being driven, i.e.,

$C_{storage} \geq 100 \text{ x (gate charge of FET at } 10V \div 10V)$

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytics capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required by the HV912x to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510kΩ to 680KΩ resistor if V_{DD} will be 12V. A precision resistor is *not* required; ± 5% is fine.

Clock Oscillator

The clock oscillator of the 912x consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC In and OSC Out pins is required to set oscillator frequency (see graph). For the 50% maximum duty cycle versions the Discharge pin is normally connected to V_{SS} (ground). For the 99% duty cycle version, Discharge can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV912x and competitive 912x's: The oscillator is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I-430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The Reference of the HV912x consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of −1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be.

A ≈50KΩ resistor is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV912x is not noisy, as some previous examples have been, overriding the reference should seldom be necessary.

Because the reference of the 912x is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Detailed Description (continued)

Error Amplifier

The error amplifier in the HV912x is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV912x uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

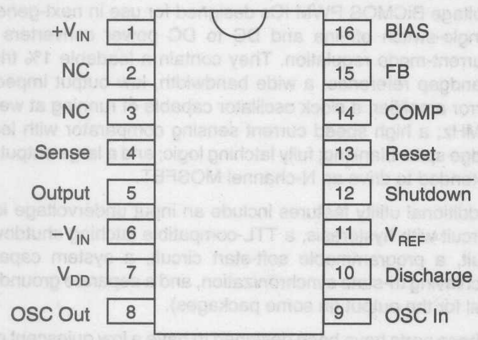
Remote Shutdown

The shutdown and reset pins of the 912x can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used they should be left open, or connected to V_{DD}.

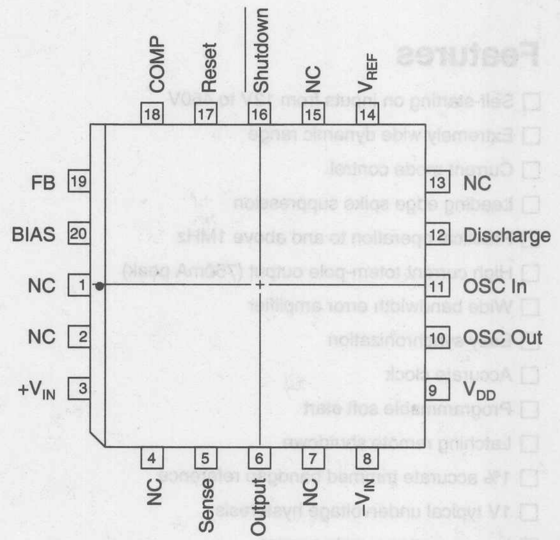
Output Buffer

The output buffer of the HV912x is of standard CMOS construction (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

Pinout



16 Pin DIP Package
top view



20-pin PJ Package
top view

Supertex inc.

HV9124
HV9127

Objective

High-Voltage Current-Mode PWM Controller

Ordering Information

Max Duty Cycle	Package Options			
	16 Pin Plastic DIP	16 Pin Ceramic DIP	16 Pin Plastic PLCC	DICE
49%	HV9124P	HV9124C	HV9124PJ	HV9124X
99%	HV9127P	HV9127C	HV9127PJ	HP9127X

Standard temperature range for all parts is industrial (-40° to +85°C).
For military temperature range parts (-55° to +125°C) contact factory.

Features

- ☐ Self-starting on inputs from 12V to 450V
- ☐ Extremely wide dynamic range
- ☐ Current mode control
- ☐ Leading edge spike suppression
- ☐ Practical operation to and above 1MHz
- ☐ High current totem-pole output (750mA peak)
- ☐ Wide bandwidth error amplifier
- ☐ Easy synchronization
- ☐ Accurate clock
- ☐ Programmable soft start
- ☐ Latching remote shutdown
- ☐ 1% accurate trimmed bandgap reference
- ☐ 1V typical undervoltage hysteresis
- ☐ Low operating supply current

Applications

- ☐ General-purpose controller for single-switch power supplies to 150W
- ☐ Low-volume high-efficiency power supplies
- ☐ Very high efficiency low-wattage power supplies
- ☐ Very compact power supplies
- ☐ Universal input power supplies

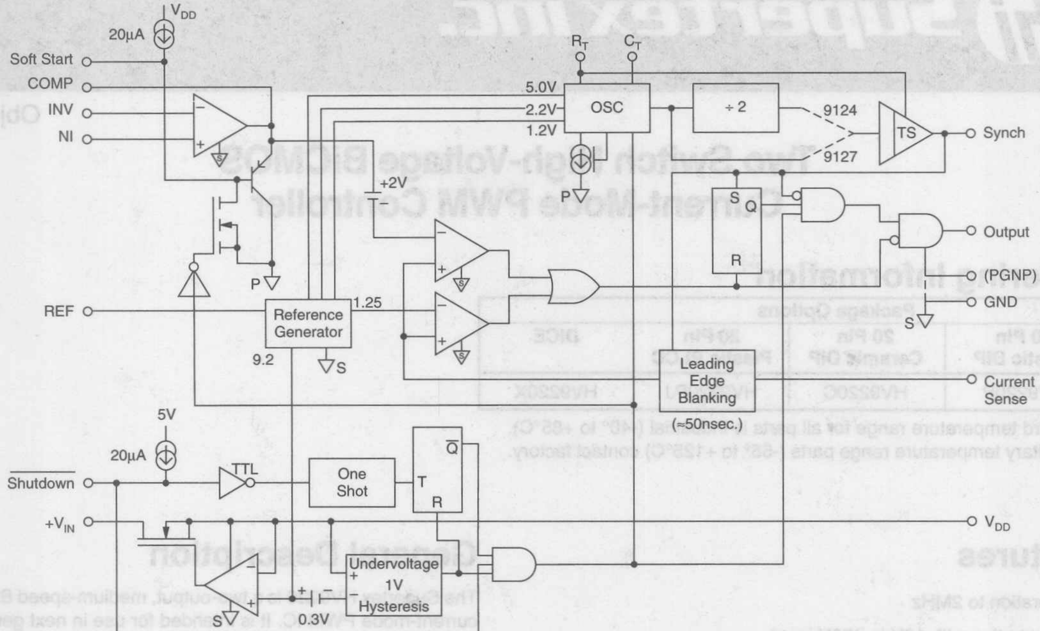
General Description

The Supertex HV9124 and HV9127 are high-performance, high-voltage BiCMOS PWM ICs designed for use in next-generation single-switch off-line and DC to DC power converters using current-mode regulation. They contain a loadable 1% trimmed bandgap reference; a wide bandwidth, low output impedance, error amplifier; a clock oscillator capable of running at well over 1MHz; a high speed current sensing comparator with leading-edge spike blanking; fully latching logic; and a large output buffer intended to drive an N-channel MOSFET.

Additional utility features include an input undervoltage lockout circuit with hysteresis, a TTL-compatible latching shutdown circuit, a programmable soft-start circuit, a system capable of achieving tri-state synchronization, and a separate ground terminal for the output (in some packages).

These parts have been designed to have a low quiescent current and an operating current of less than 3mA when running at 500KHz. They are available in plastic and ceramic dual-in-line packages and plastic surface-mount packages.

Functional Block Diagram



Supertex inc.

Objective

Two Switch High-Voltage BiCMOS Current-Mode PWM Controller

Ordering Information

Package Options			
20 Pin Plastic DIP	20 Pin Ceramic DIP	20 Pin Plastic PLCC	DICE
HV9220P	HV9220C	HV9220PJ	HV9220X

Standard temperature range for all parts is industrial (-40° to +85°C).
For military temperature range parts (-55° to +125°C) contact factory.

Features

- ☐ Operation to 2MHz
- ☐ Self-starting with 10V to 450V input
- ☐ Easy synchronization with PFC ICs
- ☐ Low power high speed BiCMOS
- ☐ Available in surface mount and chip form
- ☐ Two 1.5A CMOS outputs
- ☐ 1% trimmed bandgap reference
- ☐ Oscillator accuracy ±1%
- ☐ Customer-set undervoltage ON and OFF

Applications

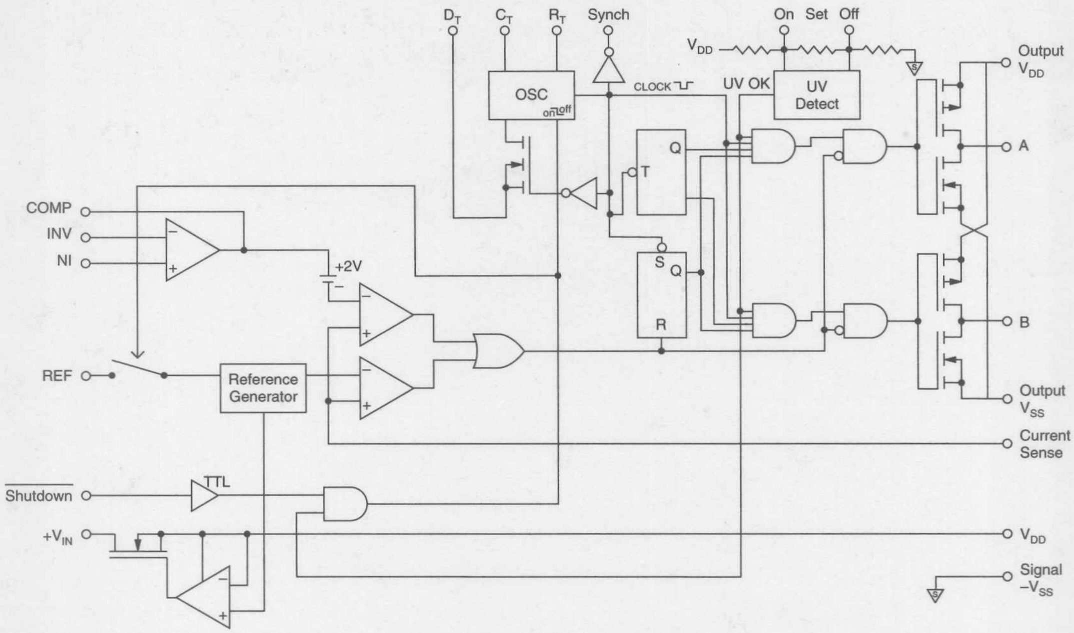
- ☐ Medium to high power converters/inverters
- ☐ Very compact power converters
- ☐ High efficiency converters
- ☐ High frequency power converters

General Description

The Supertex HV9220 is a two-output, medium-speed BiCMOS, current-mode PWM IC. It is intended for use in next generation tow- and four-switch fixed frequency switchmode power converters. On-board functions include: a 1% accurate clock oscillator capable of operating to well beyond 2MHz, with synchronization port and deadtime control; a 1% accurate, loadable, trimmed bandgap reference; fully latched steering and modulation logic, with double pulse prevention; two 1.5A peak totem-pole outputs; an undervoltage circuit where tip point and hysteresis are both user-programmable; a fast current sensing circuit; a >2MHz bandwidth fully accessible error amplifier; a direct-from-high-voltage starting circuit; and a TTL-compatible remote shutdown circuit.

The use of separate ground pins for linear and switching sections of the IC, assisted by the use of bipolar transistors where needed, allows exceptionally precise low noise operation of the linear sections. The DMOS output structure, with fast body diodes, eliminates the need for protective clamping diodes on the outputs, accepts inductive kickbacks (up to peak output current) without damage, and allows the unit to drive either MOSFETs or gate transformers unassisted. The high voltage input MOSFET allows direct self-starting from any input from 10V to 450V without the need for a housekeeping power supply. The industry's first 1% accurate clock allows better control over magnetics sizes than has previously been the case, and aids in the production of medium-stability inverters. The circuit is built on an EPI layer to eliminate the possibility of latchup form inductive ringing or low-level radiation.

Functional Block Diagram



Chapter 14 – CMOS Consumer/Industrial Products

Supertex inc.

Programmable Data Coder

Ordering Information

Device	28-Pin Plastic DIP	28-Pin Plastic Quad J Lead	28-Pin SO Gullwing	Die
DC7	DC7P	DC7PJ	DC7WG	DC7X

Features

- 8 data bits (byte wide data)
- 7 address bits (128 addresses)
- Manchester phase encoding
- Transmitter/receiver in one circuit
- Schmitt trigger input for excellent noise rejection
- Built-in oscillator using non-critical RC components
- Zener diode to regulate the power supply
- Low power, high noise immunity CMOS technology
- Ability to decode original signals
- Automatic preamble generation

Applications

- Multi-port computer I/O
- Smoke & fire alarm control systems
- Pocket pagers
- Digital locks
- Theft alarm systems
- Security systems
- Digital paging systems
- Special identification code systems
- Remote sensor data acquisition systems
- Single channel digital transmission of information

General Description

The DC7 is a single monolithic chip using metal gate CMOS technology for low cost, low power, high yield and high reliability. This dual purpose circuit is capable of working either as an encoder, or decoder of its own transmission, in applications where exclusive recognition of address codes is required in addition to transmission or reception of 8 data bits. It will decode 1 of 128 address codes. In the transmit mode, this circuit is capable of generating the possible codes by connecting the Address and Data Inputs to V_{DD} or GND for a "1" or a "0". In the receive mode, this circuit is capable of decoding the transmitted signals and simultaneously making comparisons to the local address code for identification.

Absolute Maximum Ratings

Supply Voltage with respect to GND	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GND = 0V; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	GND - 0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for pins T/R, SDI
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, A0 - A6, D0 - D7
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	$V_{OH} = V_{DD}$ - 1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{OUT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GND all outputs floating

Notes:
1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.
2. This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

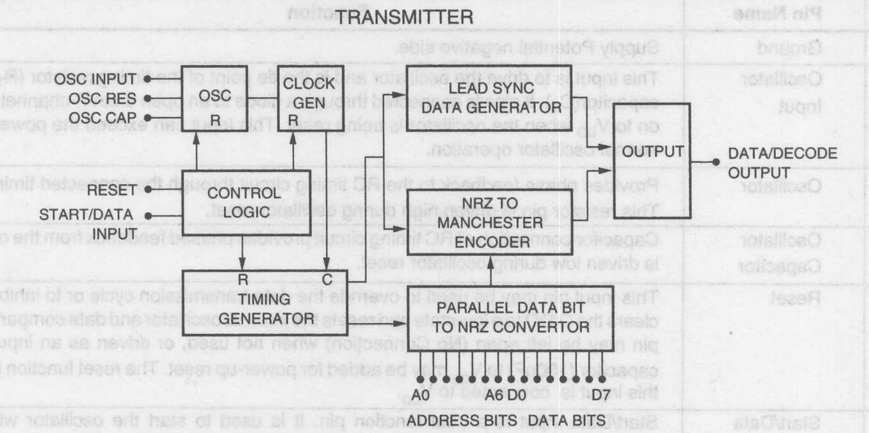
Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
f_C	Clock Frequency	0		20	kHz	R = 150k, C = 100pF; Clock Period (t_C) = 1/f_c
t_{SDI}	Start Pulse Width	500			ns	
t_{DDO}	DDO Delay from SDI		5		µs	
t_{DC}	Data Clock Pulse Width		.5t_C		sec	
t_{WORD}	Full Cycle Word Length		130t_C		sec	
R_R	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
C_R	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

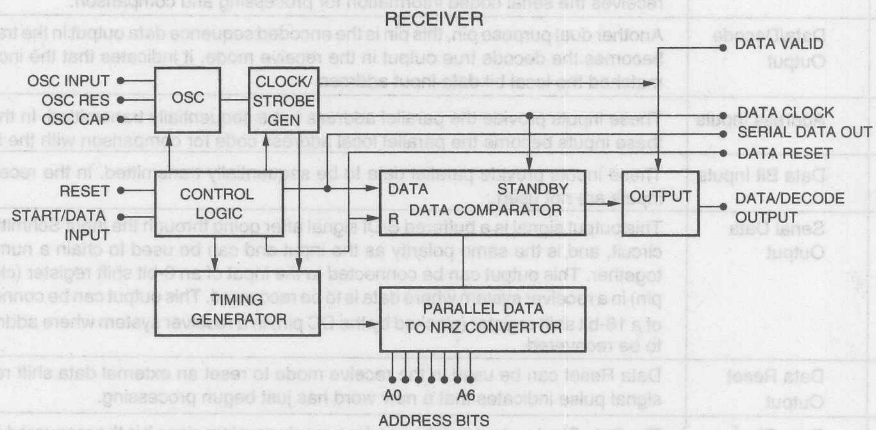
Note:
1. Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor(C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies during normal oscillator operation.
OR	Oscillator	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note: This resistor pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
RS	Reset	This input pin may be used to override the data transmission cycle or to inhibit an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pF) to V_{DD} may be added for power-up reset. The reset function is activated when this input is connected to V_{DD}.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And, in the receive mode, this input receives the serial coded information for processing and comparison.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
A0-A6	Address Inputs	These inputs provide the parallel address to be sequentially transmitted. In the receive mode, these inputs become the parallel local address code for comparison with the incoming data.
D0-D7	Data Bit Inputs	These inputs provide parallel data to be sequentially transmitted. In the receive mode, these inputs are not used.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmitt Trigger, a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of an 8-bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered. This output can be connected to the input of a 16-bit shift register (clocked by the DC pin) in a receiver system where address and data are to be recovered.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this signal pulse indicates that a new word has just begun processing.
DC	Data Clock Outputs	The Data Clock output may be used in a receive system since it is the recovered data sync pulses. Also, this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode; a logic low puts it in the receive mode.
V_{DD}	V_{DD}	Positive Supply Potential: This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Block Diagrams





Operation

General

The DC7 mode of operation is controlled by the transmit/receive control input (T/R). When switched from V_{DD} to GND, the circuit will automatically change the oscillator, start/data input, and data decoder output from transmit to receive mode.

The DC7 contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5%, or from a regulated power supply in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1 - D_{15} drivers, the resistors should be tied to a voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0mA minimum at 1.0 volt V_{DS} . All inputs are gate protected to both power supplies by internal diodes. The Address Data Inputs of the DC7 each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The transmit/receive input does not have a pull up or pull down resistor. The start/data input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger Input circuit to improve noise rejection.

Transmit Function

This function is selected by connecting the transmit/receive control input to V_{DD}. This enables the transmit mode and the circuit to function, as an encoder, sampling the 7 address and 8 data input pin digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded) and presenting it to the D/DO pin for transmission (usually to another DC device used as the decoder circuit). The encoder will transmit the serial data each time the start/data input is activated.

This encoded data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1"s and then a space indicating that the encoded data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 7 bits of address and 8 bits of data.

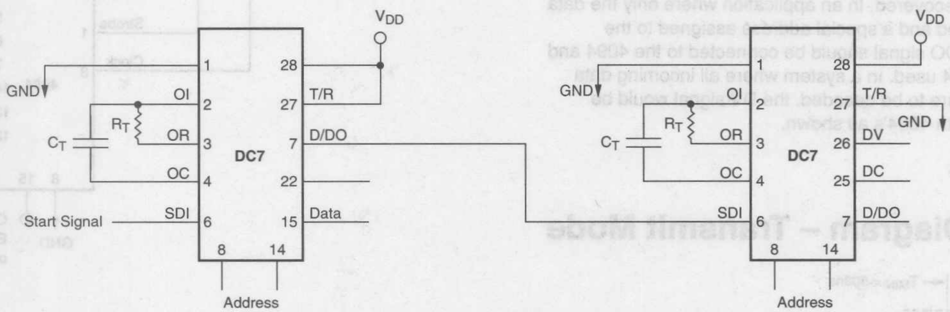
Receive Function

The receive mode is selected by connecting the transmit/receive control input to ground. In this mode the circuit will work as a decoder receiving the serial data in Manchester Encoded format and recovering the clock. The incoming data is converted to a 15-bit serial word. It is compared with the local address word by sampling the address inputs (7-bits). These bits are usually programmed to the expected address that will be decoded. If the two address words match, the decoded output will go to a logic "1" state, but if the two do not match the decoded output will stay low. Also, if the words do not match but the bit stream was valid (i.e., 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12-bits will be recognized. But, during the 13th interval where no bit transition occurs, the circuit times out and awaits the start bit of the address and data sequence.

The DC7 will only compare the first 7 bits and ignore the state of the last 8- bits — that is, 128 distinct address codes with 8 bits that may be used for data transmission.

Transmit and Receive Address and Data Patterns

DC7 to DC7



Transmitted Bit Sequence

1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	A0						A6	D0							D7

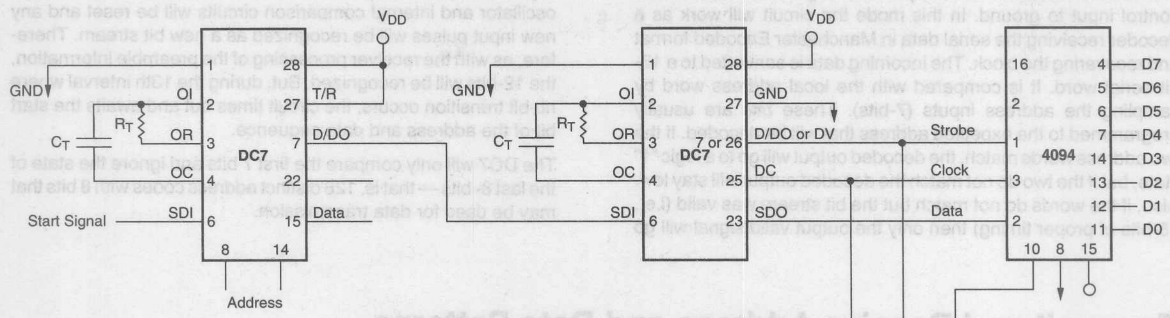
Received Address Code

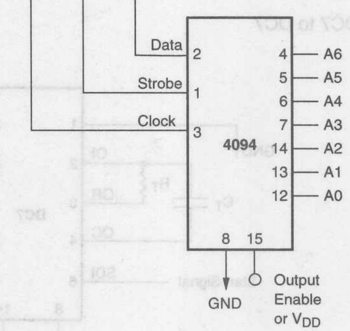
1	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D
	A0						A6	D0							D7

Note: Bit Sequence Code Format
X = Programmable
0 = Hardwired Internally Zero
1 = Hardwired Internally One
D = Don't Care in Receive Mode (Data)

When unused, the DV, DC, DRS and SDO pins should be left floating and **must not** be tied to either a power supply or to ground.

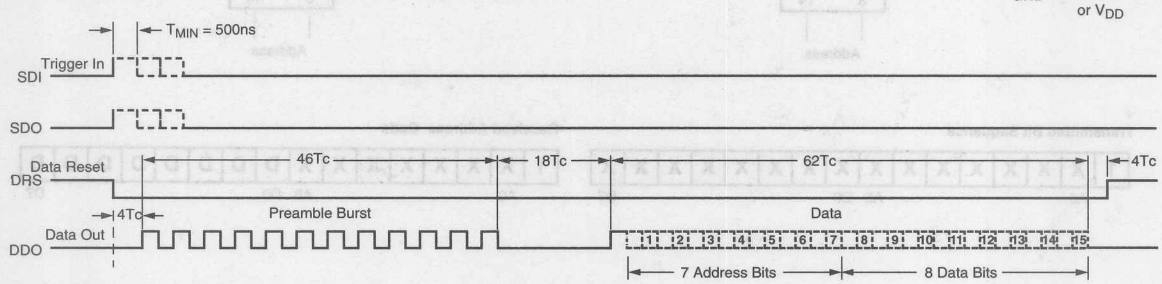
Typical Application





The circuit shown above demonstrates the use of the DC7 where both the data and address bits can be transmitted from one location to another and both the data and address bits of the transmitter recovered. In an application where only the data is to be recovered and a special address assigned to the receiver, the D/DO signal should be connected to the 4094 and only the top 4094 used. in a system where all incoming data and addresses are to be decoded, the DV signal would be connected to both 4094's as shown.

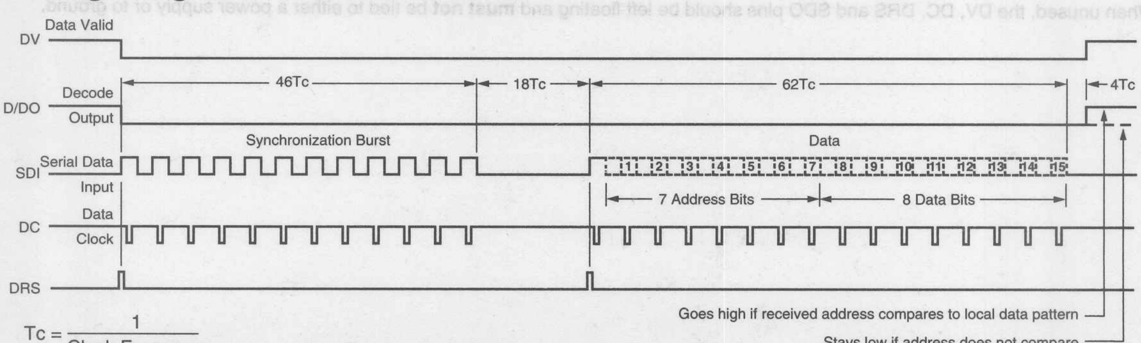
Timing Diagram – Transmit Mode



Total Time Required for Transmission of One Sequence = (DRS – 4Tc) =130Tc

$$Tc = \frac{1}{\text{Clock Frequency}}$$

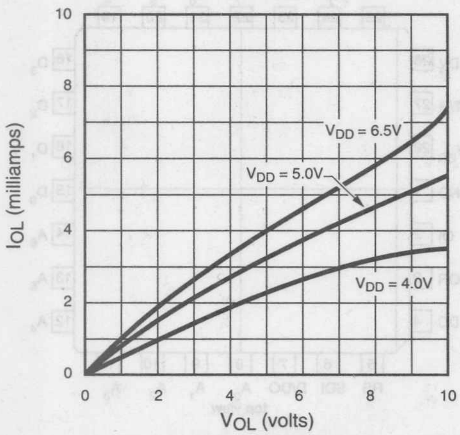
Timing Diagram – Receive Mode



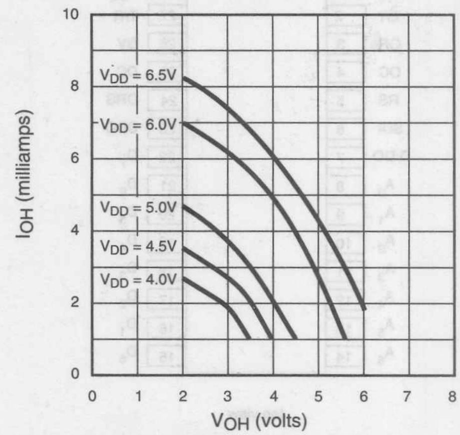
$$Tc = \frac{1}{\text{Clock Frequency}}$$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

I_{OL} vs V_{DD} vs D_{OL}

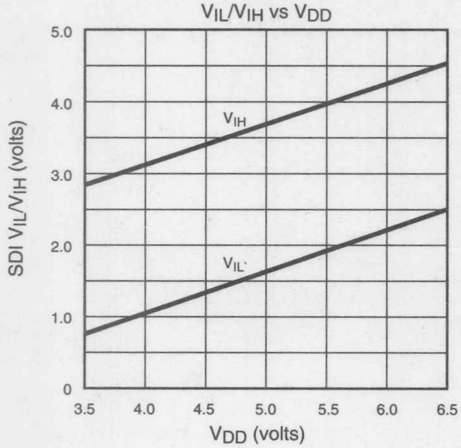


I_{OH} vs V_{DD} vs V_{OH}

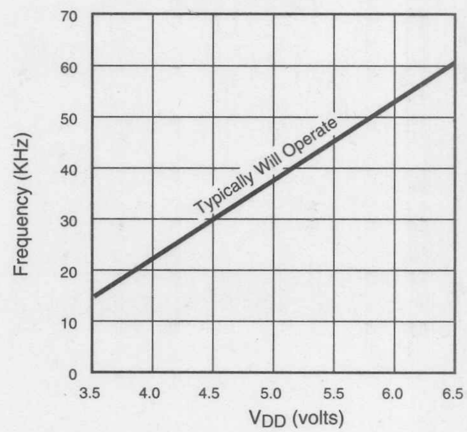


SDI Input

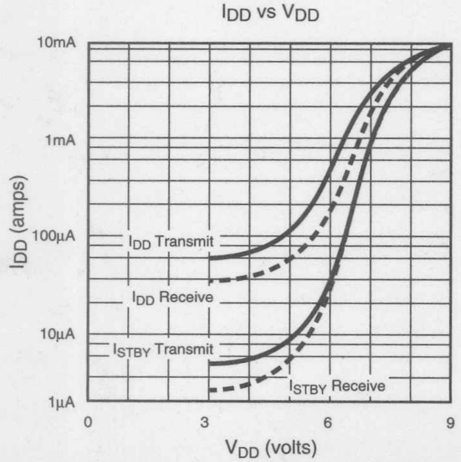
V_{IL}/V_{IH} vs V_{DD}



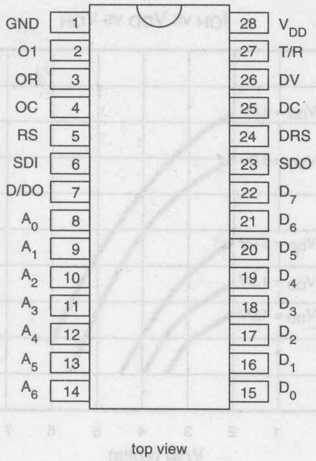
Operating Frequency vs V_{DD}



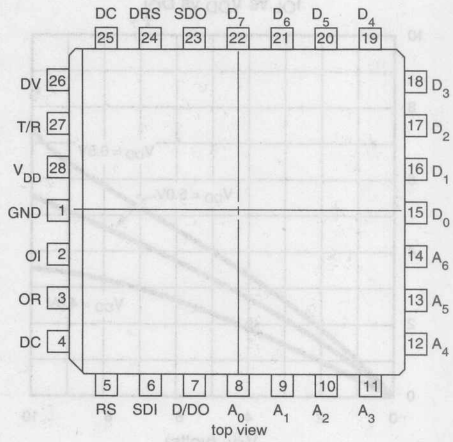
I_{DD} vs V_{DD}



Pin Configuration



28-pin DIP and 28-pin SOW



28-pin J-lead Package

Supertex inc.

ED5, ED9, ED9R
ED10, ED11
ED15, ED15R

Programmable Encoder/Decoder

Ordering Information

Device	Package			
	Plastic DIP (#Pins)	J-Lead PLCC (# pins)	Plastic SOW Gullwing (# pins)	Die
ED5	ED5P (18)	—	—	—
ED9	ED9P (18)	—	ED9WG (20)	—
ED9R*	ED9RP(18)	—	ED9RWG (20)	—
ED10	—	—	ED10WG (20)	—
ED11	ED11P (28)	—	ED11WG (28)	—
ED15	ED15P (28)	ED15PJ (28)	ED15WG (28)	ED15X
ED15R*	ED15RP (28)	ED15RPJ (28)	ED15RWG (28)	ED15RX

* Gate-protected version

Features

- ☐ Manchester phase encoding
- ☐ Encoder/decoder in one circuit
- ☐ Schmitt Trigger Input for excellent noise rejection
- ☐ Built-in oscillator using non-critical RC components
- ☐ Zener diode to regulate the power supply
- ☐ Low power, high noise immunity CMOS technology
- ☐ Ability to decode original signals
- ☐ Automatic preamble generation
- ☐ Ruggedized devices available

Applications

- ☐ Smoke & fire alarm control systems
- ☐ Security systems
- ☐ Theft alarm systems
- ☐ Digital locks
- ☐ Digital paging systems
- ☐ Garage door openers
- ☐ Systems that require a special identification code
- ☐ Pocket pagers
- ☐ Recognition or transmission

General Description

The ED series is a single monolithic chip using metal-gate CMOS technology for low cost, low power, high yield and high reliability. It is a dual purpose circuit, capable of working either as an encoder, or as decoder of its own transmissions, in applications where exclusive recognition of a special code is required. It will decode up to1 of 32,768 codes. In the transmit mode, each circuit is capable of generating the possible codes by connecting the Data Inputs to V_{DD} or GND for a "1" or a "0". In the receive mode, each circuit is capable of decoding the transmitted signal and simultaneously making a comparison to the local address code for identification.

'R' version products are ruggedized to provide greater protection against ESD damage caused by improper handling. These devices are gate-protected and meet the 2000V ESD ratings of EIA standards. The oscillation frequency is also different between the "R" version and the standard device when the same RC network is used. Please refer to the typical performance curves for details.

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Absolute Maximum Ratings

Supply Voltage with respect to GND	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

Note: All inputs of non-'R' version device, except OI, contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range.

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GND = 0V; T_A = 25°C)

Symbol	Parameter	Min	Typ Note 1	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	GND- 0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for pins T/R, SDI
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, D1-D15
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{OUT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GND all outputs floating

Notes:
1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.
2 This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ Note1	Max	Unit	Conditions
f_c	Clock Frequency	0		20	kHz	R=150k, C= 100pF; Clock Period (t_c)=1/f_C
t_{SDI}	Start Pulse Width	500			ns	
t_{DDO}	DDO Delay from SDI		5		µs	
t_{DC}	Data Clock Pulse Width		.5t_C		sec	
t_{WORD}	Full Cycle Word Length		130t_C		sec	
R_R	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
C_R	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor (C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note: This pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.

RS	Reset Input	This input pin may be used to override the data transmission cycle or to inhibit an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pf) to V_{DD} may be added for power-up reset. The Reset function is activated when this input is connected to V_{DD}.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And in the receive mode, this input receives the serial coded information for processing and comparison.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
D1-D15	Data Bit Inputs	These Inputs provide parallel input data to be sequentially transmitted. The 18-pin package options have some pins omitted and hence these data positions will have logical zeros transmitted. In the receive mode, these imputs become the parallel local address code for comparison with the incoming data. Note that with the ED11 and ED5 options, the data bits 11-15 are not used in the comparison when in the receive mode.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmitt Trigger, a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of a 16-bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered regardless of its comparison to a preset address word.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this Output signal pulse indicates that a new word has just begun processing.
DC	Data Clock Output	The Data Clock output may be used in a receive system since it is the recovered data sync pulses. Also, this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode; a logic low puts it in the receive mode.
V_{DD}	V_{DD}	Positive Supply Potential: This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Operation

ED15 and ED15R General Description

The ED15 and ED15R series mode of operation is controlled by the Transmit/Receive control input (T/R). When switched from V_{DD} to GND, the circuit will automatically change the oscillator, Start/Data input, and Data/Decoder Output from Transmit to Receive mode.

The circuit contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5% in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1 - D_{15} drives, the resistors should be tied to a voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0 mA minimum at 1.0 volt V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The Data Inputs each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The Transmit/Receive input does not have a pull up or pull down resistor. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger Input circuit to improve noise rejection.

Encoder Function

This function is selected by connecting the Transmit/Receive control input to V_{DD}. This enables the Transmit mode and the circuit to function as an encoder, sampling the 15 Data Input pins' digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded), and presenting it to the D/DO pin for transmission (usually to another ED device used as the decoder circuit). The encoder will transmit the serial data each time the Start/Data input is activated.

This encoded Data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1's", then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 15 bits of addresses and/or controls.

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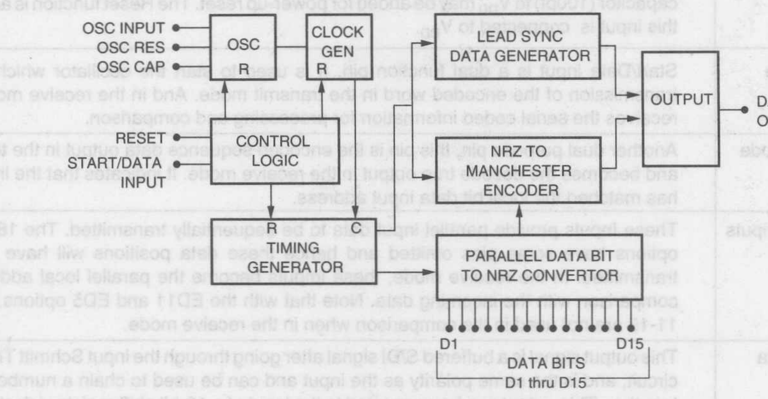
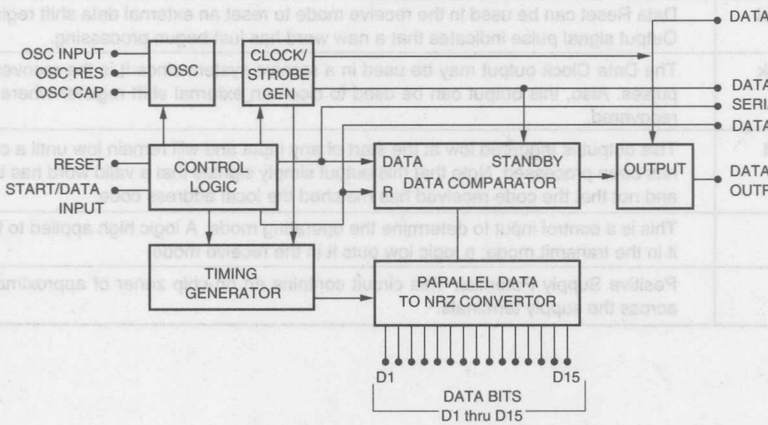
Block Diagrams

TRANSMITTER



RECEIVER



Decoder Function

The receive mode is selected by connecting the Transmit/Receive control input to ground. In this mode the circuit will work as a decoder, receiving the serial data in Manchester Encoded format and recovering the clock. The incoming data is converted to a 15-bit serial word. It is compared with the local data word by sampling the Data Inputs (15-bits). These bits are usually programmed to the expected Data that will be decoded. If the two data words match, the decoded output will become logic "1" state, but if the two words do not match the decoded output will stay low. Also, if the words do not match but the bit stream was valid (i.e., 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12 bits will be recognized. But during the 13th interval where no bit transition occurs, the circuit times out and awaits the start bit of the data sequence.

ED5 Option

The 18-pin packaging option of the ED11 die is called ED5. In the transmit mode it is only capable of 5 bits of programmable code. All the other bits are held at zero. But in the receive mode, the circuit has the five (32) unlock code bits plus the last four transparent bits of the ED11. The ED5 also supplies the necessary output signals to process the 4 bits of control data.

ED9 and ED9R Option

The ED9 and ED9R are18-pin packaging of the ED15 and ED15R die. The operation and function of this circuit is the same as the ED15 and ED15R; the only difference being the available pins. In the transmit mode the circuit is only capable of encoding 9 bits of data, the other 6 bits are not programmable and remain zeros. The pin configuration also drops DV, DC, DRS, and SDO such that the circuit can now only respond to a data match condition on the only output, #D/DO. In the receive mode the circuit can decode the same 9 bits of data, enabling up to 512 possible addresses.

ED10 Option

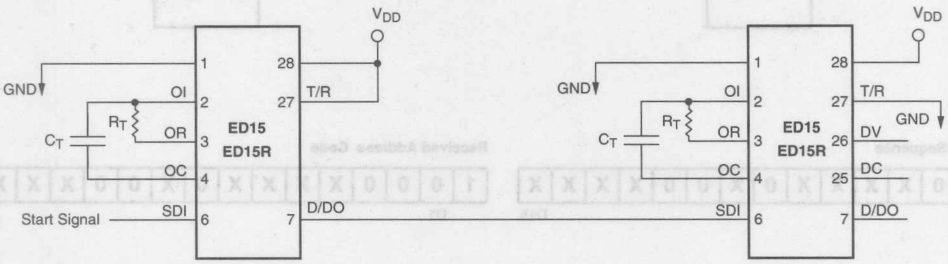
TheED10 is an ED9 in the 20-pin package. The 2 additional pins are one more data pin (hence ED10) and the DRS pin. The latter is useful for multiple transmissions as shown in the Figures below. This can lead to more reliable reception in some circumstances.

ED11 Option

The ED11 differs from the ED15 in that in the receive mode the ED11 will only compare the first 11 bits and ignore the state of the last 4 bits; that is, 2048 distinct address codes with 4 bits may be used for control data transmission.

Transmit and Receive Data Patterns of ED-Series Devices

ED15 to ED15 and ED15R and ED15R



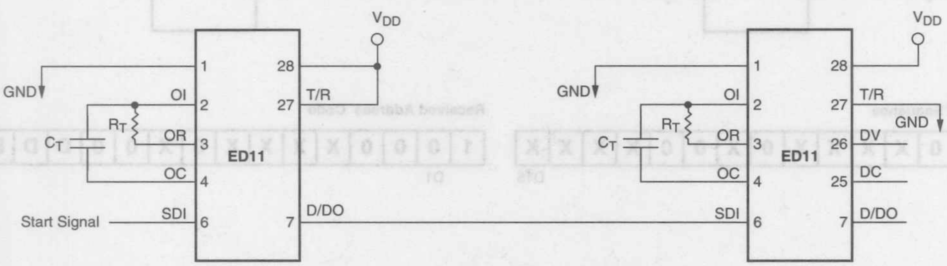
Transmitted Bit Sequence

D1														D15
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Received Address Code

D1														D15
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X

ED11 to ED11



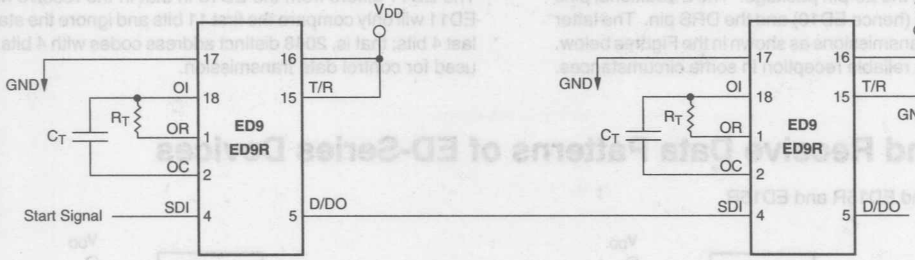
Transmitted Bit Sequence

D1														D15
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Received Address Code

D1														D15
1	X	X	X	X	X	X	X	X	X	X	D	D	D	D

ED9 to ED9 and ED9R to ED9R



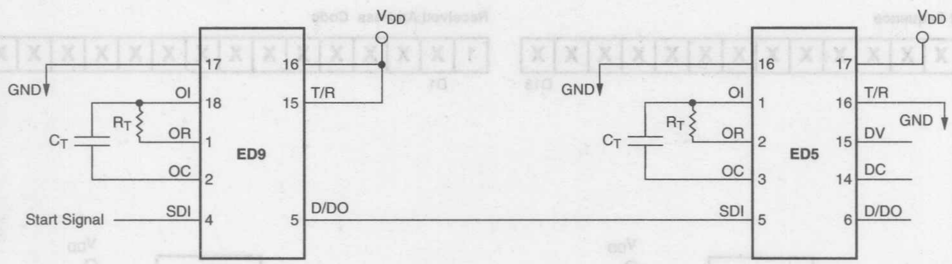
Transmitted Bit Sequence

D1														D15
1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

Received Address Code

D1														D15
1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

ED9 to ED5



Transmitted Bit Sequence

D1														D15
1	0	0	0	X	X	X	X	0	X	0	0	X	X	X	X

Received Address Code

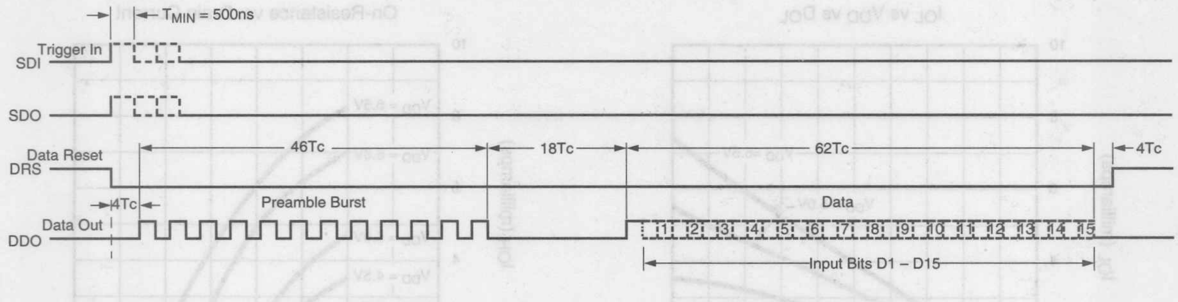
D1														D15
1	0	0	0	X	X	X	X	0	X	0	0	D	D	D	D

Notes:

Bit Sequence Code Format
- X = Programmable
- 0 = Hardwired Internally Zero
- 1 = Hardwired Internally One
- D = Don't Care in Receive Mode

When unused, the DV, DC, DRS and SDO pins should be left floating and **must not** be tied to either a power supply or to ground.

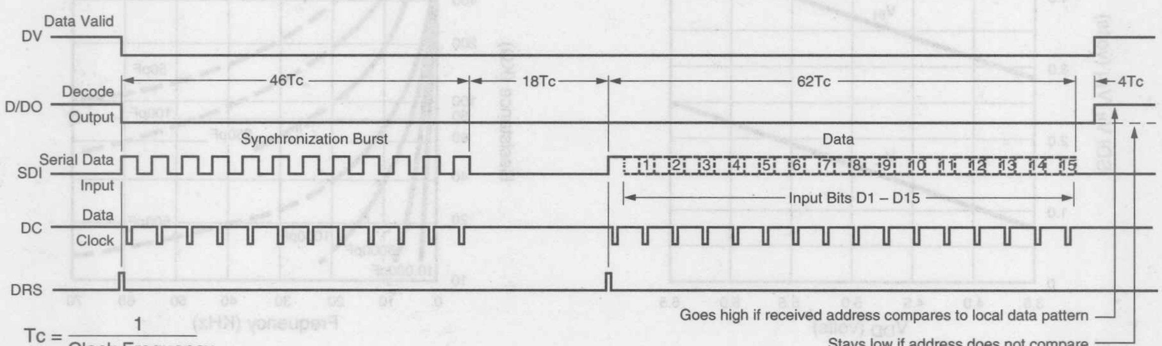
Timing Diagram – Transmit Mode



Total Time Required for Transmission of One Sequence = (DRS – 4Tc) =130Tc

$$Tc = \frac{1}{\text{Clock Frequency}}$$

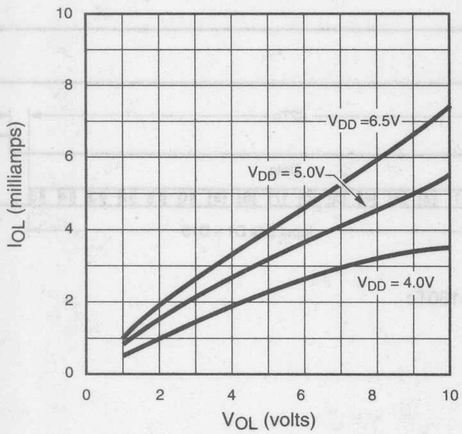
Timing Diagram – Receive Mode



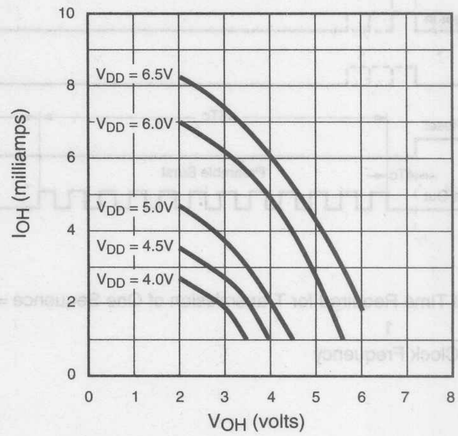
$$Tc = \frac{1}{\text{Clock Frequency}}$$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

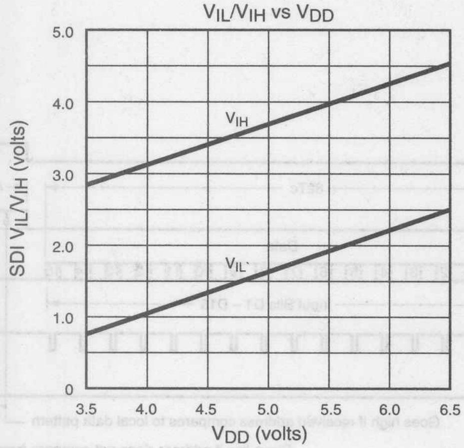
I_{OL} vs V_{DD} vs D_{OL}



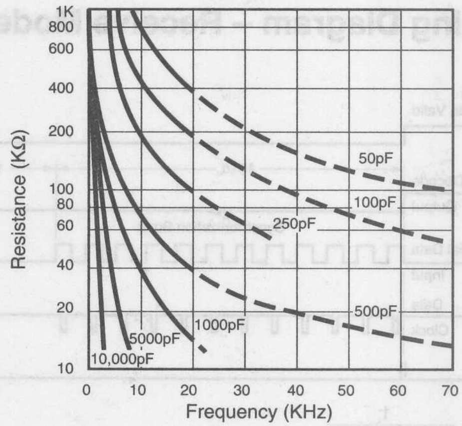
On-Resistance vs. Drain Current



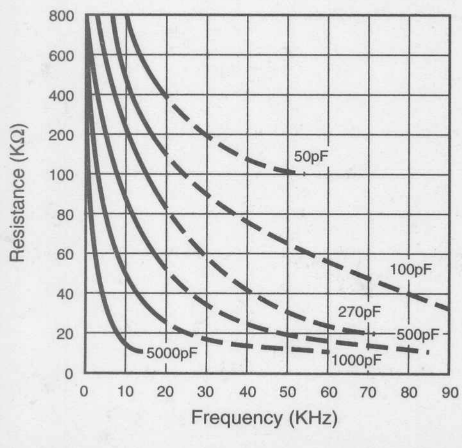
SDI Input
V_{IL}/V_{IH} vs V_{DD}



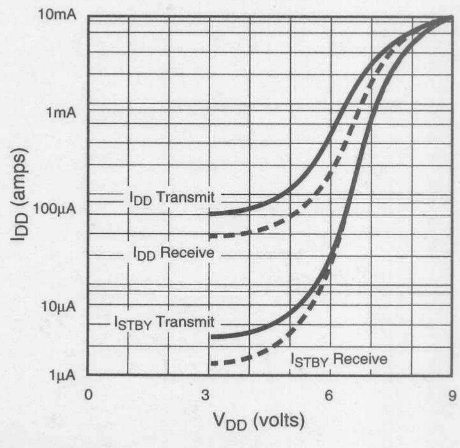
Resistance vs Oscillator Frequency – ED's



Resistance vs Oscillator Frequency – ED9R, ED15R



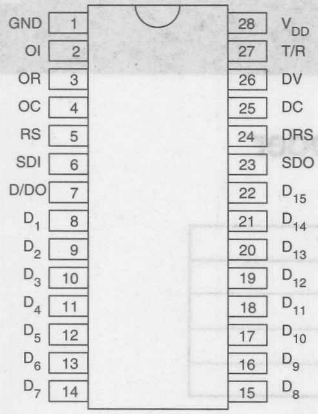
I_{DD} vs V_{DD}



Note: Operation is not guaranteed if the oscillation frequency is higher than 20KHz

Pin Configuration

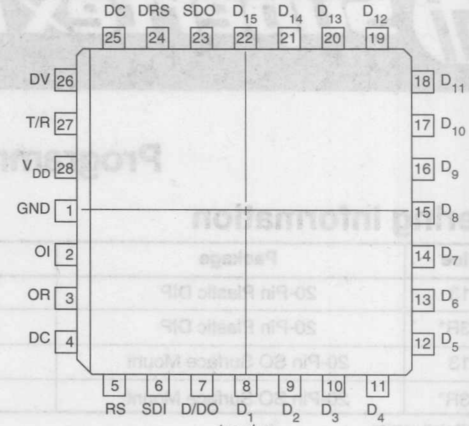
ED11, ED15 and ED15R



top view

28-pin DIP

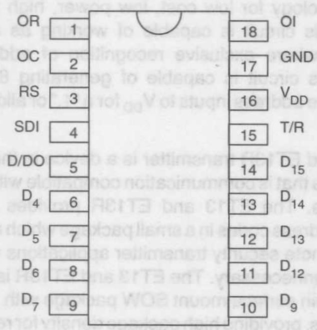
ED15 and ED15R



top view

28-pin J-lead Package

ED9 and ED9R



top view

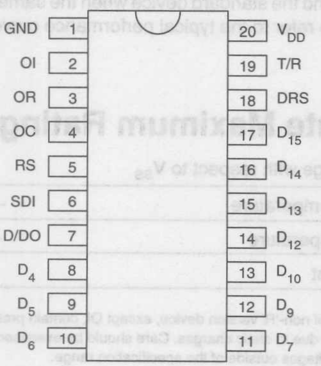
18-pin DIP

ED5

top view

18-pin DIP

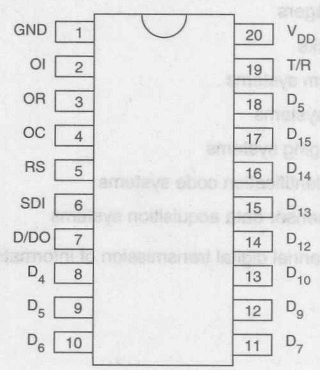
ED9 and ED9R



top view

20-pin DIP/SOW 20

ED10



top view

20-pin DIP/SOW 20

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Programmable Encoder

Ordering Information

Device	Package	Order Number
ET13	20-Pin Plastic DIP	ET13P
ET13R*	20-Pin Plastic DIP	ET13RP
ET13	20-Pin SO Surface Mount	ET13WG
ET13R*	20-Pin SO Surface Mount	ET13RWG

* Gate-protected version.

Features

- High density transmit only ED device
- 13 address bits (8192 addresses)
- Manchester phase encoding
- Transmitter compatible with ED15 series
- Schmitt Trigger input for excellent noise reduction
- Built-in oscillator using non-critical RC components
- Zener diode to regulate the power supply
- Low power, high noise immunity
- 20-pin surface mount SO package
- Automatic preamble generation
- Ruggedized device available

Applications

- Smoke and fire alarm systems
- Pocket pagers
- Digital locks
- Theft alarm systems
- Security systems
- Digital paging systems
- Special identification code systems
- Remote sensor data acquisition systems
- Single channel digital transmission of information

General Information

The ET13 and ET13R is a single monolithic chip using metal gate CMOS technology for low cost, low power, high yield and high reliability. This circuit is capable of working as an encoder in applications where exclusive recognition of address codes is required. This circuit is capable of generating 8192 codes by connecting the address inputs to V_{DD} for a "1," or allowed to float for a "0."

The ET13 and ET13R transmitter is a device in the Supertex ED series of parts that is communication compatible with any other ED series device. The ET13 and ET13R provides the maximum number of address codes in a small package which makes it ideally suited for remote security transmitter applications where receiver operation is unnecessary. The ET13 and ET13R is also available in a new 20-pin surface mount SOW package with .050-inch pitch gullwing leads, providing high package density for remote transmitter applications.

'R' version products are ruggedized to provide greater protection against ESD damage caused by improper handling. These devices are gate-protected and meet the 2000V ESD ratings of EIA standards. The oscillation frequency is also different between the "R" version and the standard device when the same RC network is used. Please refer to the typical performance curves for details.

Absolute Maximum Ratings

Supply Voltage with respect to V_{SS}	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°
Zener Current	100mA

Note: All inputs of non-'R' version device, except OI, contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range.

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GND = 0.0V; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	GND- 0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for ST
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, D1-D15
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} -1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0		I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{OUT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GND all inputs floating

Notes :

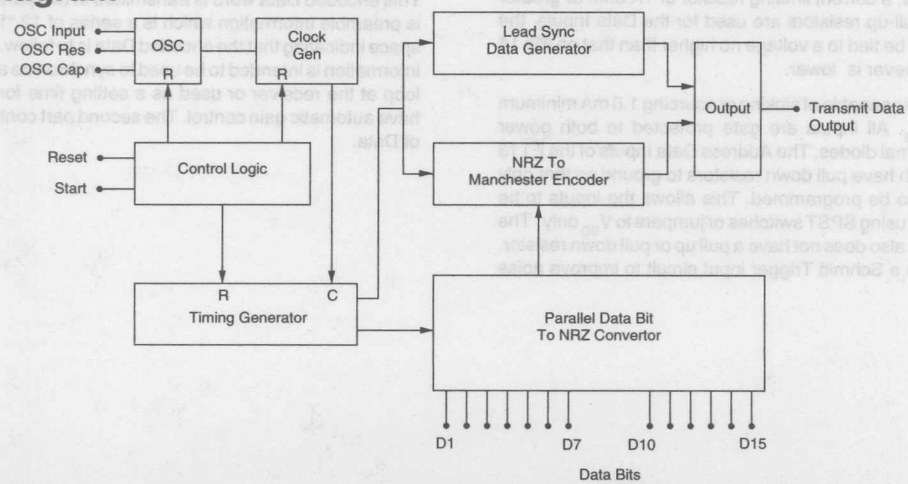
1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.
2. This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
f_c	Clock Frequency	0		20	kHz	R = 150k, C = 100pF; Clock Period (t_c) = 1/f_c
t_{st}	Start Pulse Width	500			ns	
T_{DO}	TDO Delay from SDI		5		µs	
t_{WORD}	Full Cycle Word Length		130t_c		sec	

Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Block Diagram



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Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (RT), and the timing capacitor (CT). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. NOTE: This pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
RS	Reset Input	This input pin may be used to override the data transmission cycle or to inhibit an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or it may be driven as an input, or an external capacitor (100pF) to V_{DD} may be added for power-up reset. The Reset function is activated when this input is connected to V_{DD}.
ST	Start	Start input is used to start the oscillator which enables the transmission of encoded word.
TDO	Transmit Data Output	This pin is the encoded sequence data output.
D1-D15	Data Bit Inputs	In the ED series devices, these inputs provide parallel input data to be sequentially transmitted. The 20-pin ET13 has some pins omitted and, hence, these data positions will have logical zeros transmitted.
V_{DD}	V_{DD}	Positive Supply Potential: This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Operation

General

The ET13 and ET13R is a programmable transmitter, encoding 13 data bits into a serial Manchester code bit stream.

The ET13 and ET13R contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ±5%, or from a regulated power supply in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull-up resistors are used for the Data Inputs, the resistors should be tied to a voltage no higher than that on Pin 14 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0 mA minimum at 1.0 volts V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The Address Data Inputs of the ET13 and ET13R each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The Start/Data Input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger input circuit to improve noise rejection.

Function

The ET13 and ET13R functions as an encoder, sampling the 13 Data Input pins' digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded) and presenting it to the TDO pin for transmission (usually to an ED device used as the decoder circuit). The encoder will transmit the serial data each time the Start (ST) input is activated.

This encoded Data word is transmitted in two parts. The first part is preamble information which is a series of 12 "1's" and then a space indicating that the encoded Data is to follow. This preamble information is intended to be used to synchronize a phase locked-loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 13 bits of Data.

Transmit and Receive Data Patterns of ED-Series Devices

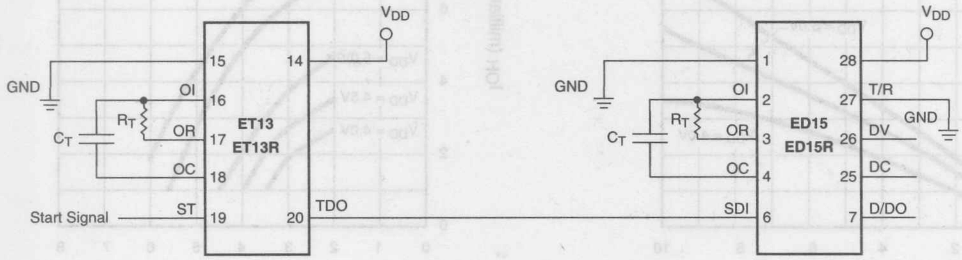
Note: Bit Sequence Code Format

x = Programmable

0 = Hardwired Internally Zero

1 = Hardwired Internally One

ET13 to ED15 and ET13R to ED15R



Transmitted Bit Sequence

1	X	X	X	X	X	X	X	0	0	X	X	X	X	X	X

D1 … D15

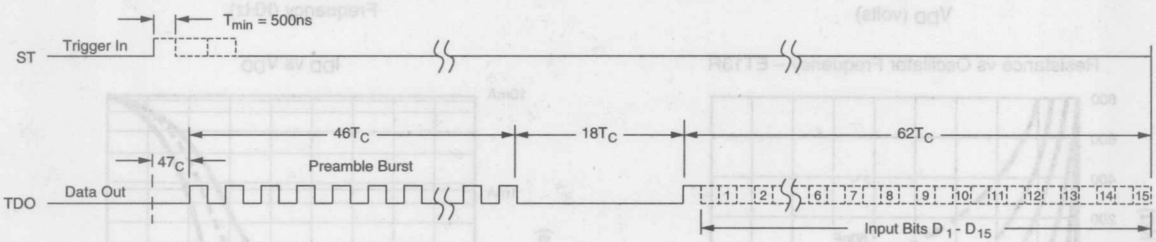
Received Address Code

1	X	X	X	X	X	X	X	0	0	X	X	X	X	X	X

D1 … D15

Timing Diagram – Transmit

Timing Diagram – Transmit

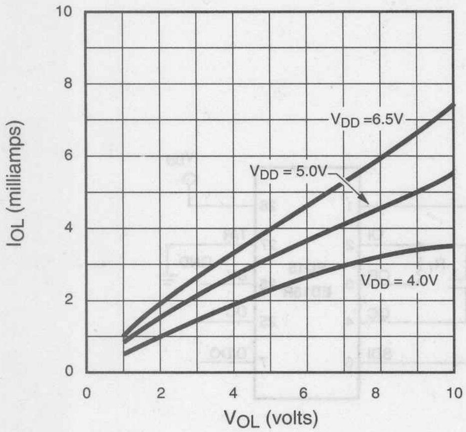


Total Time Required for Transmission of One Sequence = $130T_C$

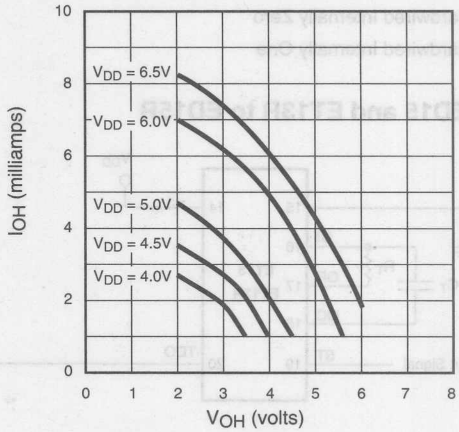
$$T_C = \frac{1}{\text{CLOCK FREQUENCY}}$$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

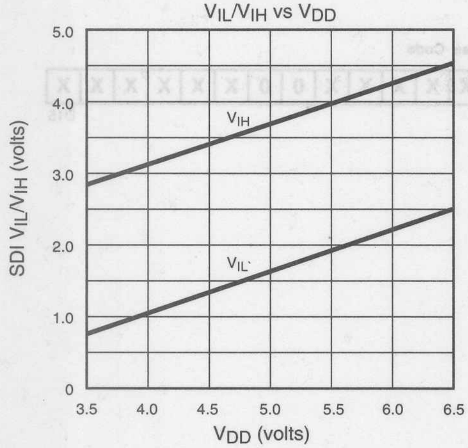
I_{OL} vs V_{DD} vs D_{OL}



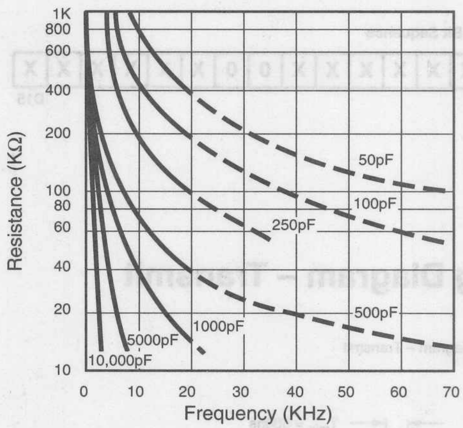
On-Resistance vs. Drain Current



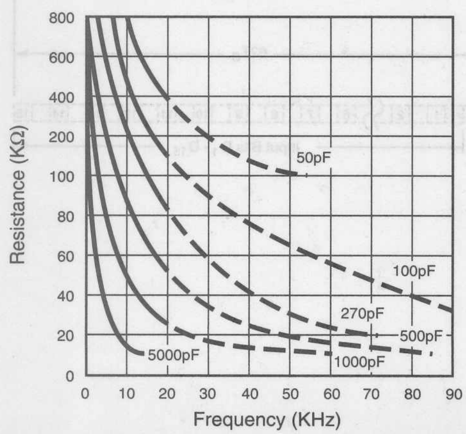
SDI Input
V_{IL}/V_{IH} vs V_{DD}



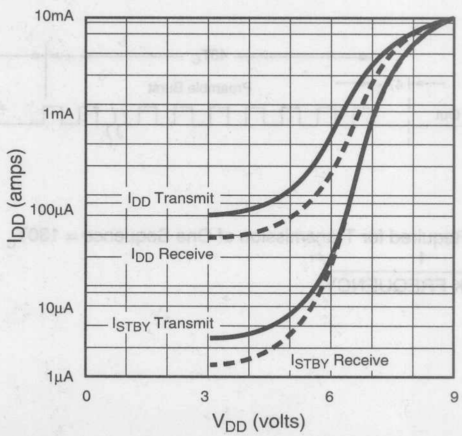
Resistance vs Oscillator Frequency – ET13



Resistance vs Oscillator Frequency – ET13R

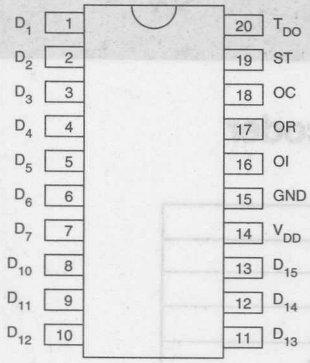


I_{DD} vs V_{DD}



Note: Operation is not guaranteed if the oscillation frequency is higher than 20KHz.

Pin Configuration



top view

20-pin DIP/SOW 20

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Supertex inc.

ET15
ET15R

Programmable Encoder

Ordering Information

Device	Package	Order No.
ET15	20-Pin Plastic DIP	ET15P
ET15R*	20-Pin Plastic DIP	ET15RP
ET15	20-Pin SO Surface Mount	ET15WG
ET15R*	20-Pin SO Surface Mount	ET15RWG

* Gate-protected version

Features

- High density transmit only ED device
- 12 address bits (4096 addresses)
- Manchester phase encoding
- Data reset (DRS) pin for multiple transmissions
- Transmitter compatible with ED15 series
- Schmitt Trigger input for excellent noise reduction
- Built-in oscillator using non-critical RC components
- Zener diode to regulate the power supply
- Low power, high noise immunity
- 20-pin surface mount SO package
- Automatic preamble generation
- Ruggedized devices available

Applications

- Smoke and fire alarm systems
- Pocket pagers
- Digital locks
- Theft alarm systems
- Security systems
- Digital paging systems
- Special identification code systems
- Remote sensor data acquisition systems
- Single-channel digital transmission of information

General Information

The ET15 and ET15R is a single monolithic chip using metal gate CMOS technology for low cost, low power, high yield and high reliability. This circuit is capable of working as an encoder in applications where exclusive recognition of address codes is required. This circuit is capable of generating 4096 codes by connecting the address inputs to V_{DD} for a "1," or allowing them to float for a "0." The ET15 and ET15R permits multiple transmissions of data, improving the probability of valid reception in high-noise environments.

The ET15 and ET15R Transmitter is a device in the Supertex ED Series of parts that is communication-compatible with any other ED Series device. The ET15 and ET15R provides the maximum number of address codes in a small package which makes it ideally suited for remote security transmitter applications where receiver operation is unnecessary. The ET15 and ET15R is also available in a new 20-pin surface mount SOW package with .050-inch pitch gullwing leads, providing high package density for remote transmitter applications.

"R" version products are ruggedized to provide greater protection against ESD damage caused by improper handling. These devices are gate-protected and meet the 2000V ESD ratings of EIA standards.

Absolute Maximum Ratings

Supply Voltage with respect to V_{SS}	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

Note: All inputs of non-"R" version device, except OI, contain protection circuitry to prevent damage due to static charges. Care should be exercised to prevent application of voltages outside of the specification range.

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GND = 0.0V; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	GND- 0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for ST
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, D2-D15
V_{OH}	Output High Voltage	V_{DD} - 0.3				V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} -1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{OUT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GND all inputs floating

Notes:

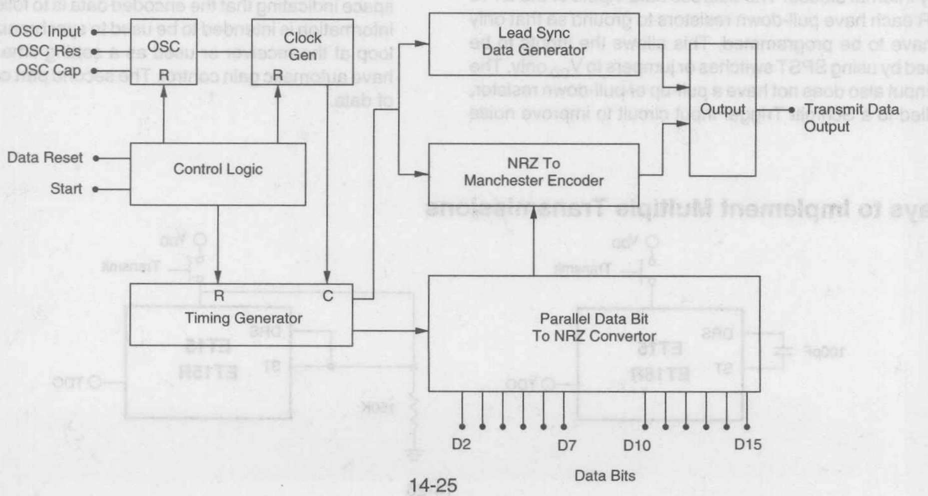
1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.
2. This parameter is periodically sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
f_C	Clock Frequency	0		15	kHz	R = 150k, C = 100pF; Clock Period (t_C) = 1/f_C
t_{ST}	Start Pulse Width	500			ns	
T_{DO}	TDO Delay from SDI		5		µs	
t_{WORD}	Full Cycle Word Length		130t_C		sec	

Note 1: Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Block Diagram



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Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (RT), and the timing capacitor (CT). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies and does so during normal oscillator operation.
OR	Oscillator Resistor	Provides phase feedback to the RC timing circuit through the connected timing resistor. NOTE: This pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
DRS	Data Reset	This output goes high after a valid data transmission (see Timing Diagram). This may be used to either indicate a completed transmission or to restart transmission.
ST	Start	Start input is used to start the oscillator which enables the transmission of encoded word.
TDO	Transmit Data Output	This pin is the encoded sequence data output.
D2-D15	Data Bit Inputs	In the ED series devices, these inputs provide parallel input data to be sequentially transmitted. The 20-pin ET15 has some pins omitted and, hence, these data positions will have logical zeros transmitted.
V_{DD}	V_{DD}	Positive Supply Potential: This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Operation

General

The ET15 and ET15R is a programmable transmitter, encoding 12 data bits into a serial Manchester code bit stream.

The ET15 and ET15R contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ±5%, or from a regulated power supply in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull-up resistors are used for the data inputs, the resistors should be tied to a voltage no higher than that on pin 14 or 6 volts, whichever is lower.

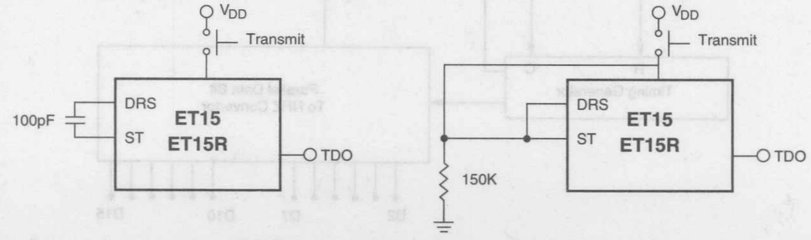
Output drivers are capable of sinking or sourcing 1.0 mA minimum at 1.0 volts V_{DS}. All inputs are gate protected to both power supplies by internal diodes. The address data inputs of the ET15 and ET15R each have pull-down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The start/data input also does not have a pull-up or pull-down resistor, but is applied to a Schmitt Trigger input circuit to improve noise rejection.

Function

The ET15 and ET15R functions as an encoder, sampling the 12 data input pins' digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (phase encoded) and presenting it to the TDO pin for transmission (usually to an ED device used as the decoder circuit). The encoder will transmit the serial data each time the start (ST) input is activated. For multiple transmissions of the preamble/encoded data, the DRS pin may be connected to the ST input, with the TRANSMIT function controlled by a push button switch in the V_{DD} line. (See diagrams below.) In high-noise environments, multiple transmissions can improve the probability of a valid received transmission.

This encoded data word is transmitted in two parts. The first part is preamble information which is a series of 12 "1s" and then a space indicating that the encoded data is to follow. This preamble information is intended to be used to synchronize a phase-locked loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 12 bits of data.

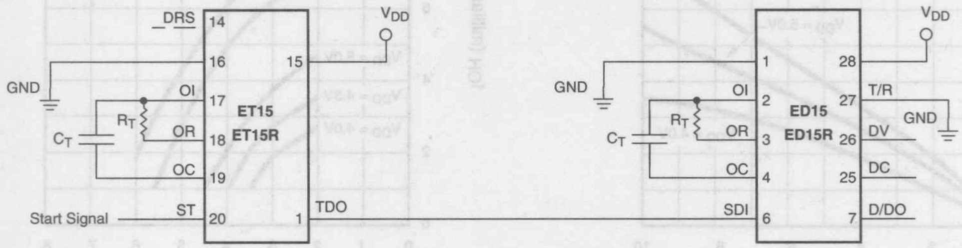
Two Ways to Implement Multiple Transmissions



Transmit and Receive Data Patterns of ED-Series Devices

Note: Bit Sequence Code Format
x = Programmable
0 = Hardwired Internally Zero
1 = Hardwired Internally One

ET15 to ED15 and ET15R to ED15R



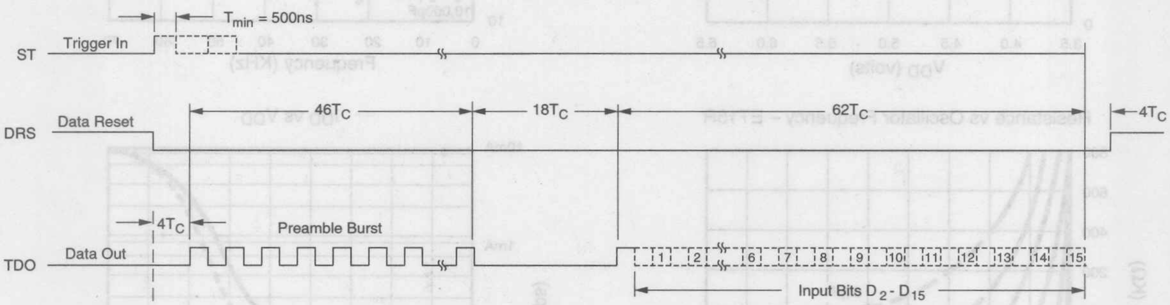
Transmitted Bit Sequence

D1															D15
1	0	X	X	X	X	X	X	0	0	X	X	X	X	X	X

Received Address Code

D1															D15
1	0	X	X	X	X	X	X	0	0	X	X	X	X	X	X

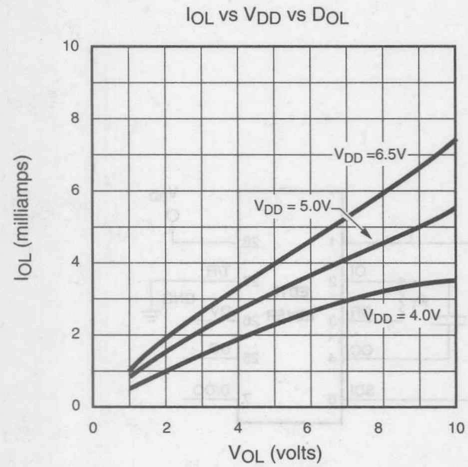
Timing Diagram – Transmit

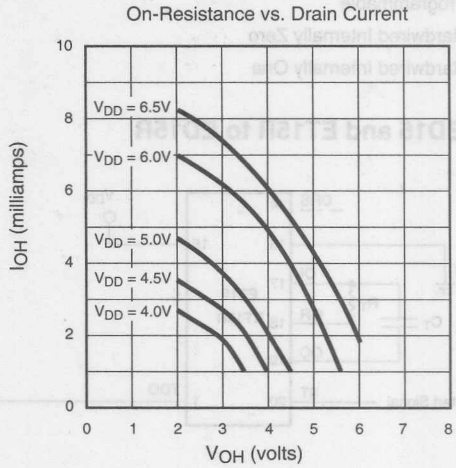


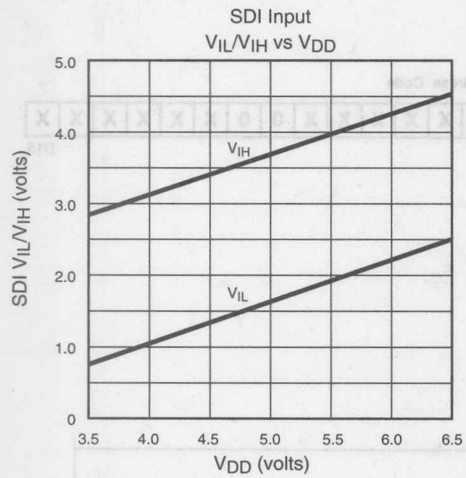
Total Time Required for Transmission of One Sequence = (DRS – $4T_C$) = $130T_C$

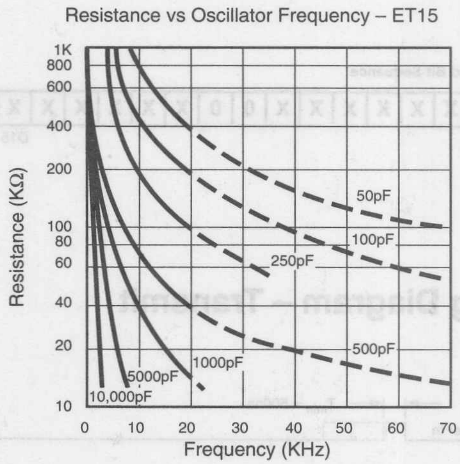
$$T_C = \frac{1}{\text{CLOCK FREQUENCY}}$$

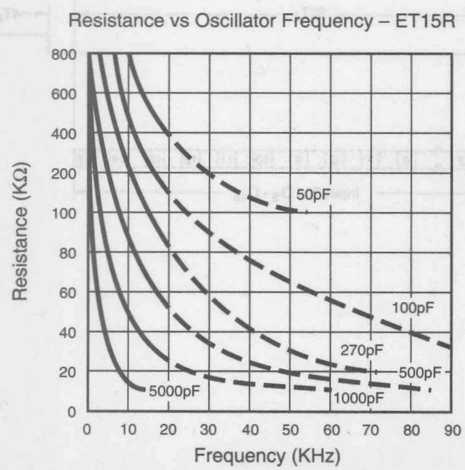
Typical Performance Curves (T_A = 25°C unless otherwise noted)

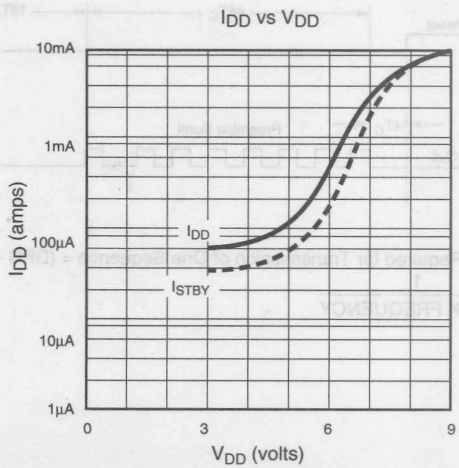






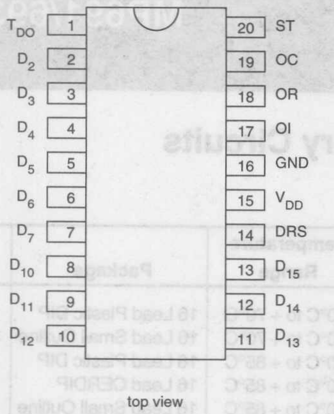






Note: Operation is not guaranteed if the oscillation frequency is higher than 20KHz.

Pin Configuration



20-pin DIP/SOW 20

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Supertex inc.

MP690/692/694
MP691/693/695

Microprocessor Supervisory Circuits

Ordering Information

Device	Temperature Range	Package	Order Number
MP690	0°C to + 70°C	8 Lead Plastic DIP	MP690P
	-40°C to + 85°C	8 Lead Plastic DIP	MP690MP
	-40°C to + 85°C	8 Lead CERDIP	MP690MD
	-55°C to +125°C	8 Lead CERDIP	RCMP690D
MP691	0°C to + 70°C	16 Lead Plastic DIP	MP691P
	0°C to + 70°C	16 Lead Wide SO	MP691WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP691MP
	-40°C to + 85°C	16 Lead CERDIP	MP691MD
	-40°C to + 85°C	16 Lead Wide SO	MP691MWG
	-55°C to +125°C	16 Lead CERDIP	RCMP691D
MP692	0°C to + 70°C	8 Lead Plastic DIP	MP692P
	-40°C to + 85°C	8 Lead Plastic DIP	MP692MP
	-40°C to + 85°C	8 Lead CERDIP	MP692MD
	-55°C to +125°C	8 Lead CERDIP	RCMP692D

Device	Temperature Range	Package	Order Number
MP693	0°C to + 70°C	16 Lead Plastic DIP	MP693P
	0°C to + 70°C	16 Lead Small Outline	MP693WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP693MP
	-40°C to + 85°C	16 Lead CERDIP	MP693MD
	-40°C to + 85°C	16 Lead Small Outline	MP693MWG
	-55°C to +125°C	16 Lead CERDIP	RCMP693D
MP694	0°C to + 70°C	8 Lead Plastic DIP	MP694P
	-40°C to + 85°C	8 Lead Plastic DIP	MP694MP
	-40°C to + 85°C	8 Lead CERDIP	MP694MD
	-55°C to +125°C	8 Lead CERDIP	RCMP694D
MP695	0°C to + 70°C	16 Lead Plastic DIP	MP695P
	0°C to + 70°C	16 Lead Small Outline	MP695WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP695MP
	-40°C to + 85°C	16 Lead CERDIP	MP695MD
	-40°C to + 85°C	16 Lead Small Outline	MP695MWG
	-55°C to +125°C	16 Lead CERDIP	RCMP695D

Features

- ☐ Precision voltage monitor:
  4.65V in MP690, MP691, MP694, and MP695
  4.40V in MP692 and MP693
- ☐ Power OK/reset time delay – 50, 200ms, or adjustable
- ☐ Watchdog timer –100ms, 1.6 sec, or adjustable
- ☐ Minimum component count
- ☐ 1µA standby current
- ☐ Battery backup power switching
- ☐ Onboard gating of chip enable signals
- ☐ Voltage monitor for power fail or low battery warning

Applications

- ☐ Computers
- ☐ Controllers
- ☐ Intelligent instruments
- ☐ Automotive systems
- ☐ Critical µP power monitoring

General Description

The MP690 Family of supervisory circuits reduces the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include µP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MP690 family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

The MP690, MP692, and MP694 are supplied in 8-pin packages and provide four functions:

1) A Reset output during power-up, power-down, and brown out conditions.
2) Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
4) A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MP691, MP693 and MP695 are supplied in 16-pin packages and perform all MP690/692 functions, plus:

1) Write protection of CMOS RAM or EEPROM.
2) Adjustable reset and watchdog timeout periods.
3) Separate outputs for indicating a watchdog timeout, backup battery switchover, and low V_{CC}.

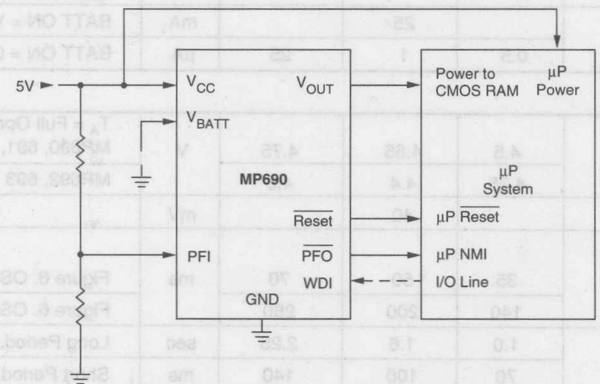
Absolute Maximum Ratings

Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
V_{BATT}	-0.3V to 6.0V
All other Inputs (Note 1)	-0.3V to (Vout +0.5V)
Input Current	
V_{CC}	200mA
V_{BATT}	50mA
GND	20mA
Output Current	
V_{OUT} short circuit protected	
All Other Outputs	20mA
Rate-of-Rise, V_{BATT}, V_{CC}	100V/µs

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Power Dissipation	
8 Pin Plastic DIP	
(Derate 5mW/°C above +70°C)	400mW
8 Pin CERDIP	
(Derate 8mW/°C above +85°C)	500mW
16 Pin Plastic DIP	
(Derate 7mW/°C above +70°C)	600mW
16 Pin Small Outline	
(Derate 7mW/°C above +70°C)	600mW
16 Pin CERDIP	
(Derate 10mW/°C above +85°C)	600mW
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

Typical Operating Circuit



MP690 Typical Application

Electrical Characteristics

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1 and 2)

Parameter	Min	Typ	Max	Unit	Conditions
BATTERY BACKUP SWITCHING					
Operating Voltage Range					
MP690, 691, 694, 695 V_{CC}	4.75		5.5	V	
MP690, 691, 694, 695 V_{BATT}	2.0		4.25	V	
MP692, 693 V_{CC}	4.5		5.5	V	
MP692, 693 V_{BATT}	2.0		4.0	V	
V_{OUT} Output Voltage	V_{CC} - 0.3	V_{CC} - 0.1		V	I_{OUT} = 1mA
	V_{CC} - 0.5	V_{CC} - 0.25			I_{OUT} = 50mA
V_{OUT} in Battery Backup Mode		V_{BATT} - 0.1	V_{BATT} - 0.02	V	I_{OUT} = 100µA, V_{CC}< V_{BATT} - 0.2V
Supply Current (excludes I_{OUT})		2	5	mA	I_{OUT} = 1mA
		3.5	15		I_{OUT} = 50mA
Supply Current in Battery Backup Mode		0.6		µA	V_{CC} = 0V, V_{BATT} = 2.8V
Battery Standby Current (+ = Discharge, - = Charge)	-0.1		+0.02	µA	5.5V > V_{CC} > V_{BATT} + 0.2V, T_A = 25°C
	-1.0		+0.02		T_A = Full Operating Range
Battery Switchover Threshold V_{CC} - V_{BATT}		70		mV	Power Up
		50			Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.4	V	I_{SINK} = 3.2mA
BATT ON Output Short Circuit Current		25		mA	BATT ON = V_{OUT}
	0.5	1	25	µA	BATT ON = 0V
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	4.5	4.65	4.75	V	T_A = Full Operating Range MP690, 691, 694, 695
	4.25	4.4	4.5		MP692, 693
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
MP690/691/692/693	35	50	70	ms	Figure 6. OSC SEL High, V_{CC} = 5V
MP694/695	140	200	280		Figure 6. OSC SEL High, V_{CC} = 5V
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	sec	Long Period, V_{CC} = 5V
	70	100	140	ms	Short Period, V_{CC} = 5V
Watchdog Timeout Period, External Clock	3840		4097	Clock	Long Period
	768		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	200			ns	V_{IL} = 0.4, V_{IH} = 3.5V
$\overline{\text{RESET}}$ and $\overline{\text{LOW LINE}}$ Output Voltage			0.4	V	I_{SINK} = 1.6mA, V_{CC} = 4.25V
	3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
RESET and $\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 1.6µA
	3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
Output Short Circuit Current	1	3	25	µA	$\overline{\text{RESET}}$, RESET, $\overline{\text{WDO}}$, $\overline{\text{LOWLINE}}$
WDI Input Threshold					
Logic Low			0.8	V	V_{CC} = 5V[2]
Logic High	3.5				
WDI Input current		20	50	µA	WDI = V_{OUT}
	-50	-15		µA	WDI = 0V

Electrical Characteristics (continued)

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1 and 2)

Parameter	Min	Typ	Max	Unit	Conditions
POWER FAIL DETECTOR					
PFI Input Threshold	1.2	1.3	1.4	V	V_{CC} = 5V, T_A = Full
PFI Input Current		±0.01	±25	nA	0 To V_{CC} - 0.7V
$\overline{\text{PFO}}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA
	3.5				I_{SOURCE} = 1µA
PFO Short Circuit Source Current	1	3	25	µA	PFI = 0V, $\overline{\text{PFO}}$ = 0V
CHIP ENABLE GATING					
$\overline{\text{CE}}$ IN Thresholds			0.8	V	V_{IL}
	3.0				V_{IH}
$\overline{\text{CE}}$ IN Pullup Current		3		µA	
CE OUT Output Voltage			0.4	V	I_{SINK} = 3.2mA
	V_{out} -1.5				I_{SOURCE} = 3.0mA
	V_{out} -0.05				I_{SOURCE} = 1µA, V_{CC} = 0V
CE Propagation Delay		50	200	ns	V_{CC} = 5V
OSCILLATOR					
OSC IN Input Current		±2		µA	
OSC SEL Input Pullup Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0V, C_{OSC} = 47pF

Notes:

1. The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.
2. WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

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Pin Description

Name	Pin		Function
	MP690/692/694	MP691/693/695	
V_{CC}	2	3	The +5V input.
V_{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	1	2	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	3	4	0V ground reference for all signals.
$\overline{\text{RESET}}$	7	15	$\overline{\text{RESET}}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MP690/691/694/695, and 4.4V for the MP692 and MP693. $\overline{\text{RESET}}$ remains low for 50ms after V_{CC} returns to 5V (except 200ms in MP694/695). $\overline{\text{RESET}}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{\text{RESET}}$ pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and $\overline{\text{WDO}}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND when not used. See Figure 1.
$\overline{\text{PFO}}$	5	10	$\overline{\text{PFO}}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{\text{PFO}}$ goes low when V_{CC} is below V_{BATT}.
$\overline{\text{CE}}$ IN		13	The input to the $\overline{\text{CE}}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{\text{CE}}$ OUT		12	$\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and V_{CC} is above the reset threshold (4.65V for MP691and MP695, 4.4V for MP693). See Figure 6.
BATT ON		5	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 100mA rating of V_{OUT}.
$\overline{\text{LOW LINE}}$		6	$\overline{\text{LOW LINE}}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET		16	RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.
OSC SEL		8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3µA internal pullup. See Table 1.
OSC IN		7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven low. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is high, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{\text{WDO}}$		14	The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{\text{WDO}}$ remains high. $\overline{\text{WDO}}$ also goes high when $\overline{\text{LOW LINE}}$ goes low.

Typical Applications

MP691, MP693 and MP695

A typical connection for the MP 691/693/695 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 100mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 500Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1μA maximum when V_{CC} is between 0V and V_{BATT} - 700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor's $\overline{\text{RESET}}$ line low when V_{CC} is below 4.65V (4.4V for MP693). An internal monostable holds $\overline{\text{RESET}}$ low for 50ms* after V_{CC} rises above 4.65V (4.4V for MP693). This prevents repeated toggling of $\overline{\text{RESET}}$ even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The MP690 Family power-up $\overline{\text{RESET}}$ pulse lasts 50ms* to allow for this oscillator start-up time. The manual reset switch and the 0.1μF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MP691/693/695 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the power fail input (PFI). When the voltage at PFI falls below 1.3V, the power fail output ($\overline{\text{PFO}}$) drives the processor's NMI input low. If a power fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} falls from 4.8V to 4.65V to save data into RAM. An earlier power fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MP691/693/695 $\overline{\text{CE}}$ OUT line drives the Chip Select inputs of the CMOS RAM, $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN as long as V_{CC} is above the 4.65V (4.4V for MP693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{\text{CE}}$ OUT goes high, independent of the logic level at $\overline{\text{CE}}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The $\overline{\text{LOW LINE}}$ output goes low when V_{CC} falls below 4.65V (4.4V for MP693).

* 200ms for MP695

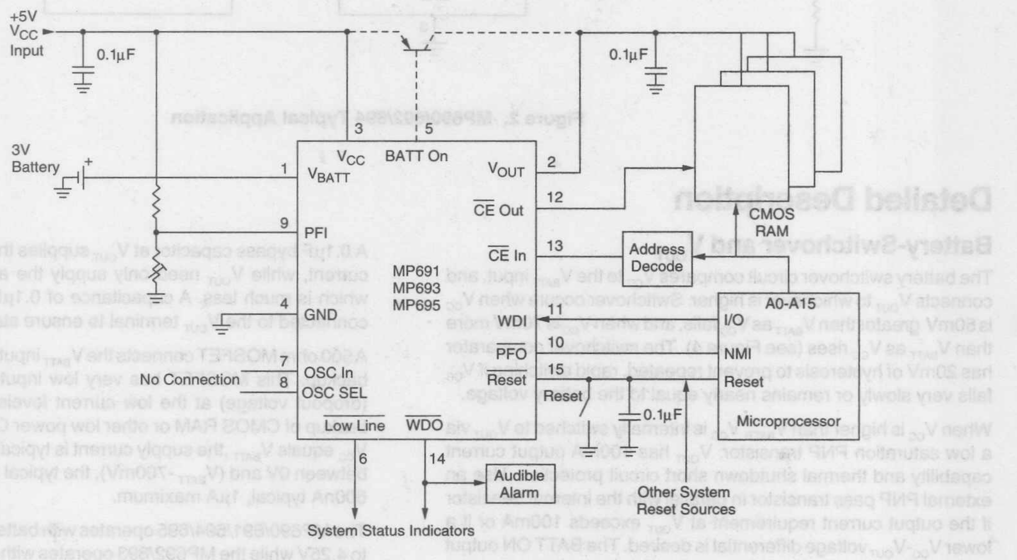


Figure 1. MP691/693/695 Typical Application

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MP691/693 will issue a 50ms* $\overline{\text{RESET}}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low, it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MP690, MP692 and MP694

The 8-pin MP690, MP692 and MP694 have most of the features of the MP691, MP693 and MP695. Figure 2 shows the MP690/692/694 in a typical application. Operation is much the same as with the MP691/693/695 (Figure 1) but in this case the Power Fail Input (PFI) monitors the unregulated input to the 7805 regulator. The MP690/694 $\overline{\text{RESET}}$ output goes low when V_{CC} falls below 4.65V. The $\overline{\text{RESET}}$ output of the MP692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 100mA. The MP690/692/694 does not have a BATT ON output to drive an external transistor. The MP690/692/694 also does not include chip enable gating circuitry that is available on the MP691/693/695. In many systems though, $\overline{\text{CE}}$ gating is not needed since a low input to the microprocessor $\overline{\text{RESET}}$ line prevents the processor from writing to RAM during power-up and power-down transients.

The MP690/692/694 watchdog timer has a fixed 1.6 second timeout period. If WDI remains either low or high for more than 1.6 seconds, a $\overline{\text{RESET}}$ pulse is sent to the microprocessor. The watchdog timer is disabled if WDI is left floating.

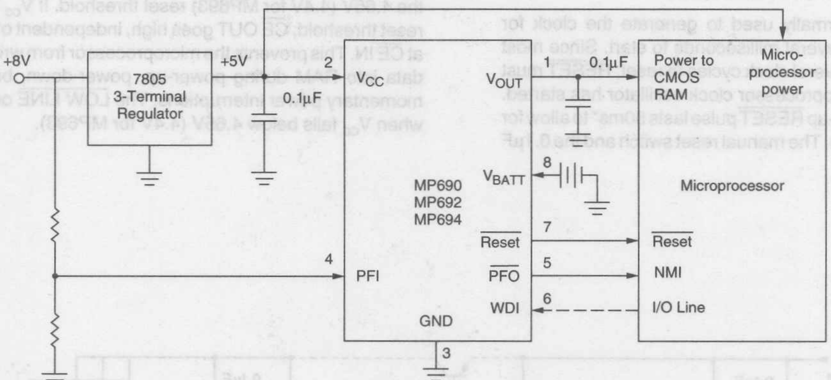


Figure 2. MP690/692/694 Typical Application

Detailed Description

Battery-Switchover and V_{OUT}

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 100mA output current capability and thermal shutdown short circuit protection. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 100mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MP691/693/695 only) can directly drive the base of the external transistor.

It should be noted that the MP690/691/692/693/694/695 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns.

A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 500 ohm MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT}, the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV), the typical supply current is only 600nA typical, 1µA maximum.

The MP690/691/694/695 operates with battery voltages from 2.0V to 4.25V while the MP692/693 operates with battery voltages from 2.0V to 4.0V. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small charging current of typically 10nA (5µA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharging current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (5µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the status of the input and output in the low power battery backup mode.

Reset Output

$\overline{\text{RESET}}$ is an active low output which goes low whenever V_{CC} falls below 4.5V (MP690/691/694/695) or 4.25V (MP692/693). It will remain low until V_{CC} rises above 4.75V (MP 690/691/694/695) or 4.5V (MP692/693) for 50 milliseconds.* (See Figures 5 and 6.)

The guaranteed minimum and maximum thresholds of the MP 690/691/694/695 are 4.5V and 4.75V, while the guaranteed thresholds of the MP692/693 are 4.25V and 4.5V. The MP690/691/694/695 is compatible with 5V supplies with a +10%, -5% tolerance while the MP692/693 is compatible with 5V ±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MP690/691/694/695, and 4.4V in the MP692/693.

The response time of the reset voltage comparator is about 100µs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{\text{RESET}}$ output.

$\overline{\text{RESET}}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{RESET}}$ has an internal 3µA pullup and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{\text{CE}}$ Gating and RAM Write Protection

The MP691, MP693 and MP695 use two pins to control the $\overline{\text{Chip Enable}}$ or $\overline{\text{Write}}$ inputs of CMOS RAMs. When V_{CC} is +5V, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max), an internal gate forces $\overline{\text{CE}}$ OUT high, independent of $\overline{\text{CE}}$ IN. The MP693 $\overline{\text{CE}}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{\text{CE}}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{\text{CE}}$ OUT typically drives the $\overline{\text{CE}}$, $\overline{\text{CS}}$, or $\overline{\text{Write}}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{\text{CE}}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{\text{CE}}$ OUT is too long, connect $\overline{\text{CE}}$ IN to GND and use the resulting $\overline{\text{CE}}$ OUT to control a high speed external logic gate. A second alternative is to AND the $\overline{\text{LOW LINE}}$ output with the $\overline{\text{CE}}$ or $\overline{\text{WR}}$ signal. An external logic gate and the $\overline{\text{RESET}}$ output of the MAX690/692/964 can also be used for CMOS RAM write protection.

* 200ms for MP694 and MP695

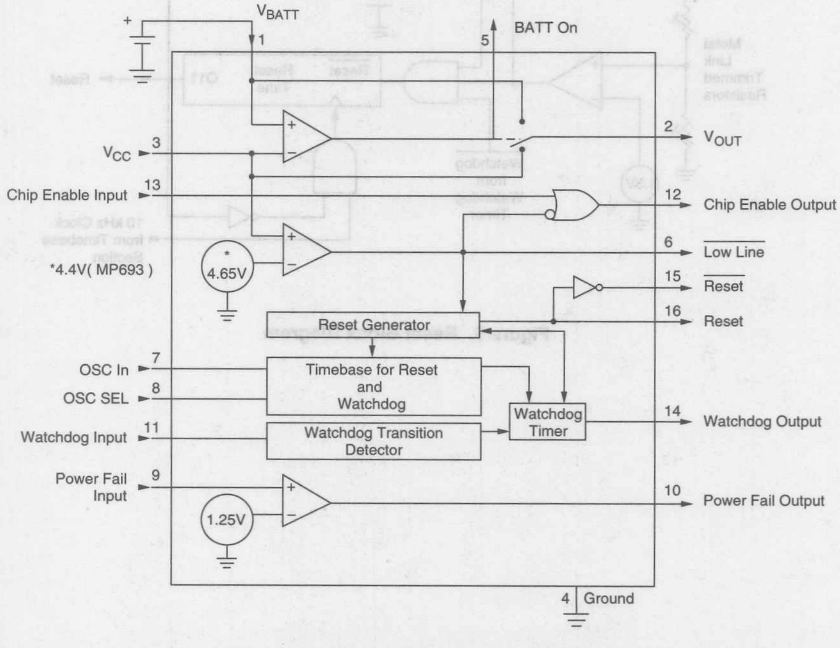


Figure 3. MP 691/693/695 Block Diagram

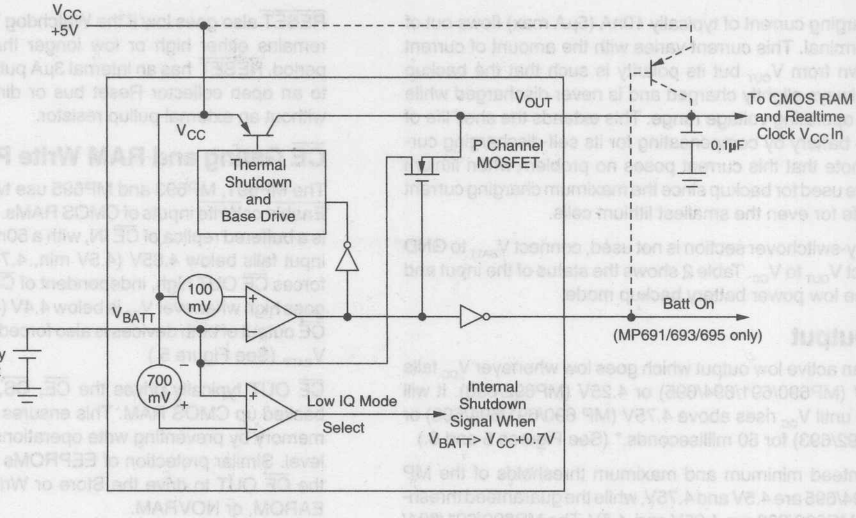


Figure 4. Battery–Switchover Block Diagram

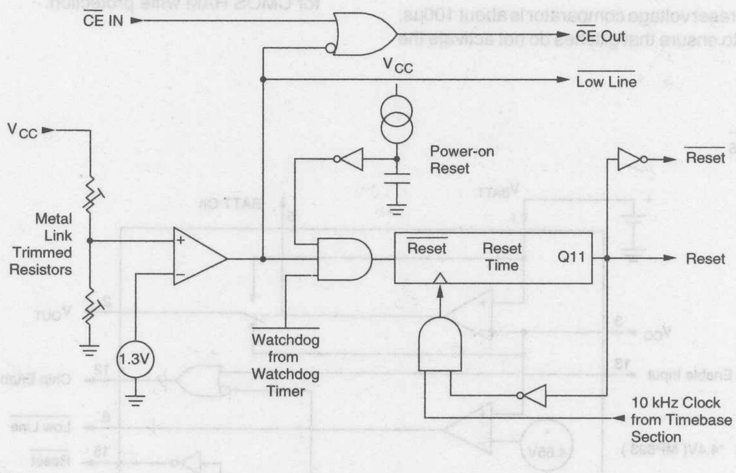
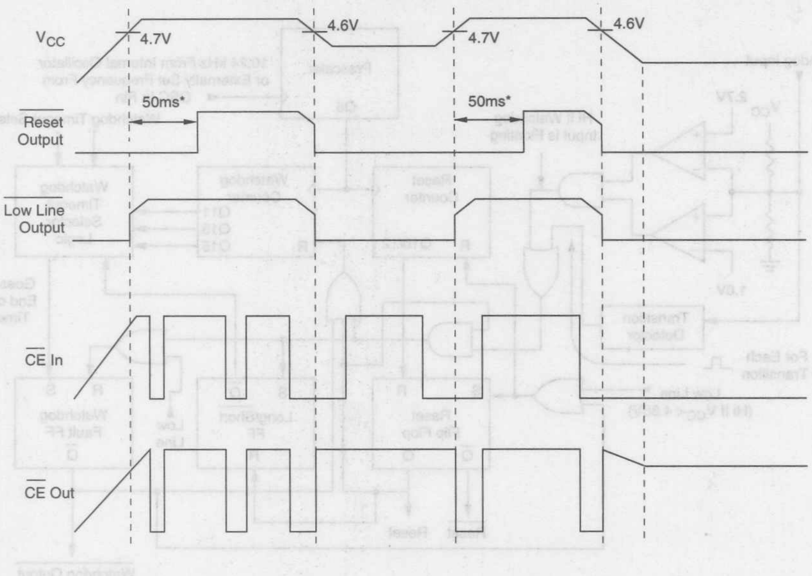


Figure 5. Reset Block Diagram



*200ms for MP694 and MP695

Figure 6. Reset Timing

1.3V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output ($\overline{\text{PFO}}$) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the +5V supply falls below 4.75V. $\overline{\text{PFO}}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the $\overline{\text{RESET}}$ output goes low (4.5V for MP692/693).

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{\text{PFO}}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 millisecond* $\overline{\text{RESET}}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MP691/693/695 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output ($\overline{\text{WDO}}$, MP691/693/695 only) goes low if the watchdog timer "times out," and it remains low until set high by the next transition on the watchdog input. $\overline{\text{WDO}}$ is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6 seconds and the reset pulse width is fixed at 50ms* on the 8-pin MP690, MP692 and MP694. The MP691, MP693 and MP695 allow these times to be adjusted per Table 1. Figure 8 shows various oscillator configurations.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset, the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period to 70ms.

* 200ms for MP694 and MP695

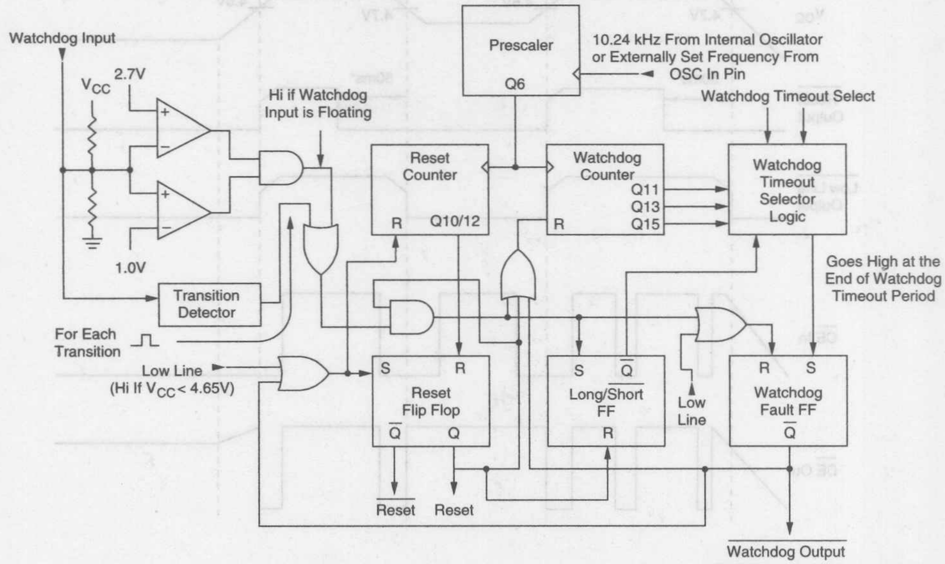


Figure 7. Watchdog Timer Block Diagram

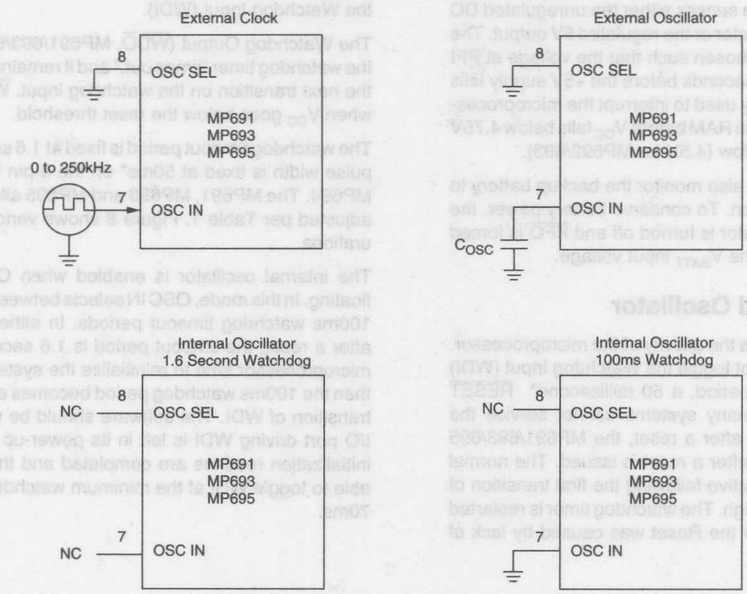


Figure 8. Oscillator Circuits

Table 1. MP691, MP693 and MP695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period	
		Normal	Immediately After Reset	MP691/693	MP695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor	$\frac{400ms}{47pF} \times C$	$\frac{1.6\ sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$	$\frac{800ms}{47pF} \times C$
High/Floating	Low	100ms	1.6 sec	50ms	200ms
High/Floating	High / Floating	1.6 sec	1.6 sec	50ms	200ms

Notes:
1. The MP690 watchdog timeout period is fixed at 1.6 seconds nominal; the MP690 Reset pulse width is fixed at 50ms nominal.
2. When the MP691 OSC SEL pin is low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz.
   The nominal oscillator frequency with external capacitor is $F_{OSC}\,(Hz) = \frac{184{,}000}{C(pF)}$
3. See Electrical Characteristics Table for minimum and maximum timing values.

Application Hints

Other Uses of the Power Fail Detector

In Figure 9, the Power Fail Detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the Power Fail Detector is not as accurate as the onboard Reset voltage detector, a trimpot must be used to adjust the voltage detection threshold. Both the PFO and $\overline{RESET}$ outputs have high sink current capability and only 10µA of source current drive. This allows the two outputs to be connected directly to each other in a "wired or" fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use,even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 12. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 13). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MP690 from detecting that the microprocessor is no longer working. In most cases, a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01µF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 14 is used.

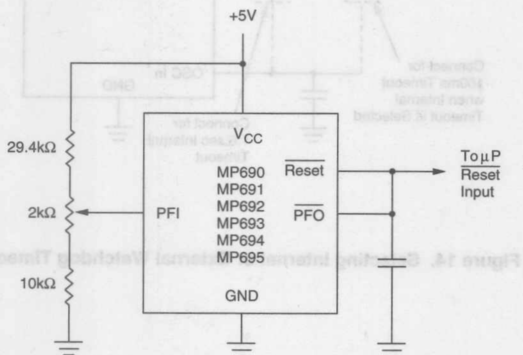


Figure 9. Externally Adjustable V_{CC} Reset Threshold

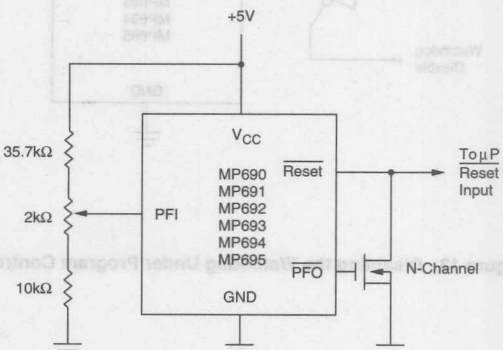


Figure 10. Reset on Overvoltage or Undervoltage

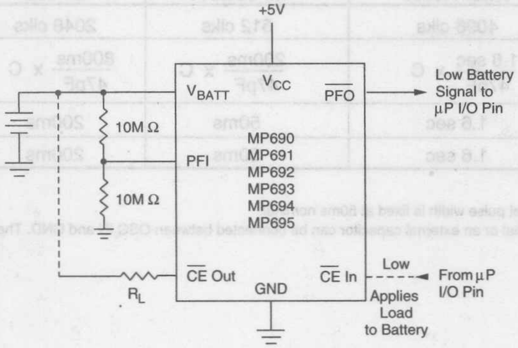
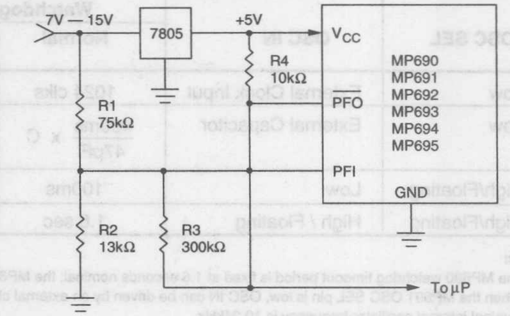


Figure 11. Backup Battery Monitor with Optional Test Load



$V_H = 9.125V$
$V_L = 7.9V$
Hysteresis = 1.23V

$$V_H = 1.3V \left(1 + \frac{R1}{R2} + \frac{R1}{R3}\right)$$

$$V_L = 1.3V \left(1 + \frac{R1}{R2} + \frac{(5V - 1.3V)\,R1}{1.3V\,(R3 + R4)}\right)$$

$$\text{Hysteresis} \approx 5V \times \frac{R1}{R3}$$

Assuming $R4 \ll R3$

Figure 12. Adding Hysteresis to the Power Fail Voltage Comparator

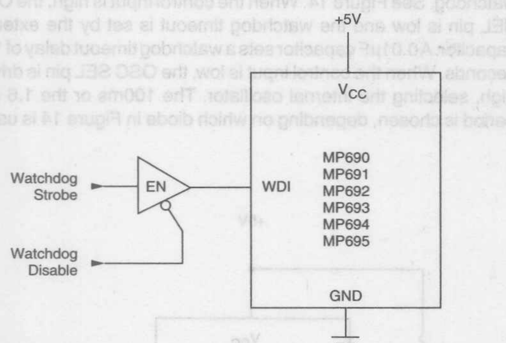


Figure 13. Disabling the Watchdog Under Program Control

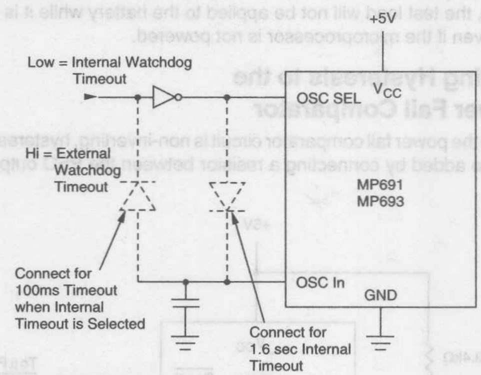
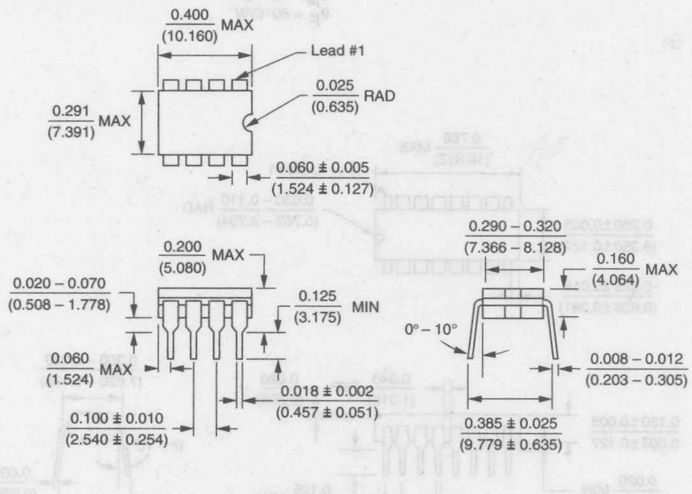


Figure 14. Selecting Internal or External Watchdog Timeout

Table 2. Input and Output Status In Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	Logic high.
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high.
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low.
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE}$ OUT	Logic high.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12μA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1μA maximum when V_{CC} is less than V_{BATT} - 700mV.

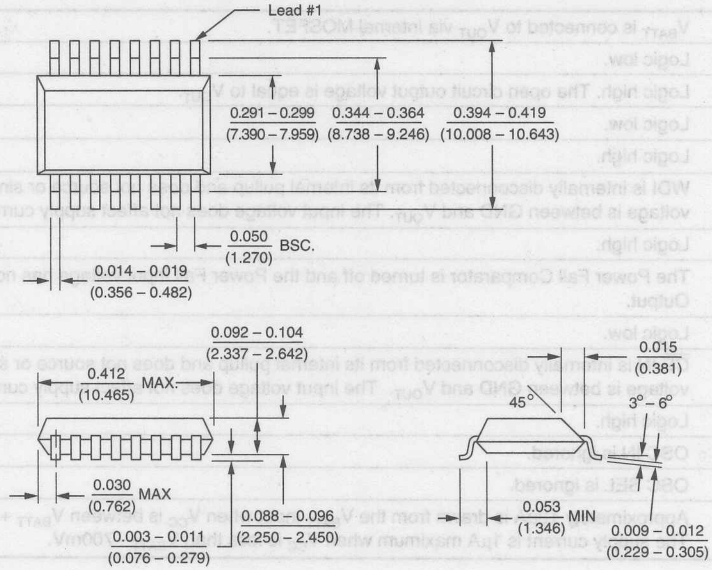
Package Information



8 LEAD CERDIP (D)

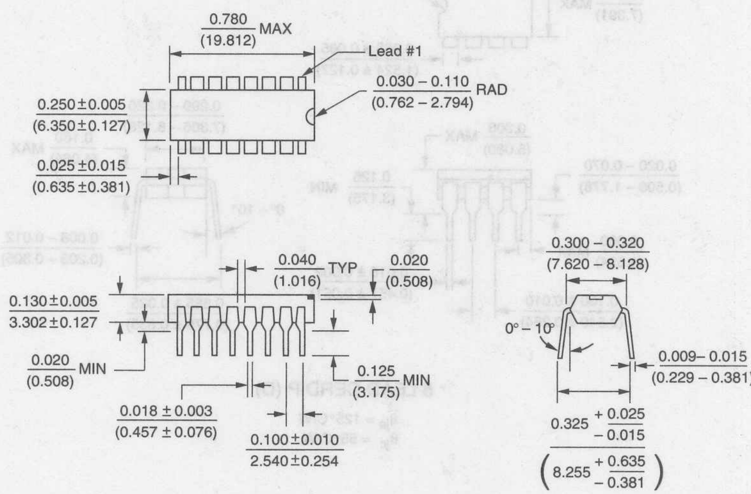
θ_{ja} = 125°C/W
θ_{jc} = 55°C/W

14



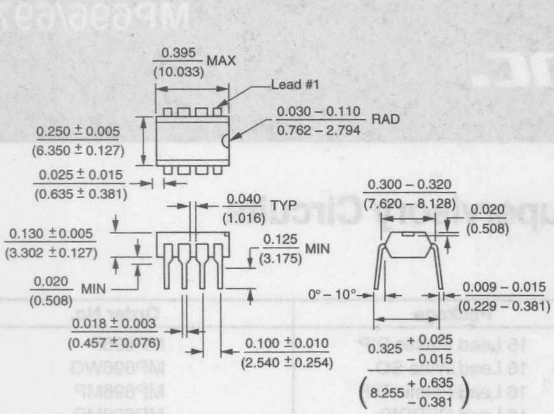
16 Lead Small Outline, Wide (WG)

θ_{ja} = 105° C/W
θ_{jc} = 60° C/W



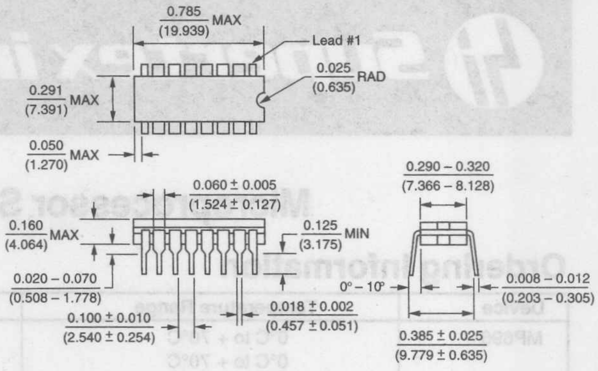
16 Lead Plastic DIP (P)

θ_{ja} = 100° C/W
θ_{jc} = 60°C/W



8 LEAD PLASTIC DIP (P)

θ_{ja} = 120° C/W
θ_{jc} = 70° C/W



16 LEAD CERDIP (D)

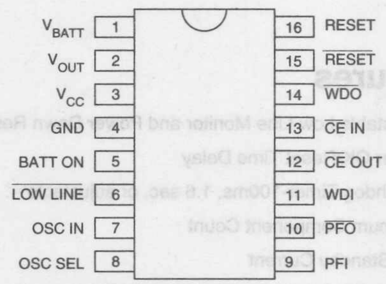
θ_{ja} = 100° C/W
θ_{jc} = 50° C/W

Pin Configuration

MP690, MP692 and MP694

top view
8-pin DIP

MP691, MP693 and MP695



top view
16-pin DIP

14

Supertex inc.

Microprocessor Supervisory Circuits

Ordering Information

Device	Temperature Range	Package	Order No.
MP696	0°C to + 70°C	16 Lead Plastic DIP	MP696P
	0°C to + 70°C	16 Lead Wide SO	MP696WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP696MP
	-40°C to + 85°C	16 Lead CERDIP	MP696MD
	-40°C to + 85°C	16 Lead Wide SO	MP696MWG
	-55°C to + 125°C	16 Lead CERDIP	RCMP696D
MP697	0°C to + 70°C	16 Lead Plastic DIP	MP697P
	0°C to + 70°C	16 Lead Wide SO	MP697WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP697MP
	-40°C to + 85°C	16 Lead CERDIP	MP697MD
	-40°C to + 85°C	16 Lead Wide SO	MP697MWG
	-55°C to + 125°C	16 Lead CERDIP	RCMP697D

Features

- ☐ Adjustable Low Line Monitor and Power Down Reset
- ☐ Power OK/Reset Time Delay
- ☐ Watchdog Timer-100ms, 1.6 sec, or adjustable
- ☐ Minimum Component Count
- ☐ 1uA Standby Current
- ☐ Battery Backup Power Switching (MP696)
- ☐ Onboard Gating of Chip Enable Signals (MP697)
- ☐ Separate Monitor for Power Fail or Low Battery Warning

Applications

- ☐ Computers
- ☐ Controllers
- ☐ Intelligent Instruments
- ☐ Automotive Systems
- ☐ Critical µP Power Monitoring

General Description

The MP696/697 supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include uP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MP696/697 significantly improves system reliability and accuracy compared to that obtained with separate ICs or discrete components.

The MP696 and MP697 are supplied in 16 pin packages and perform six functions:

1. A Reset output during power-up, power-down and brownout conditions. The threshold for this "low line" reset is adjustable by an external voltage divider.
2. A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
3. Individual outputs for low line and watchdog fault conditions.
4. The Reset time may be left at its default value of 50 ms. or may be varied with an external capacitor or clock pulses.
5. A separate 1.3 volt threshold detector for power fail warning, low battery detection, or to monitor a power supply other than V_{CC}.

The MP696 also has battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic.

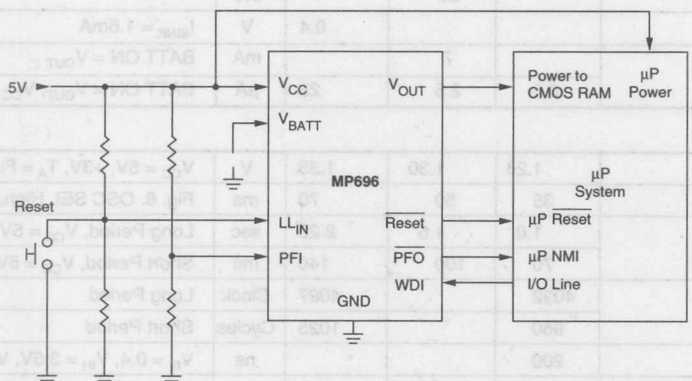
The MP697 lacks battery backup switching, but has write protection pins (CE_{IN} and CE_{OUT}) for CMOS RAM or EPROM. In addition, it consumes less than 250 microamperes.

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
V_{BATT}	-0.3V to 6.0V
All Other Inputs (Note 1)	-0.3V to (V_{OUT} +0.5V)
Input Current	
V_{CC}	200mA
V_{BATT}	50mA
GND	20mA
Output Current	
V_{OUT}	Short Circuit Protected
All Other Outputs	20mA
Rate-of-Rise, V_{BATT}, V_{CC}	100V/µs
Power Dissipation	
16 Pin Plastic DIP (Derate 7mW/°C above +70°C)	600mW
16 Pin Small Outline (Derate 7mW/°C above +70°C)	600mW
16 Pin CERDIP (Derate 10mW/°C above +85°C)	600mW
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Operation Circuit



MP696 Typical Application

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Electrical Characteristics

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1, 2 and 3)

Parameter	Min	Typ	Max	Unit	Conditions
Operating Voltage Range					
MP696, V_{CC}	3.0		5.5	V	T_A = Full
MP696, V_{BATT}	2.0		V_{CC} -0.3	V	T_A = Full
MP697, V_{CC}	3.0		5.5	V	T_A = Full
Supply Current (MP697)		160	300	µA	T_A = Full
BATTERY BACKUP SWITCHING (MP696)					
V_{OUT} Output Voltage		V_{CC}- 0.1	V_{CC}- 0.3	V	I_{OUT} = 1mA, T_A = Full
		V_{CC}- 0.25	V_{CC}- 0.5		I_{OUT} = 50mA, T_A = Full
V_{OUT} in Battery Backup Mode	V_{BATT}- 0.1	V_{BATT}- 0.02		V	I_{OUT} = 100µA, V_{CC}< V_{BATT} - 0.2V, T_A = Full
Supply Current (excludes I_{OUT})		1.5	4	mA	I_{OUT} = 1mA
		2.5	7		I_{OUT} = 50mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0V, V_{BATT} = 2.8V, T_A = 25°C
			10		V_{CC} = 0V, V_{BATT} = 2.8V, T_A = Full
Battery Standby Leakage Current	-100		+20	nA	5.5V > V_{CC} > V_{BATT} + 0.3V, T_A = 25°C
	-1		+0.02	µA	5.5V > V_{CC} > V_{BATT} + 0.3V, T_A = Full
Battery Switchover Threshold		70		mV	Power Up
V_{CC} - V_{BATT}		50			Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.4	V	I_{SINK} = 1.6mA
BATT ON Output Short Circuit Current		7		mA	BATT ON = V_{OUT}
	0.5	2.5	25	µA	BATT ON = V_{OUT}, V_{CC} =0V
RESET AND WATCHDOG TIMER					
Low Line Voltage Threshold (LL_{IN})	1.25	1.30	1.35	V	V_{CC} = 5V, +3V, T_A = Full
Reset Timeout Delay	35	50	70	ms	Fig. 6. OSC SEL High, V_{CC} = 5V
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	sec	Long Period, V_{CC} = 5V
	70	100	140	ms	Short Period, V_{CC} = 5V
Watchdog Timeout Period, External Clock	4032		4097	Clock Cycles	Long Period
	960		1025		Short Period
Minimum WDI Input Pulse Width	200			ns	V_{IL} = 0.4, V_{IH} = 3.5V, V_{CC} = 5V
$\overline{RESET}$ and RESET Output Voltage[3]			0.4	V	I_{SINK} = 400µA, V_{CC} = 2V, V_{BATT} = 0
			0.4		I_{SINK} = 1.6mA, 3V < V_{CC} < 5.5V
	3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
$\overline{LOW\ LINE}$ and $\overline{WDO}$ Output Voltage			0.4	V	I_{SINK} = 800µA, T_A = Full
	3.5				I_{SOURCE} = 1µA, V_{CC} = 5V , T_A = Full
Output Short Circuit Current	1	3	25	µA	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOWLINE}$
WDI Input Threshold — Logic Low			0.8	V	V_{CC} = 5V [2]
WDI Input Threshold — Logic High (MP696)	3.5				
WDI Input Threshold — Logic High (MP697)	3.8				
WDI Input Current		20	50	µA	WDI = V_{OUT}
	-50	-15			WDI = 0V

Electrical Characteristics (continued)

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1, 2 and 3)

Parameter	Min	Typ	Max	Unit	Conditions
POWER FAIL DETECTOR					
PFI Input Threshold	1.2	1.3	1.4	V	V_{CC} =3V, 5V
PFI -LL_{IN} Threshold Difference		±15	±50	mV	V_{CC} =3V, 5V
PFI Input Current		±0.01	±25	nA	0 To V_{CC} - 0.7V
LL_{IN} Input Current	-25	±0.01	25	nA	MP697
	-500	±0.01	25		MP696
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 1.6mA
	3.5				I_{SOURCE} = 1μA, V_{CC} =5V
$\overline{PFO}$ Short Circuit Source Current	1	3	25	μA	PFI = 0V, $\overline{PFO}$ = 0V
CHIP ENABLE GATING (MP697)					
$\overline{CE}$ IN Thresholds			0.8	V	V_{IL}
	3.0				V_{IH}, V_{CC} = 5V
$\overline{CE}$ IN Pullup Current		3		μA	
$\overline{CE}$ OUT Output Voltage			0.4	V	I_{SINK} = 1.6mA
	V_{CC} -0.5				I_{SOURCE} = 800μA
	V_{CC} -0.05				I_{SOURCE} = 1μA, V_{CC} = 0V
$\overline{CE}$ Propagation Delay		80	150	ns	V_{CC} = 5V
OSCILLATOR					
OSC IN Input Current		±2		μA	
OSC SEL Input Pullup Current		5		μA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0V, C_{OSC} = 47pF

Notes:
1. The input voltage limits on PFI and WDI may be exceeded providing the input current is limited to less than 10mA.
2. WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Pin Description

Name	Pin		Function
	MP696	MP697	
V_{CC}	3	3	The +5V input.
V_{BATT}	1		Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	2		The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	4	5	0V ground reference for all signals.
$\overline{\text{RESET}}$	15	15	$\overline{\text{RESET}}$ goes low whenever LL_{IN} falls below 1.3 volts or V_{CC} falls below the V_{BATT} input voltage. $\overline{\text{RESET}}$ remains low for 50ms after LL_{IN} goes above 1.3 volts. $\overline{\text{RESET}}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{\text{RESET}}$ pulse width can be adjusted as shown in Table 1.
WDI	11	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and $\overline{\text{WDO}}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	9	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND when not used. See Figure 1.
$\overline{\text{PFO}}$	10	10	$\overline{\text{PFO}}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{\text{PFO}}$ goes low when V_{CC} is below V_{BATT}.
$\overline{\text{CE}}$ IN		13	The input to the $\overline{\text{CE}}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{\text{CE}}$ OUT		12	$\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and LL_{IN} is above 1.3V. See Figure 5.
BATT ON	5		BATT ON goes high when V_{CC} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 100mA rating of V_{OUT}.
$\overline{\text{LOW LINE}}$	6	6	$\overline{\text{LOW LINE}}$ goes low when LL_{IN} falls below 1.3 volts. It returns high as soon as LL_{IN} rises above 1.3 volts. See Figure 5, Reset Timing.
RESET	16	16	RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.
OSC SEL	8	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	7	7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven low. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 7. When OSC SEL is high, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{\text{WDO}}$	14	14	The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{\text{WDO}}$ remains high. $\overline{\text{WDO}}$ also goes high when $\overline{\text{LOW LINE}}$ goes low.
NC	12	2	NO CONNECTION. Leave this pin open.
LL_{IN}	13	4	LOW LINE INPUT. LL_{IN} is the CMOS input to a comparator whose other input is a precision 1.3 volt reference. The output is $\overline{\text{LOW LINE}}$ and is also connected to the reset pulse generator. See Figure 2.
TEST		1	Used during manufacture only. Always ground this pin.

Typical Applications

MP696

A typical connection for the MP696 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 500Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1µA maximum when V_{CC} is between 0V and V_{BATT} -700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor's $\overline{\text{RESET}}$ line low when LL_{IN} is below 1.3V. An internal monostable holds $\overline{\text{RESET}}$ low for 50ms after LL_{IN} rises above 1.3V. This prevents repeated toggling of $\overline{\text{RESET}}$ even if the V_{CC} power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors take several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The power-up $\overline{\text{RESET}}$ pulse lasts 50ms to allow for this oscillator start-up time. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MP696 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3V, the Power Fail Output ($\overline{\text{PFO}}$) drives the processor's NMI input low. An earlier power fail warning can be generated if the unregulated DC input of the regulator is available for monitoring.

Watchdog Timer

The microprocessor drives the Watchdog Input (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MP696 will issue a 50ms $\overline{\text{RESET}}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The Watchdog Output ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low, it remains low until a transition occurs at WDI while $\overline{\text{RESET}}$ is high. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 7.

MP697

The MP697 is nearly identical to the MP696. The MP697 lacks the battery backup feature, so it does not have the V_{BATT}, V_{OUT}, or BATT ON pins. This allows the MP697 to consume less than 250 microamperes, and it allows the inclusion of RAM write protection pins. See Figure 2.

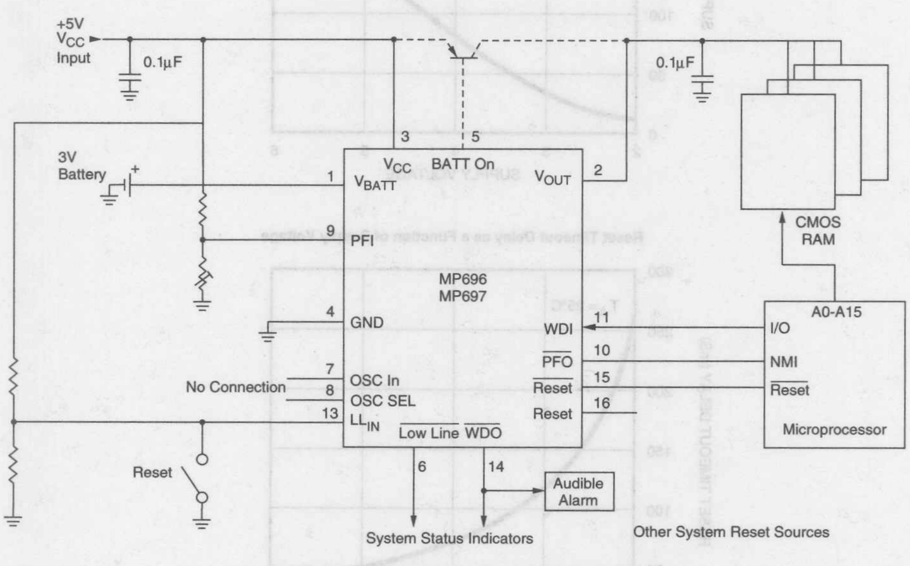
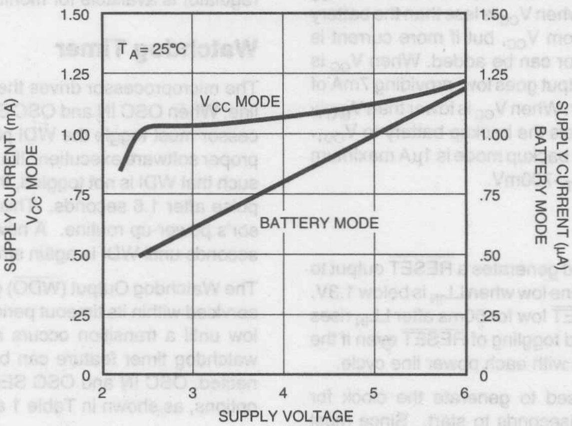


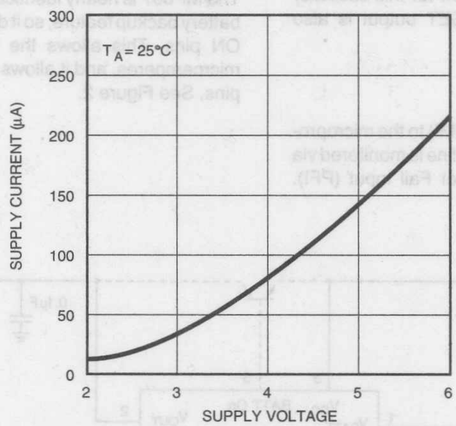
Figure 1. MP696 Typical Application

Microprocessor Supervisory Circuits

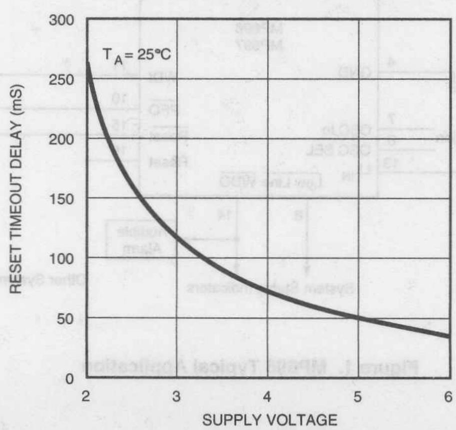
MP696
Supply Current as a Function of Supply Voltage



MP697
Supply Current as a Function of Supply Voltage



Reset Timeout Delay as a Function of Supply Voltage



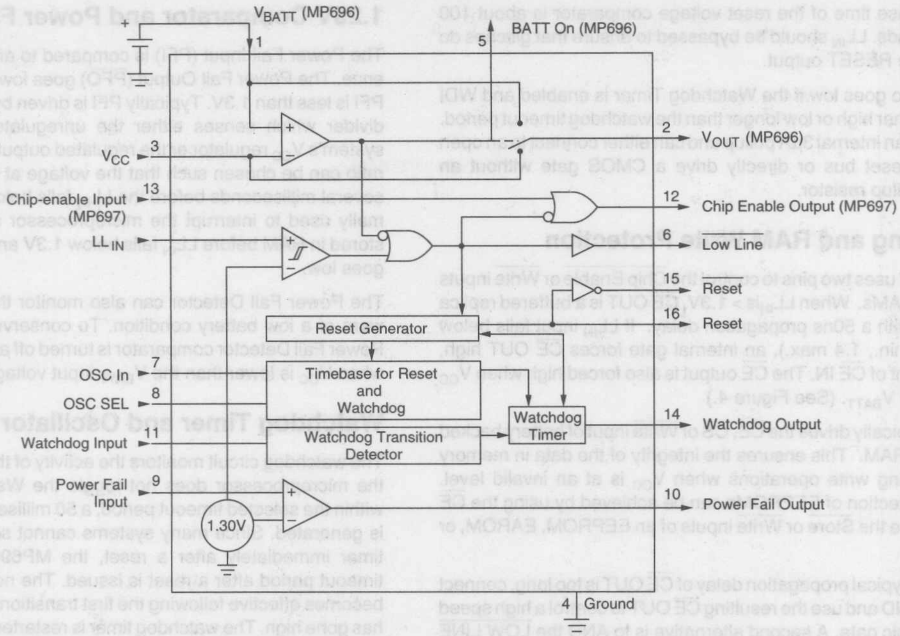


Figure 2. MP696/697 Block Diagram

Detailed Description

Battery-Switchover and V_{OUT} (MP696)

The battery switchover circuit compares V_{CC} to the V_{BATT} input and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (See Figure 3). The switchover comparator has 20mV of hysterisis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capabiltiy and thermal shutdown short circuit protection. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output can directly drive the base of the external transistor.

It should be noted that the MP696 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75nA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current while V_{OUT} need only supply the average load current which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 500 ohm MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT}, the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV), the typical supply current is only 600nA typical, 1µA maximum.

The MP696 operates with battery voltages from 2.0V to 4.25V. The battery voltage should not be within 0.5V of V_{CC} or switchover may occur. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The capacitor charging voltage should include a diode to limit the fully charged voltage to approximately 0.5V less than V_{CC}. The charging resistor for rechargable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small leakage current of typically 10nA (20nA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT}, but its polarity is such that the backup battery is always slightly charged and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum current (20nA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the status of the input and output in the low power battery backup mode.

Reset Output

$\overline{\text{RESET}}$ is an active low output which goes low whenever LL_{IN} falls below 1.3 volts. It will remain low until LL_{IN} rises above 1.312 volts for 50 milliseconds. (See Figures 4 and 5).

The guaranteed minimum and maximum low line thresholds of the MP696/697 are 1.2 and 1.4 volts. The LL_{IN} comparator has approximately 12mV of hysteresis.

The response time of the reset voltage comparator is about 100 microseconds. LL_{IN} should be bypassed to ensure that glitches do not activate RESET output.

$\overline{\text{RESET}}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{RESET}}$ hs an internal 3µA pullup and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{\text{CE}}$ Gating and RAM Write Protection

The MP697 uses two pins to control the $\overline{\text{Chip Enable}}$ or $\overline{\text{Write}}$ inputs of CMOS RAMs. When $LL_{IN}$is > 1.3V, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN, with a 50ns propagation delay. If LL_{IN} input falls below 1.3V (1.2 min., 1.4 max.), an internal gate forces $\overline{\text{CE}}$ OUT high, independent of $\overline{\text{CE}}$ IN. The $\overline{\text{CE}}$ output is also forced high when V_{CC} is less than V_{BATT}. (See Figure 4.)

CE OUT typically drives the $\overline{\text{CE}}$, $\overline{\text{CS}}$ or $\overline{\text{Write}}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{\text{CE}}$ OUT to drive the $\overline{\text{Store}}$ or $\overline{\text{Write}}$ inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{\text{CE}}$ OUT is too long, connect $\overline{\text{CE}}$ IN to GND and use the resulting $\overline{\text{CE}}$ OUT to control a high speed external logic gate. A second alternative is to AND the $\overline{\text{LOW LINE}}$ output with the $\overline{\text{CE}}$ or $\overline{\text{WR}}$ signal. An external logic gate and the $\overline{\text{RESET}}$ output of the MP696/697 can also be used for CMOS RAM write protection.

1.25V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output ($\overline{\text{PFO}}$) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's V_{CC} regulator or the regulated output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the LL_{IN} falls below 1.3V. $\overline{\text{PFO}}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before LL_{IN} falls below 1.3V and the $\overline{\text{RESET}}$ output goes low.

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{\text{PFO}}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 milliseconds $\overline{\text{RESET}}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MP696/697 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by LL_{IN} falling below 1.3V. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input(WDI).

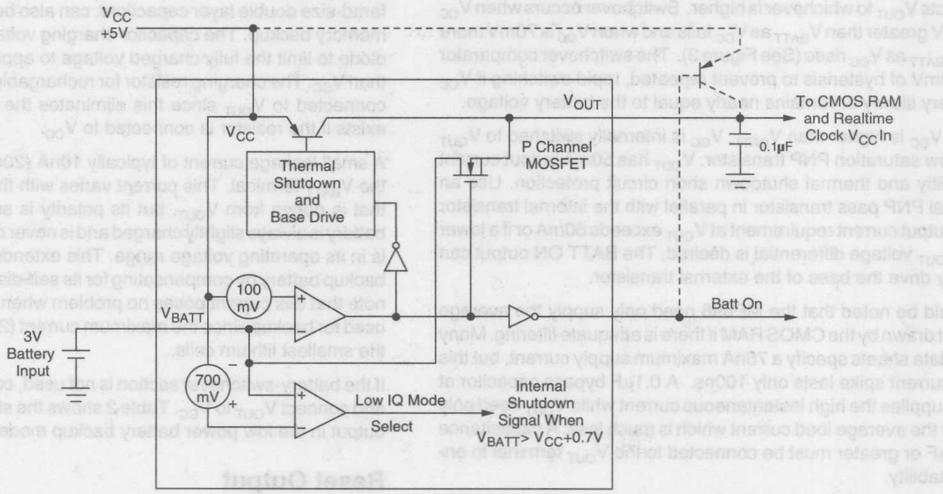


Figure 3. MP696 Battery Switchover Block Diagram

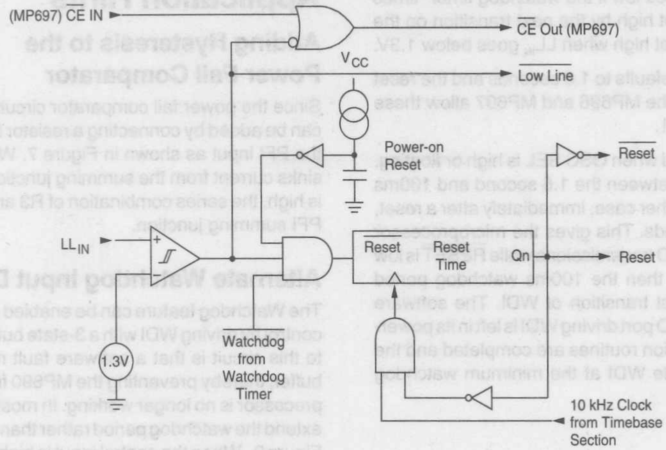


Figure 4. Reset Block Diagram

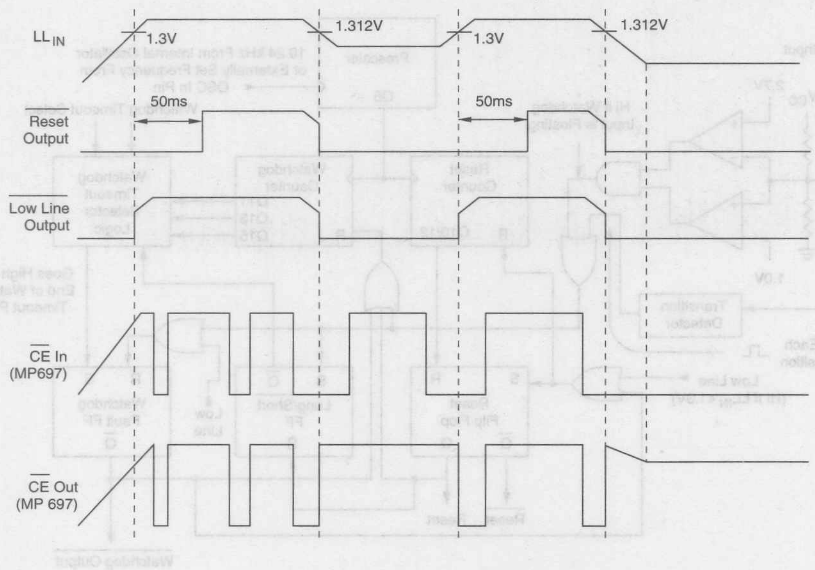


Figure 5. MP697 Reset Timing

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The Watchdog Output $\overline{WDO}$ goes low if the watchdog timer "times out," and it remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when LL_{IN} goes below 1.3V.

The watchdog timeout period defaults to 1.6 seconds and the reset pulse width defaults to 50ms. The MP696 and MP697 allow these times to be adjusted per Table 1.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset, the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. WD transmissions while $\overline{RESET}$ is low are ignored. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

Application Hints

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 7. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 8). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MP690 from detecting that the microprocessor is no longer working. In most cases, a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 9. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01µF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec. period is chosen, depending on which diode in Figure 9 is used.

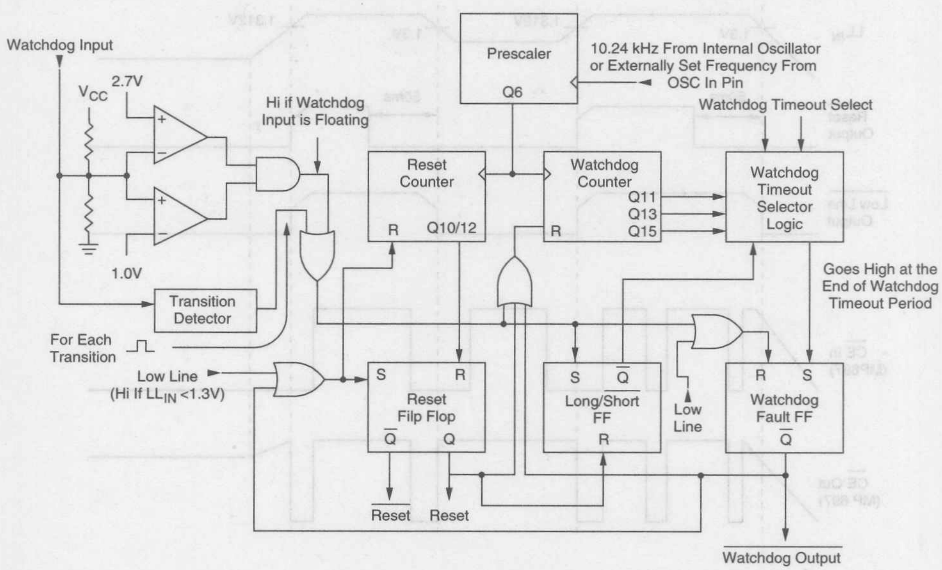


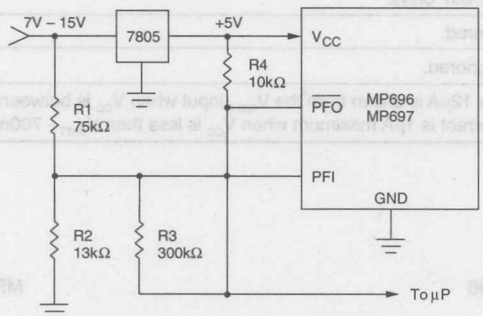
Figure 6. Watchdog Timer Block Diagram

Table 1. MP696 and MP697 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL[3]	OSC IN	Watchdog Timeout Period: Normal	Watchdog Timeout Period: Immediately After Reset	Reset Timeout Period
Low	External Clock Input	1024 clks	4096 clks	512 clks
Low	External Capacitor	$\frac{400ms}{47pF} \times C$	$\frac{1.6\,sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$
High/Floating	Low	100ms	1.6 sec	50ms
High/Floating	High / Floating	1.6 sec	1.6 sec	50ms

Notes:

1. When the MP696/697 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is $F_{OSC}(Hz) = \frac{184,000}{C_{OSC}(pF)}$
2. See Electrical Specifications Table for minimum and maximum timing values.
3. "HIGH" for the OSC SEL pin should be connected to V_{OUT}, not V_{CC} (on MP696).



$V_H = 9.125V$
$V_L = 7.9V$
Hysteresis = 1.23V

$$V_H = 1.3V \left(1 + \frac{R1}{R2} + \frac{R1}{R3}\right)$$

$$V_H = 1.3V \left(1 + \frac{R1}{R2} + \frac{(5V - 1.3V)\,R1}{1.3V\,(SR3 + R4)}\right)$$

$$\text{Hysteresis} \approx 5V \times \frac{R1}{R3}$$

Assuming $R4 \ll R3$

Figure 7. Adding Hysteresis to the Power Fail Voltage Comparator

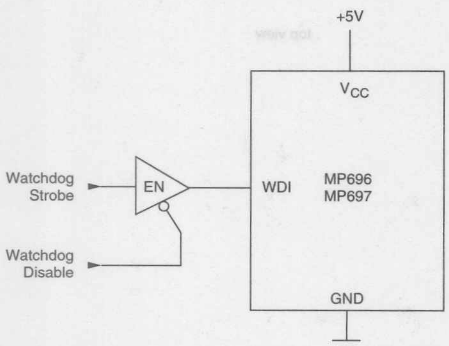


Figure 8. Disabling the Watchdog Under Program Control

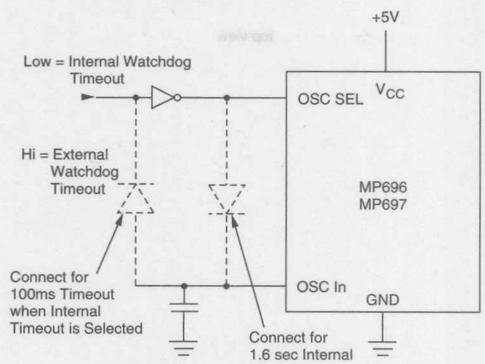


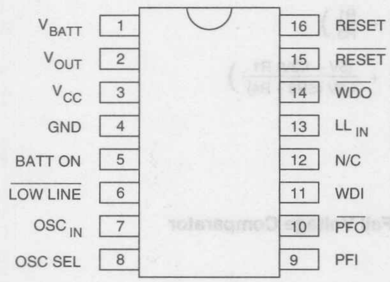
Figure 9. Selecting Internal or External Watchdog Timeout

Table 2. Input and Output Status In Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET. (MP696 only)
$\overline{\text{RESET}}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{\text{LOW LINE}}$	Logic low.
BATT ON	Logic high. (MP696 only)
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{\text{WDO}}$	Logic high.
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{\text{PFO}}$	Logic low.
$\overline{\text{CE}}$ IN	$\overline{\text{CE}}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current. (MP697 only)
$\overline{\text{CE}}$ OUT	Logic high (MP697 only).
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12µA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1µA maximum when V_{CC} is less than V_{BATT} - 700mV.

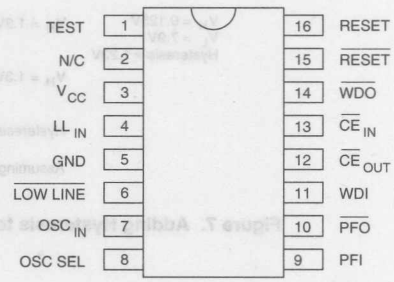
Pin Configuration

MP696



top view

MP697



top view

SD2

Supertex inc.

CMOS Photo-Electric Smoke Detector Integrated Circuit

Ordering Information

Device	Package	Order No.
SD2	16-Pin Plastic	SD2P
SD2	SOW-20	SD2WG

Features

- 6µA – Average standby current
- Minimum cost of external components
- 1mV sensitivity
- 8 to 1 increase of sample rate when smoke detected
- Improved noise rejection by multiple sampling
- Automatic LED supervisor alarm
- Multi-station input/output capability
- Horn modulation mode control
- Piezoelectric horn driver
- Smoke sensitivity adjustable by single resistor
- Self-contained oscillator requires only a resistor

Absolute Maximum Ratings

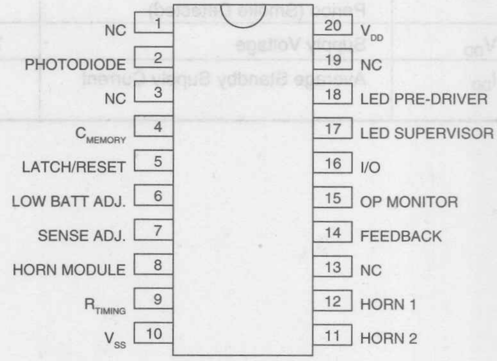
Supply Voltage	-0.5V to +15.0V
Input Voltage, all inputs	-0.5 to VDD +0.5V
Input Current, any input	±10mA
Storage Temperature Range	-40°C to +100°C
Operating Free Air Temperature Range	0°C to +55°C
Power Dissipation (Package)	300mW
Continuous Output Drive Current	25mA
Lead Temperature (Soldering, 10 sec)	300°C
Relative Humidity	90%

General Description

This low power CMOS circuit is intended for use in a pulsed LED/silicon cell smoke detector system. It is designed for use in low power, battery operated, consumer applications with a minimum of external components. This device meets UL217 requirements and is available in a 16-pin plastic DIP.

Pin Configuration

top view
16-pin DIP



top view
SOW 20

14

Electrical Characteristics

(w/R-(7) = 22 Meg Ω then f_{OSC} = 485 Hz; T_A = 25° C; V_{DD} = 9V, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IN}	Photodiode Input Leakage Current		0.01	±1.0	nA	
v_{PD}	Photodiode Input Signal Sensitivity	0.5	0.8	1.1	mV	C_{mem} = .05µF C_{input} = 5pF τ_{LED} = 100µ sec
V_{BTH}	Low Battery Threshold Voltage	7.3	7.7	8.2	V	R(4) = ∞
	Horn Modulation Frequency		8		Hz	PIN 6 to V_{DD}
	Horn Modulation Duty Cycle		62.5		%	R(7) = 22 meg Ω Smoke Detected
τ_{TBL}	Low Battery/LED Supervisor Trouble Alarm Pulse Width		17		mSec	@ f_{OSC} = 485 Hz R(7) = 22 Meg Ω
T_{TBL}	Low Battery/LED Supervisor Alarm Period		35		sec	@ f_{OSC} = 485 Hz R(7) = 22 Meg Ω
I_{OUT}	Horn Output Current	± 25			mA	V_O = IV Sink V_O = 8V Source
V_{IN}	Feedback Input Voltage Range	V_{SS}- 15		V_{DD} + 15	V	Typical Min and Max. Not 100% tested
I_{OM}	Operation Monitor Output Current, Source	-2.5	-4.5		mA	V_{OM} = 2.0V
$I_{I/O}$	I/O Output Source Current	-4.0	-10.0		mA	$V_{I/O}$ = V_{DD} -1.0
$V_{I/O}$	Remote Alarm Trigger Voltage	0.6 V_{DD}			V	Sink Current 20mA typical at V_{DD} = 4.5V
V_{IH-ON}	LED Supervisor, upper Threshold Range	V_{DD} - 0.8		V_{DD} - 0.2		
V_{I-OFF}	LED Supervisor, Safe Region	V_{DD} - 2.5		V_{DD} - 0.8	V	
V_{IL-ON}	LED Supervisor, lower Threshold Range	V_{DD} - 4.0		V_{DD} - 2.5		
I_{LED}	LED Output Source Current	-10	-20		mA	V_{LED} = 5V
T_{LED}	Photodiode Sample Pulse Period (Smoke Detected)		1.0		sec	f_{OSC} = 485 Hz
T_{LED}	Photodiode Sample Pulse Period (Smoke Detected)		8.0		sec	f_{OSC} = 485 Hz R(7) = 22 meg Ω
V_{DD}	Supply Voltage	7.0	9.0	10.0	V	
I_{DD}	Average Standby Supply Current		6.0	10.0	µA	R(7) = 22 Meg Ω V_{DD} = 9.0, Non-Alarm Mode

Pin Definition

Pin	Name	Function
1	Photodiode Input	Connect the cathode of a VTS-4085S, or equivalent, to pin 1. Connect the anode to V_{DD}. The typical allowed signal range is from V_{DD} to V_{DD} - 1.0V.
2	Memory Capacitor Input	The capacitor may range from 0.01µF to 0.05µF and should have low leakage. The detector sensitivity increases with increasing capacitance.
3	Latch/Reset Input	When connected to V_{DD}, the detector will latch on at the first detection of smoke. When connected to V_{SS}, the alarm will not latch on detection of smoke and the low battery condition will not override the smoke alarm condition. Reset after latching is accomplished by momentarily connecting this pin to V_{SS} until the horn silences. The Latch/Reset Input only affects the local smoke alarm response.
4	Low Battery Threshold	The nominal threshold of the battery alarm is 7.7 volts. The alarm point can be raised by connecting an adjustment resistor to ground, and lowered by connecting a resistor to V_{DD}.
5	Smoke Sensitivity Adjustment	A resistor or potentiometer to ground is used to adjust the duration of the LED pulse and thereby the Smoke Sensitivity. Pulse duration is proportional to the resistor value and varies approximately 100µsec per megohm.
6	Horn Modulation Control Input	When connected to V_{DD}, the Horn will pulse ON and OFF at approximately 8 Hz, with the ON time exceeding the OFF time. When connected to V_{SS}, the "Smoke" alarm will sound the Horn continuously. This control only affects the "Smoke" alarm condition.
7	Timing Resistor	A nominal resistor value of 22 megohms to V_{SS} sets the oscillator frequency to 485 Hz. Thus: a) The IR LED pulses every 8 seconds in standby. b) The OPERATION MONITOR LED pulses every 35 seconds in standby. c) The Horn modulation (ON-OFF) frequency is approximately 8Hz. d) The Low Battery or LED SUPERVISOR trouble pulse to the Horn will occur every 35 seconds, with 17ms duration. e) The IR LED will pulse every 1 second when smoke is detected. f) The Horn will be silenced just before each IR LED pulse for 4.2 ms, to reduce electromagnetic interference.
8	V_{SS}	Connect this pin to circuit common, the lowest potential.
9	Horn Output 2	This terminal is connected to the brass electrode of the piezoelectric horn.
10	Horn Output 1	This pin is connected to the large silver electrode of the piezoelectric horn.
11	Horn Feedback	This pin is connected to the small silver electrode of the piezoelectric horn.
12	Operation Monitor	This output is a current source of 4mA for driving a visible LED. The LED will flash for 17ms every 35 seconds under normal conditions. The LED will be ON continuously when smoke is first detected. This occurs before the alarm sounds and indicates that the detector is in speed-up mode (1.0 second LED pulse period). This output indicates which unit is alarming in multiple station applications. When this output is used for both local LED indication and remote logic, a resistor must be placed in series with the LED.
13	Multiple Station Input/Output	This Input/Output may be connected via twisted pairs to at least 20 other units. The output goes high after at least two consecutive smoke detections have been made. The output structure allows units of different operating voltages to be connected together with no impairment of performance or excessive loading of the higher voltage units. There is an active pull-down on the output. Because of the high current-sourcing capability of the output, this pin should never be connected to V_{SS} via a low impedance path. An Input level of greater than $0.6V_{DD}$ volts is required to ensure a local alarm.
14	LED Supervisor	This pin must be connected to the LED circuit as shown. Failures detected are open or shorted conditions in the LED and Driver circuit. A failure is indicated by a local pulsed trouble alarm. To defeat this feature, pin 14 must be tied to a voltage about 1.5-volts below V_{DD}, or to pin 2 in most applications.
15	LED Pre-Driver Output	This terminal can source about 13mA. The output voltage is zener clamped at approximately 6.7V and the current becomes limited. The LED current set resistor may be put in the collector circuit, below the LED, but the LED current and therefore the Sensitivity of the smoke detector will vary with supply voltage.

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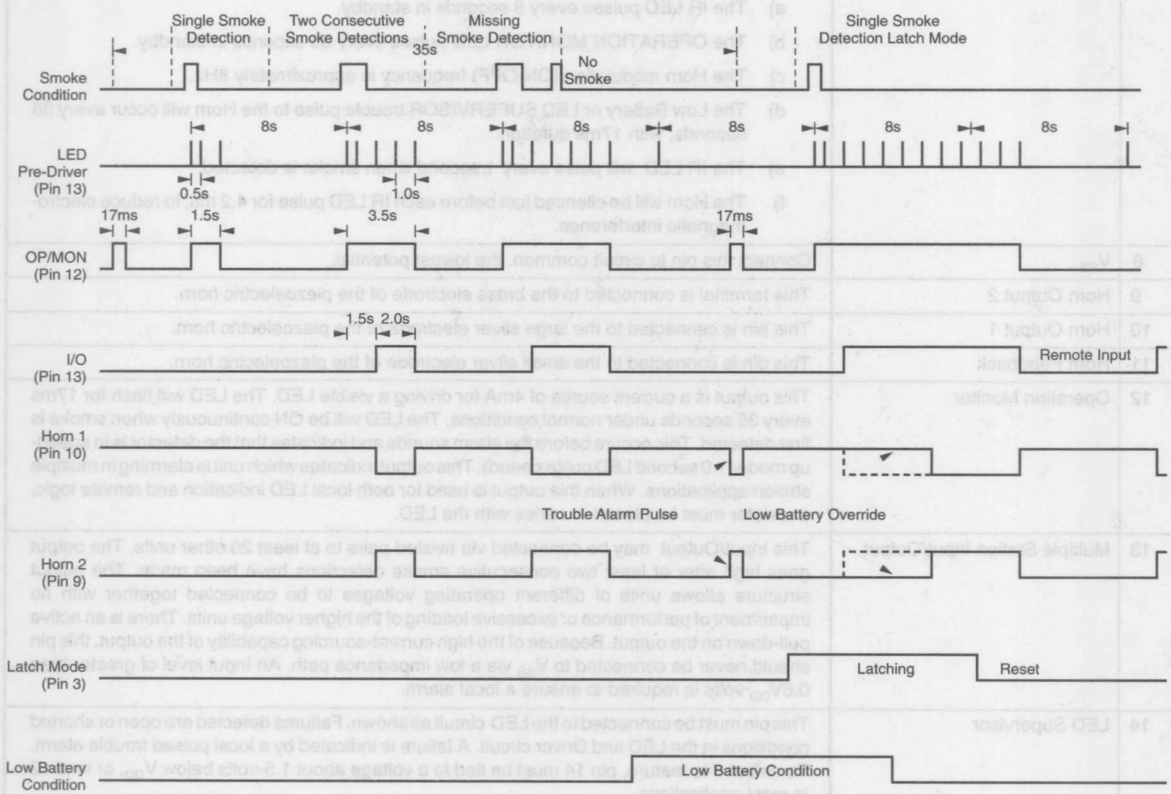
Pin Definition (cont.)

Pin	Name	Function
16	V_{DD}	This pin is connected to the positive battery terminal. Pin 16 should be solidly connected to the V_{DD} side of both the photodiode and the memory capacitor. A V_{DD} guard-ring type foil path around pins 1 and 2 will enhance noise immunity of the detection circuit. This circuit will operate from 7 to 10 volts, although average standby current will increase with supply voltage. Protect the integrated circuit from polarity reversal.
9,10	Alternate Driver for Electro-Mechanical Horns	When the smoke detector circuit is used to drive either a transistorized mechanical or electro-mechanical horn, the feedback (pin 11) must be connected to V_{DD}. When an alarm condition is not present, pin 10 will be at V_{DD} and pin 9 will be at V_{SS}. When an alarm condition is present, pin 10 will switch from V_{DD} to V_{SS} and pin 9 will switch from V_{SS} to V_{DD}. Both horn outputs are capable of sinking or sourcing more than 100mA at a 9-volt supply voltage. The steady state on current is limited to 25mA. Pin 9 must not remain at V_{DD} when chip is reset.
	Transistorized Mech. Horn	The control tab of the horn is connected to pin 9 and pin 10 is left open.
	Electro-Mechanical Horn	Pin 9 is connected through a resistor to the base of an NPN horn driver transistor. Pin 10 is left open.

Timing Waveform



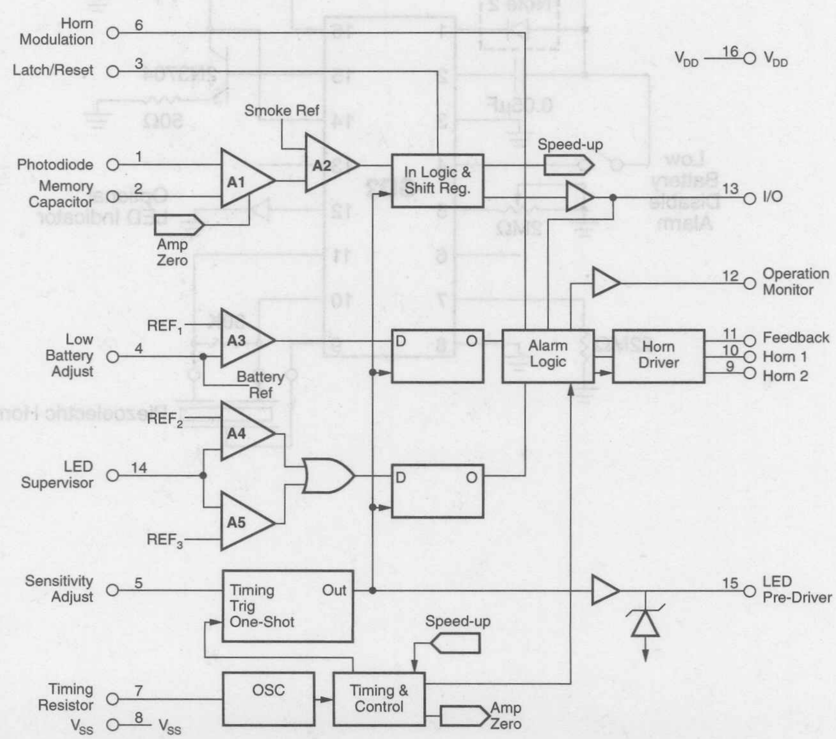
Truth Table

Alarm Status	Smoke	Low Batt.	LED Sup'r	Pin 3 Latch	Pin 4 Batt	Pin 6 Mod'l	Pin 11 Fdbk	Pin 13 I/O	Pin 9 H2	Pin 10 H1	Pin 12 OP/MO	Pin 13 I/O	Pin 15 LED
	Input Conditions						Output Conditions						
Standby	F	F	F	X	N	X	H^4	N	L	H	P^1	L	P^2
Remote	F	X	X	X	N	L	H^4	H	H^5	L^5	P^1	N	P^2
Smoke	F	X	X	X	N	H	H^4	H	$H^{5.6}$	$L^{5.6}$	P^1	N	P^2
Local	T (A)	X	X	L	N	L	H^4	N	H^5	L^5	H	H	P^3
Smoke	T (A)	X	X	L	N	H	H^4	N	$H^{5.6}$	$L^{5.6}$	H	H	P^3
Local	T (B)	F	X	H	N	L	H^4	N	H^5	L^5	H	H	P^3
Smoke	T (B)	F	X	H	N	H	H^4	N	$H^{5.6}$	$L^{5.6}$	H	H	P^3
Latched	T (B)	T	X	H	N	X	H^4	N	L^1	H^1	H	H	P^3
Low Batt	F	T	X	X	N	X	H^4	N	L^1	H^1	P^1	L	P^2
LED Sup'r	F	X	T	X	N	X	H^4	N	L^1	H^1	P^1	L	P^2
Batt Disable	F	T	F	X	H	X	H^4	N	L	H	P^1	L	P^2
Horn Disable	X	X	X	X	N	X	L	N	L	H	X	X	X

Key:
- T – Logical TRUE, Analog Condition
- F – Logical FALSE, Analog Condition
- H – Logical HIGH, Digital Level or Driver Sourcing
- L – Logical LOW, Digital Level or Driver Sinking
- P – Output PULSE HIGH, Normally LOW
- N – No Signal Applied / Open
- X – Unspecified
- A – After two consecutive smoke detections
- B – After one smoke detection

Notes:
1. Pulsed to opposite state ONCE every fourth PULSE on pin 15.
2. Normal Sample Rate, Typical 8 seconds.
3. 8 Times Normal Sample Rate, Typical 1.0 second.
4. When used with a piezo horn, this signal is oscillating,but considered HIGH.
5. When used with a piezo horn, this signal is oscillating.
6. Signal will be in non-alarm state 37.5% of time.

Block Diagram



14

Operation

This device utilizes low power CMOS technology to provide all of the necessary functions of a battery operated, photoelectric smoke detector using a minimum of external components.

The LED PRE-DRIVER output pulses an external transistor which in turn, switches on the infrared light emitting diode at a very low duty cycle. The desired IR LED pulse period is determined by the value of the external timing resistor. The Smoke Sensitivity is adjustable through a trimmer resistor which varies the IR LED pulse width.

The light sensing element is a silicon photovoltaic cell which is held at near zero bias to minimize leakage currents. The circuit can detect signals as low as 1mV and generate an alarm. The IR LED pulse repetition rate increases when smoke is detected.

For use with a 9-volt battery, an internal zener is incorporated into the IC. When the minimum battery voltage is reached (tested during the IR LED on pulse), the output produces a short trouble alarm pulse or "blip". The horn is pulsed after every fourth IR LED pulse. When the alarm mode control is set for non-latching operation, the unit will sound a continuous alarm when smoke is detected even during low battery conditions. When the alarm mode control is set for latching operation, the low battery trouble alarm will override the smoke alarm, in accordance with UL217specifications.

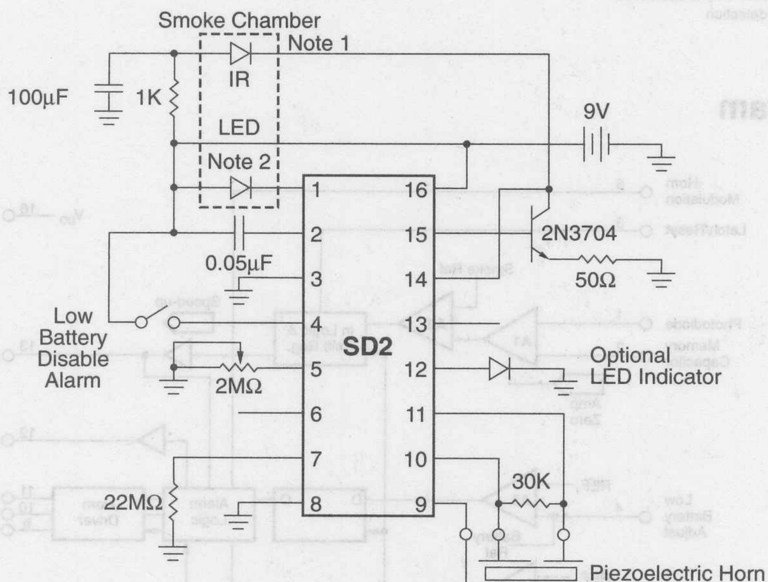
The LED SUPERVISOR tests for open or shorted conditions in the LED and Driver circuit. For either condition of the IR LED when pulsed, failure of the forward voltage to fall between two limits produces a trouble alarm pulse on the Horn after every fourth LED pulse.

The Input/Output terminal (I/O) is used to interconnect SD2 units for multiple station applications.

The OPERATION MONITOR pulses a visible LED after every fourth IR LED pulse to indicate device operation. For a local smoke detection the LED is driven continuously.

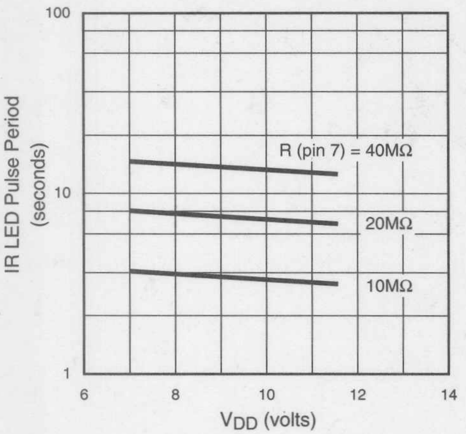
The Horn Driver circuit self-oscillates with a piezoelectric element or enables an electro-mechanical horn when pin 11 is connected to V_{DD}.

Typical System — Non-Latching Single Station

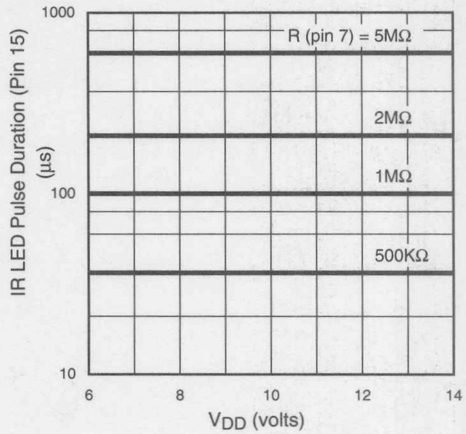


Typical Performance Curves (T_A = 25°C unless otherwise noted)

T_{LED} vs V_{DD}

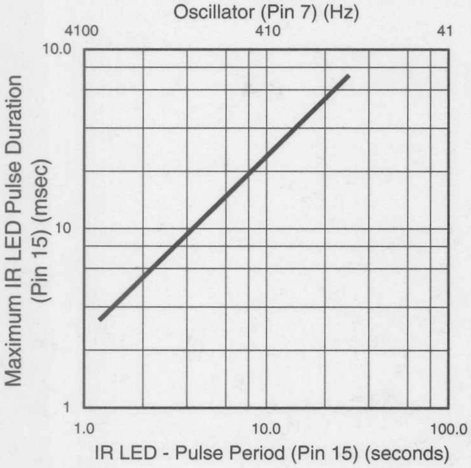


T_{PD} vs V_{DD}

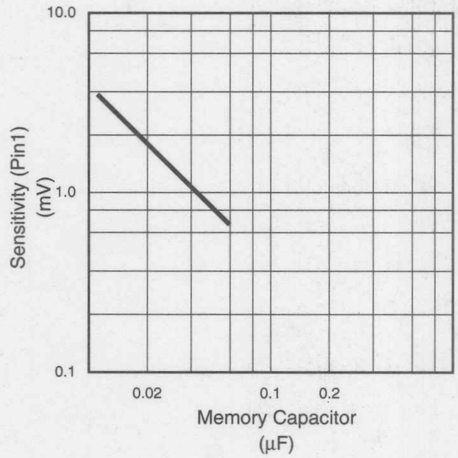


IR LED vs T_{LED} vs Oscillator

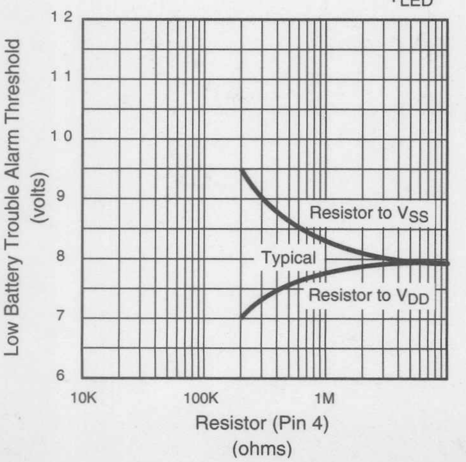
Oscillator (Pin 7) (Hz)



Detector Sensitivity vs C_{MEM}



$$I_{AVG}\ (LED) = [(I_{OH}(15)) + I_{LED}]\ \frac{T_{PD}}{T_{LED}}$$



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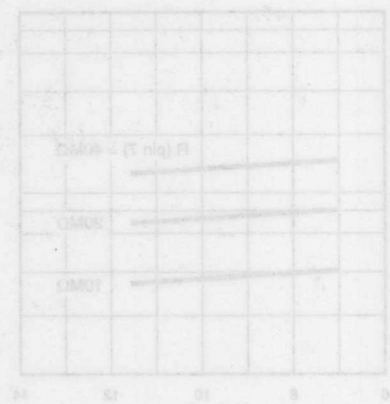
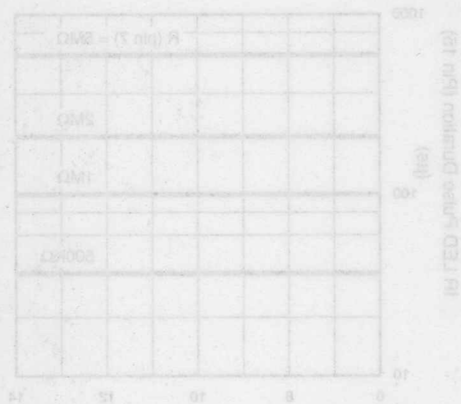
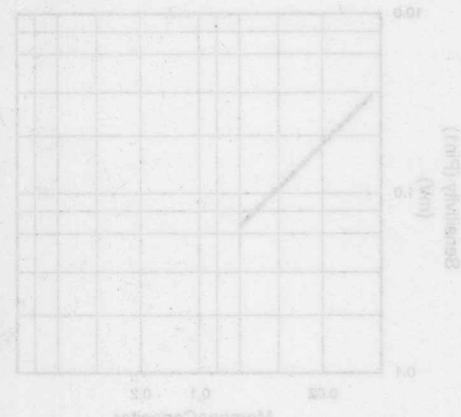
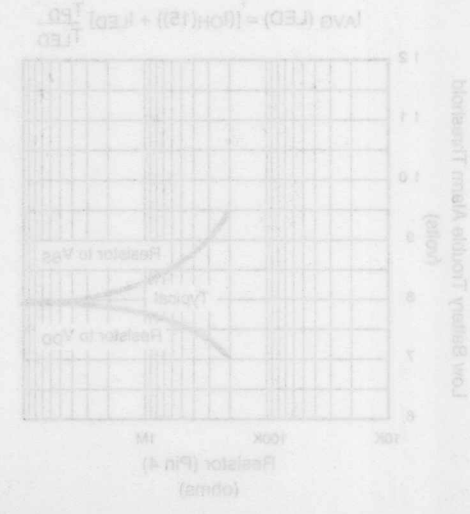
Typical Performance Curves (T_A = 25°C unless otherwise noted)





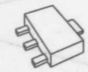




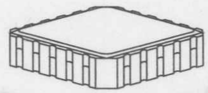
Chapter 15 – Surface Mount Packages and Lead Bend Options

Surface Mount Packages

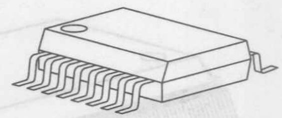
Various surface mount packages are available for HVCMOS, DMOS, and CMOS devices. Refer to the respective product data sheet for availability and package outline for detailed dimensional drawings. This section also includes lead bend and taping options.



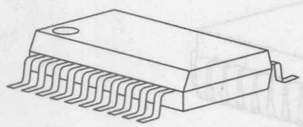
SOT-89
N8



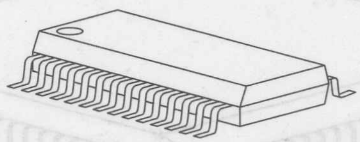
Type “C” Leadless
20 Terminal
Ceramic Chip Carrier
NF



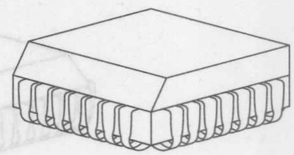
16-Lead
Small Outline
AG



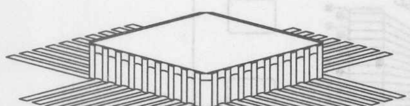
20-Lead
Small Outline
WG*



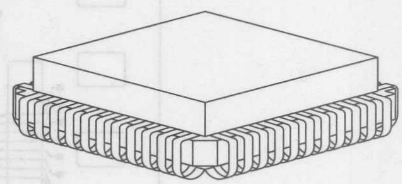
28-Lead
Small Outline
WG*



28-Lead Plastic Quad
“J” Bend
PJ



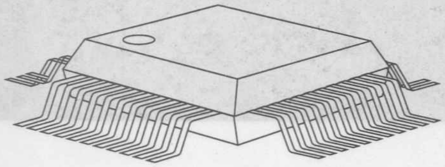
36-Leaded Ceramic Chip Carrier
CS



44-Lead Plastic and Ceramic Quads
“J” Bend
PJ / DJ

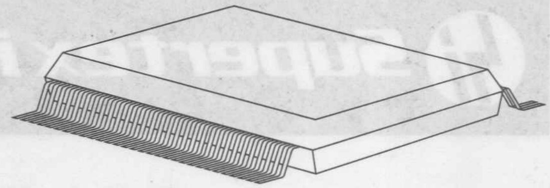
15

* 300 mil wide body



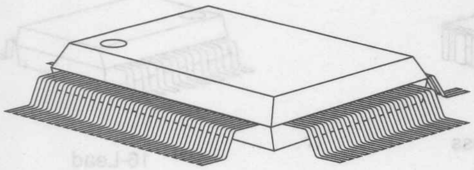
44-Lead Plastic Gullwing

PG



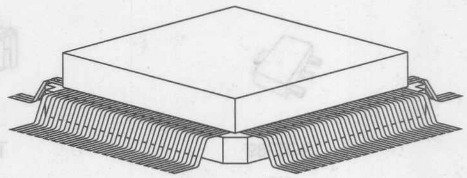
60-Lead 2-Sided Plastic Gullwing

PG



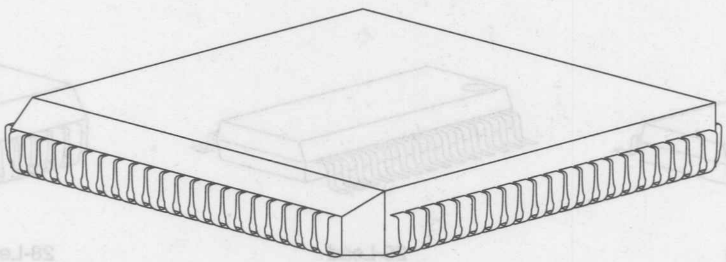
64-Lead 3-Sided Plastic Gullwing

PG / DG



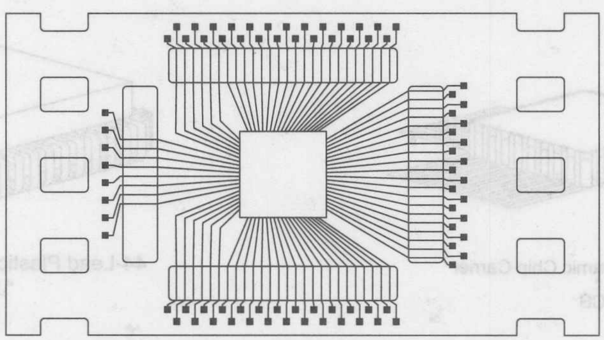
80-Lead Plastic and Ceramic Gullwing

PG / DG



84-Lead Plastic "J" Bend

PJ



Die on Tape
(for Tape Automated Bonding)

T

Lead Bend Options

Lead bend options are available in order to retrofit existing boards with small, cost effective, pin-compatible TO-92 packages, or for the purpose of surface mounting.

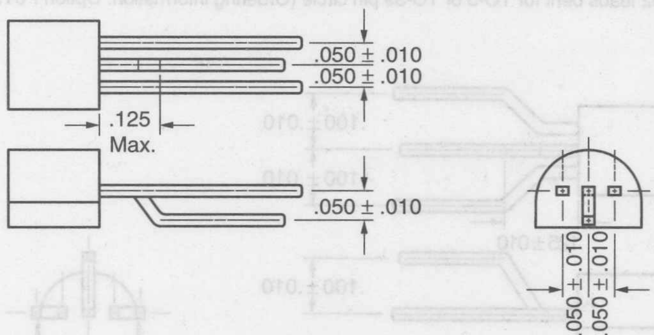


Figure 1
TO-92 leads bent for TO-18 or TO-52 pin circle (Ordering information: Option P015)*

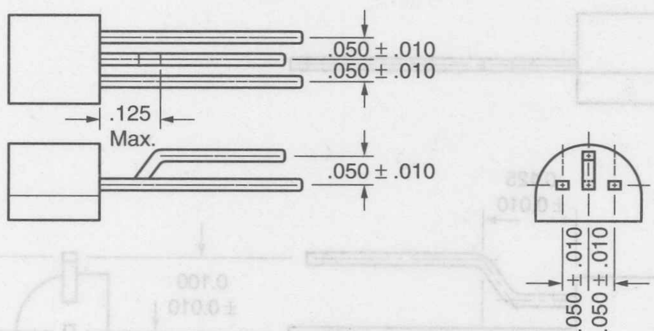


Figure 2
TO-92 leads bent for reversed TO-18 or TO-52 pin circle (Ordering information: Option P016)*

*Lead lenghts are those of original components as shown in the Package Outline Section (i.e., uncropped, unless otherwise specified).

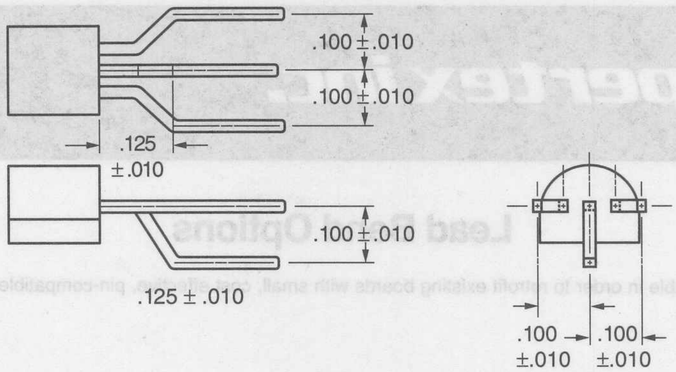


Figure 3
TO-92 leads bent for TO-5 or TO-39 pin circle (Ordering information: Option P017)*

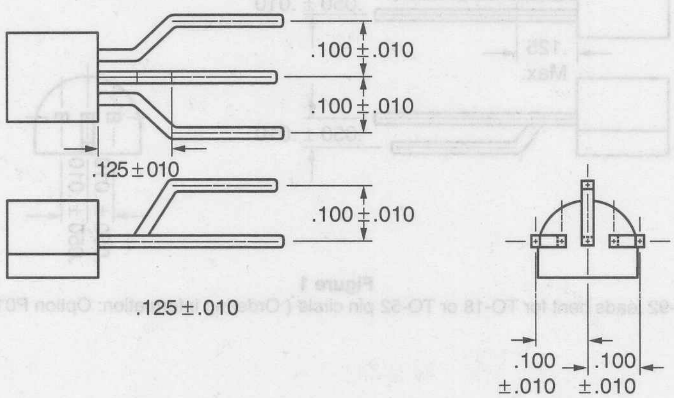


Figure 4
TO-92 leads bent for reversed TO-5 or TO-39 pin circle (Ordering information: Option P018)*

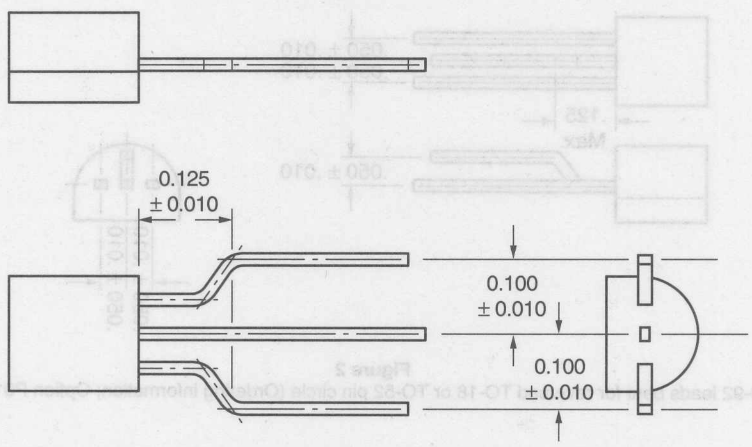


Figure 5
TO-92 leads bent for TO-220 (Ordering information: Option P011)*

*Lead lenghts are those of original components as shown in the Package Outline Section (i.e., uncropped, unless otherwise specified).

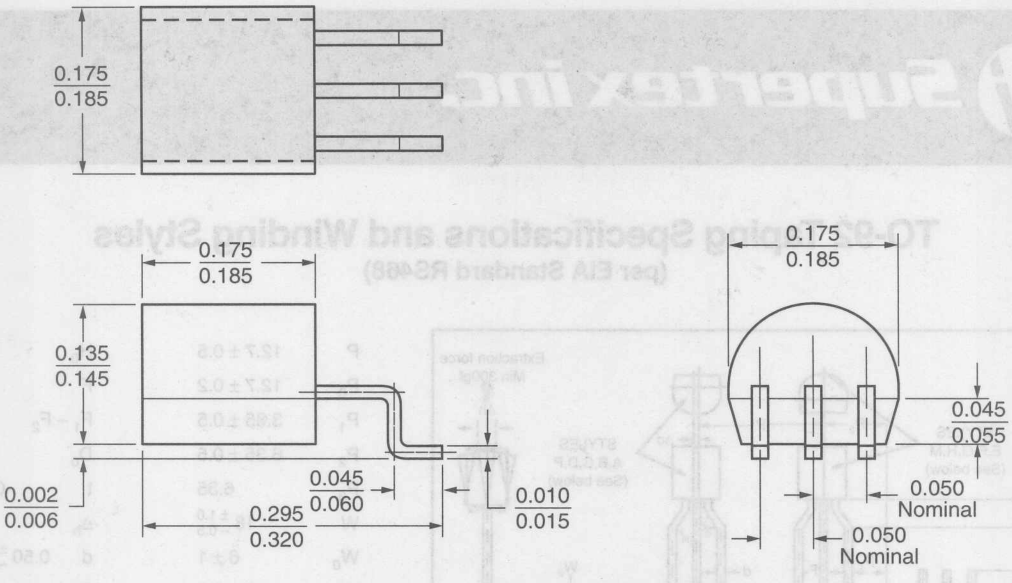
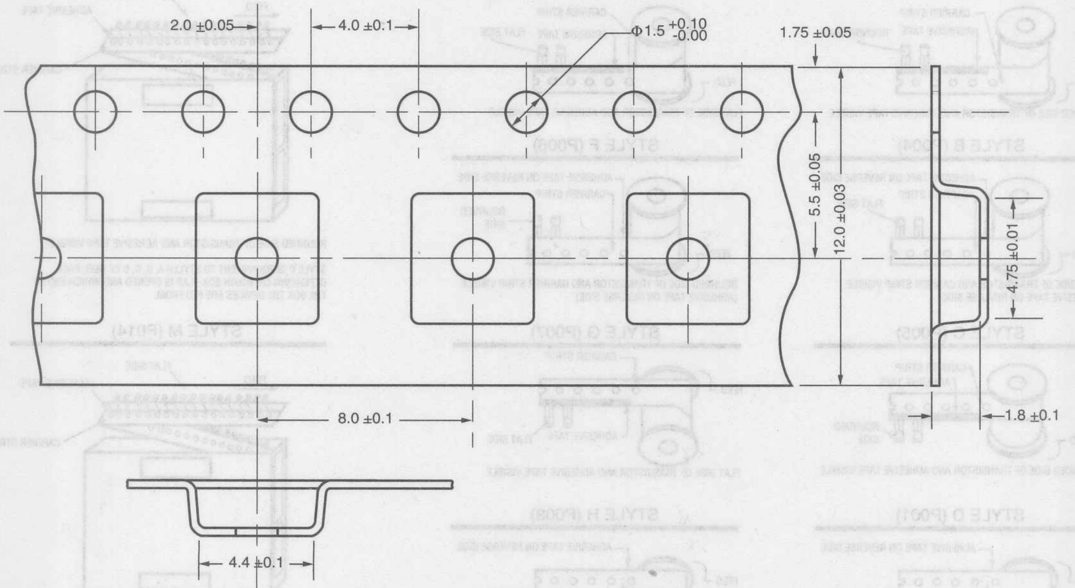


Figure 6

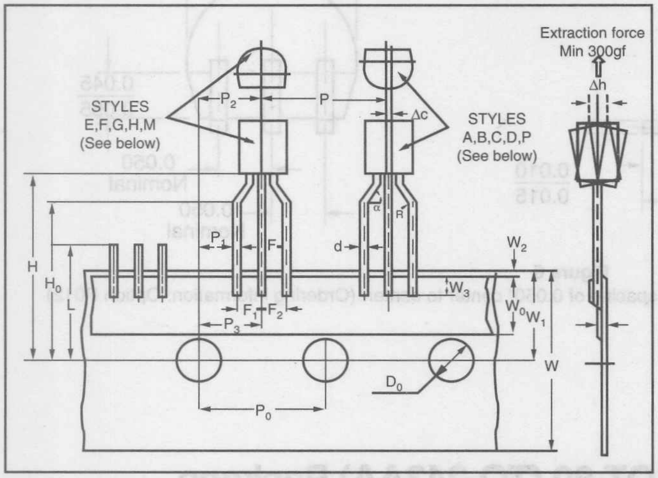
TO-92 for surface mounting. Leads formed for pad spacing of 0.050" center to center. (Ordering information: Option P012)

Carrier Tape for SOT-89 (TO-243AA) Package



Notes:
1. Tape carrier – Conductive PVC
2. Dimensions are in Millimeters
3. Top Cover Tape – 0.1mm Max

TO-92 Taping Specifications and Winding Styles
(per EIA Standard RS468)

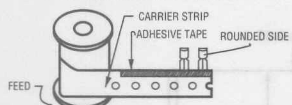


P	12.7 ± 0.5	H_0	16 ± 0.5
P_0	12.7 ± 0.2	F	$5 ^{+0.8}_{-0.2}$
P_1	3.85 ± 0.5	$F_1 - F_2$	± 0.3
P_2	6.35 ± 0.5	D_0	4 ± 0.2
P_3	6.35	t	0.7 ± 0.2
W	$18 ^{+1.0}_{-0.5}$	Δ_h	0 ± 1
W_0	6 ± 1	d	$0.50 ^{+0.06}_{-0.05}$ dia.
W_1	9 ± 0.5	R	0.8
W_2	Max. 0.5	α	45° – 60°
W_3	Min. 4.5	L	Max. 11
H	19.5 ± 0.5	Δ_C	0 ± 0.5

All dimensions in millimeters.

STYLE A (P003)

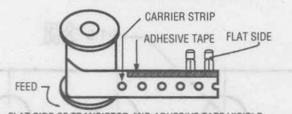
STYLE A IS PREFERRED



ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

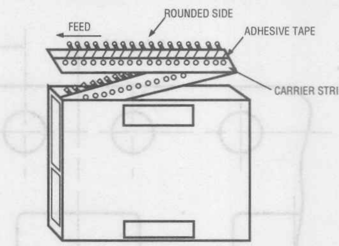
STYLE E (P002)

STYLE E IS PREFERRED



FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

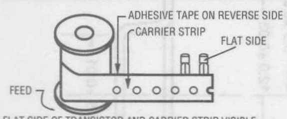
STYLE P (P013)



ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

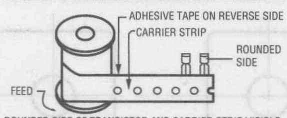
STYLE P IS EQUIVALENT TO STYLES A, B, C, D OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

STYLE B (P004)



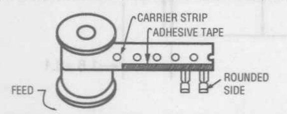
FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE F (P006)



ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE C (P005)

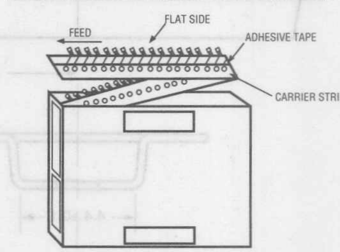


ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE G (P007)

FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

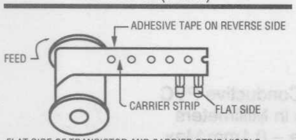
STYLE M (P014)



FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

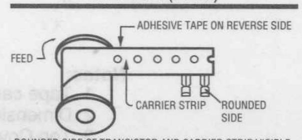
STYLE M AMMO PACK IS EQUIVALENT TO STYLES E, F, G, H, OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED-FROM.

STYLE D (P001)



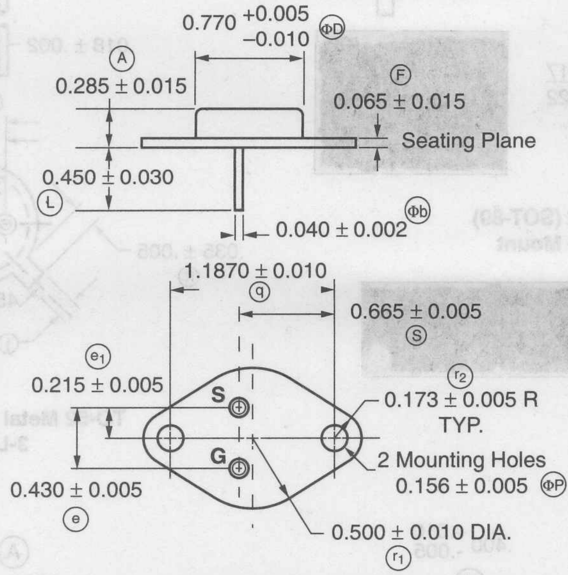
FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE H (P008)

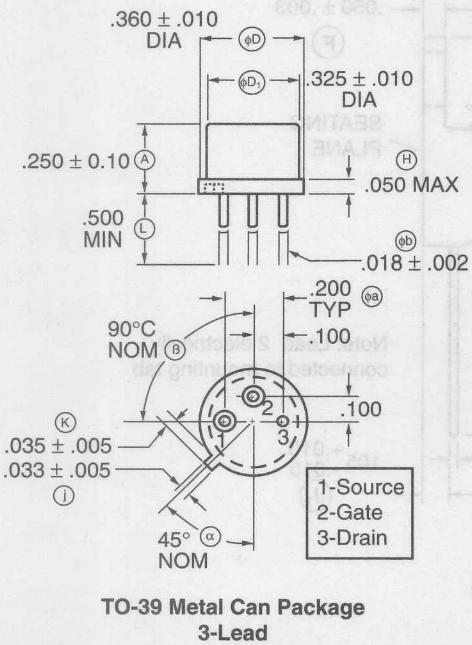


ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

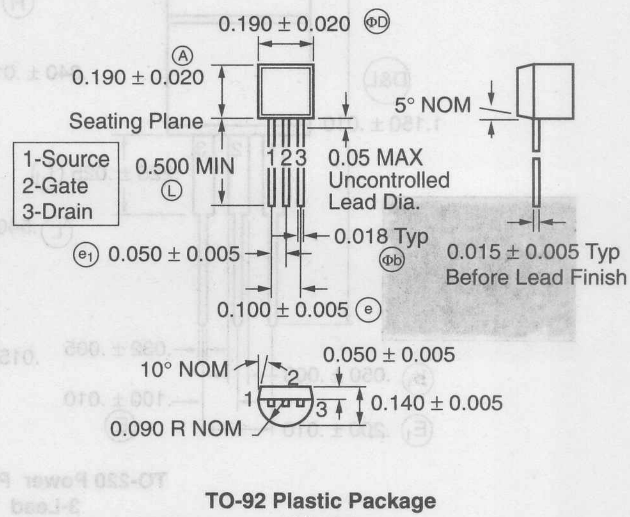
Package Outlines



TO-3 Metal Can Packages
2-Lead (Steel)

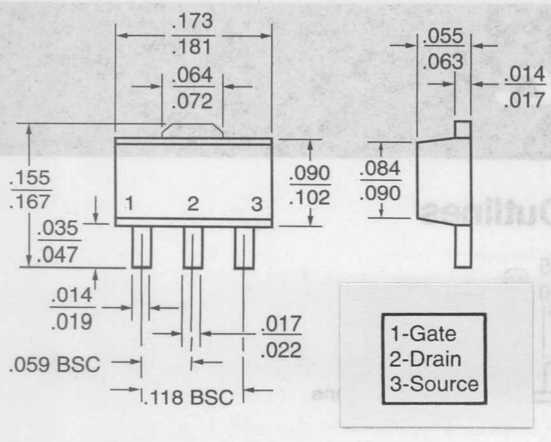


TO-39 Metal Can Package
3-Lead



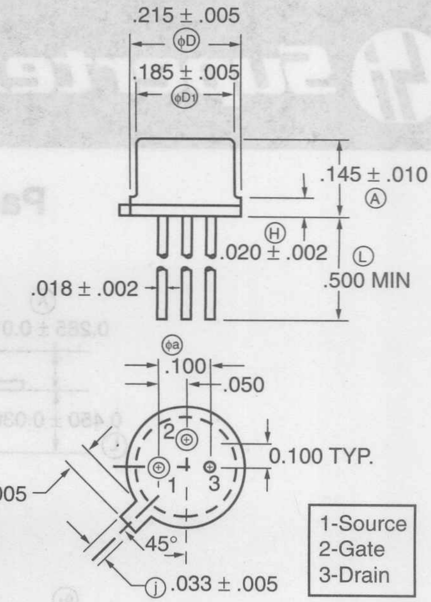
TO-92 Plastic Package
3-Lead

Note: Circle (e.g. B) indicates JEDEC Reference.

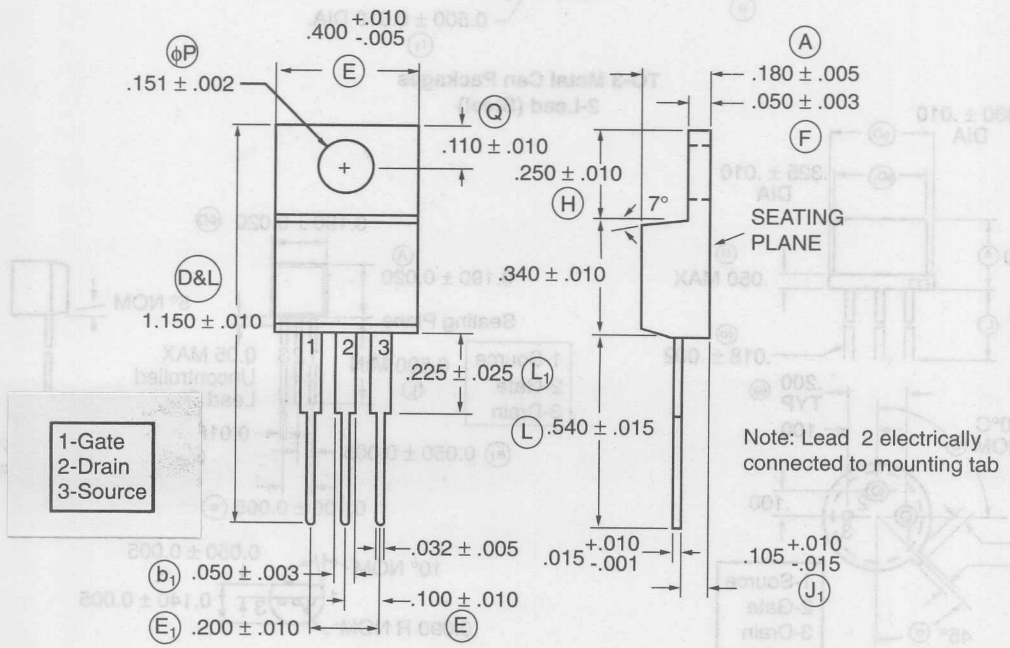


TO-243AA (SOT-89)
Surface Mount

*Pinout for LND150N8 only is:
1-Gate 2-Source 3-Drain

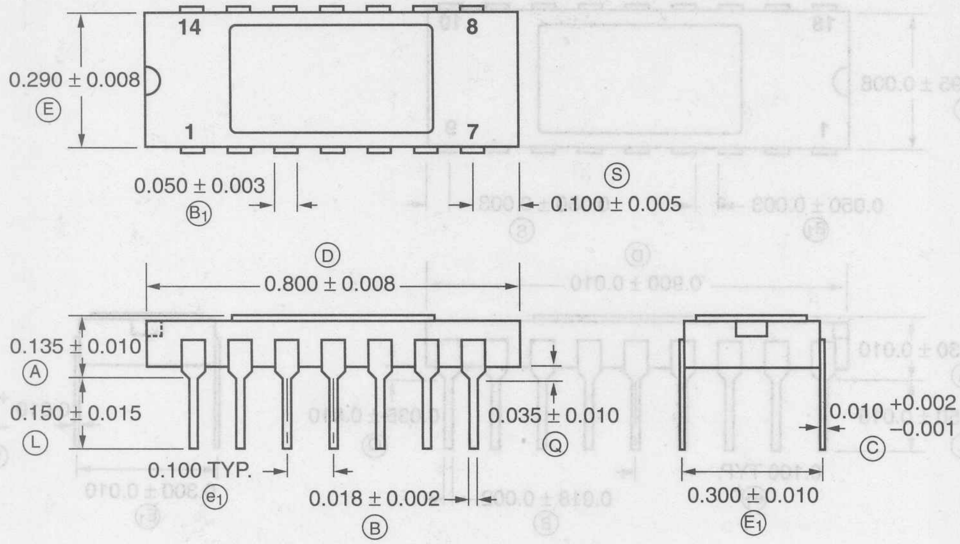


TO-52 Metal Can Package
3-Lead

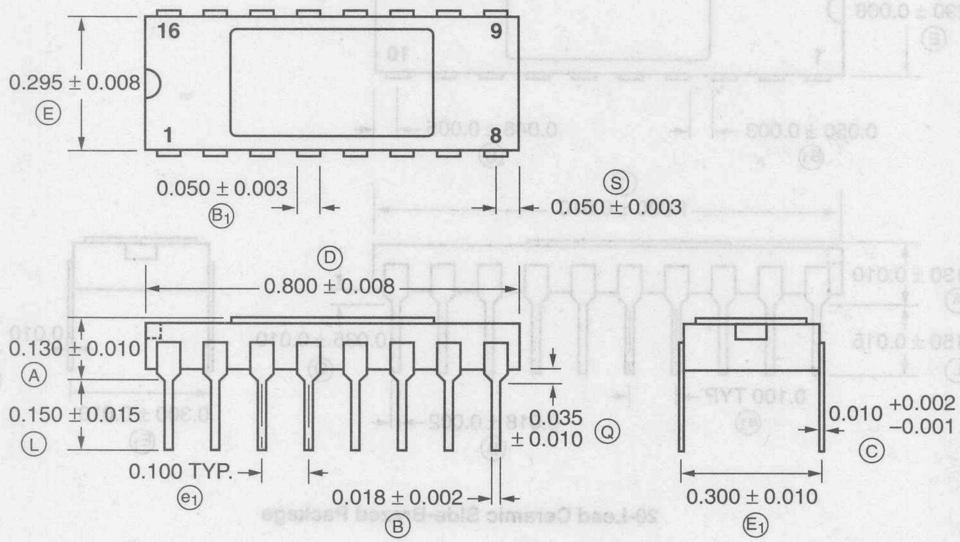


TO-220 Power Package
3-Lead

Note: Circle (e.g. B) indicates JEDEC Reference.

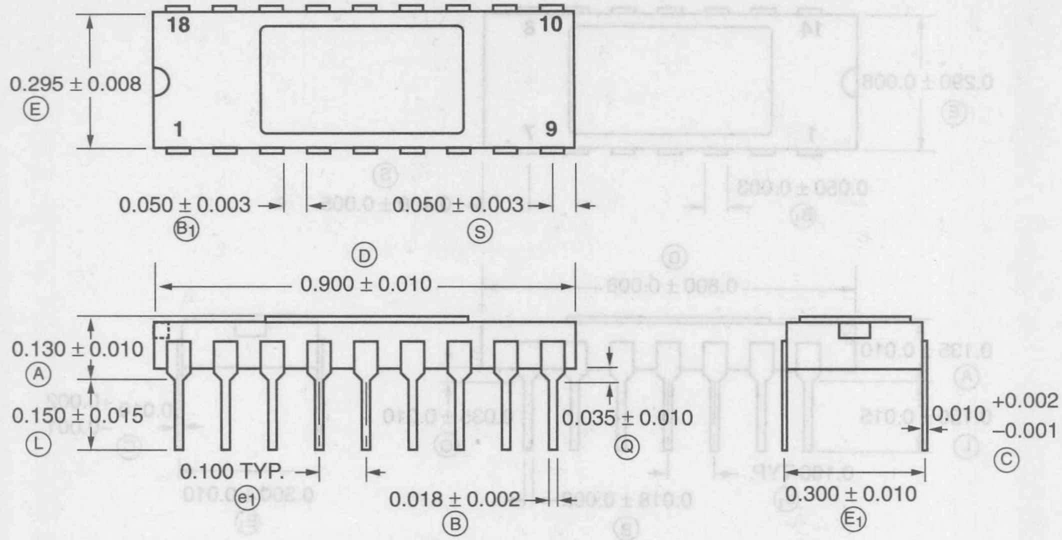


14-Lead Ceramic Side-Brazed Package

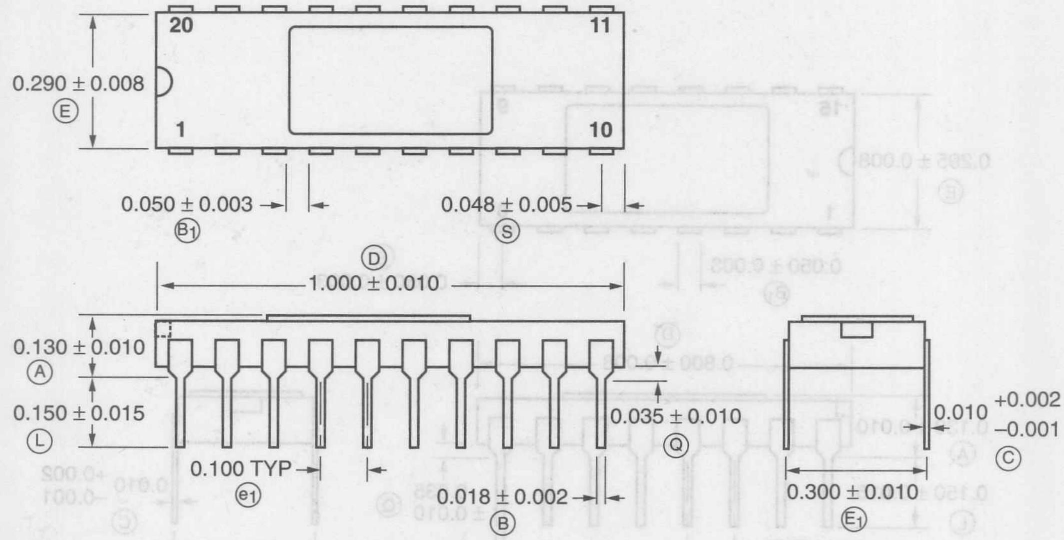


16-Lead Ceramic Side-Brazed Package

Note: Circle (e.g. B) indicates JEDEC Reference.

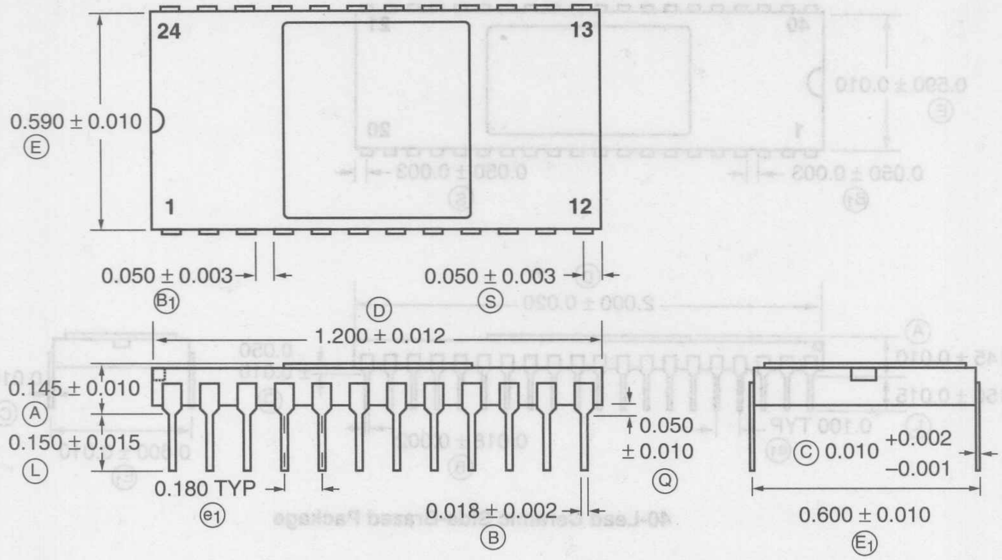


18-Lead Ceramic Side-Brazed Package

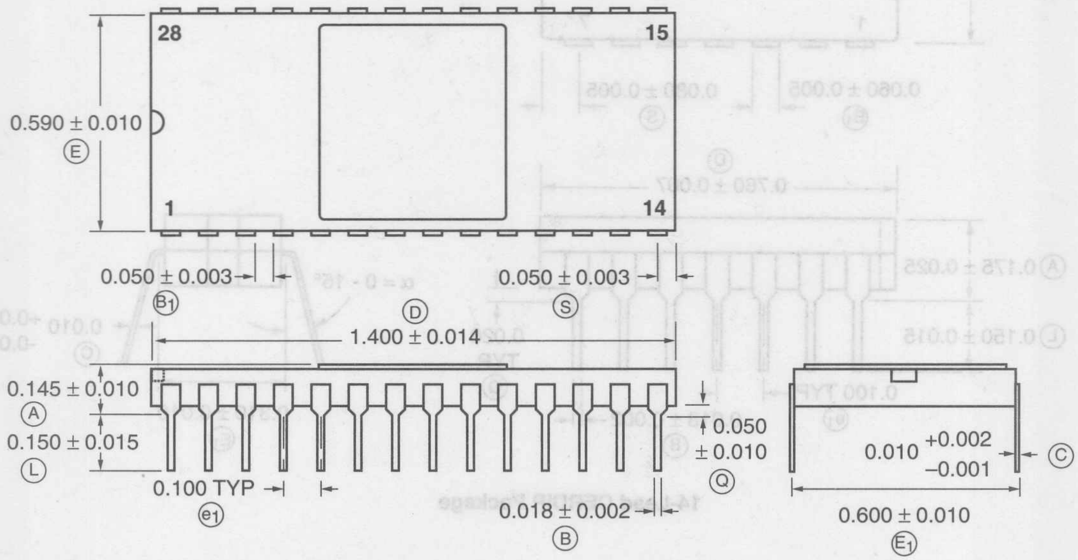


20-Lead Ceramic Side-Brazed Package

Note: Circle (e.g. B) indicates JEDEC Reference.



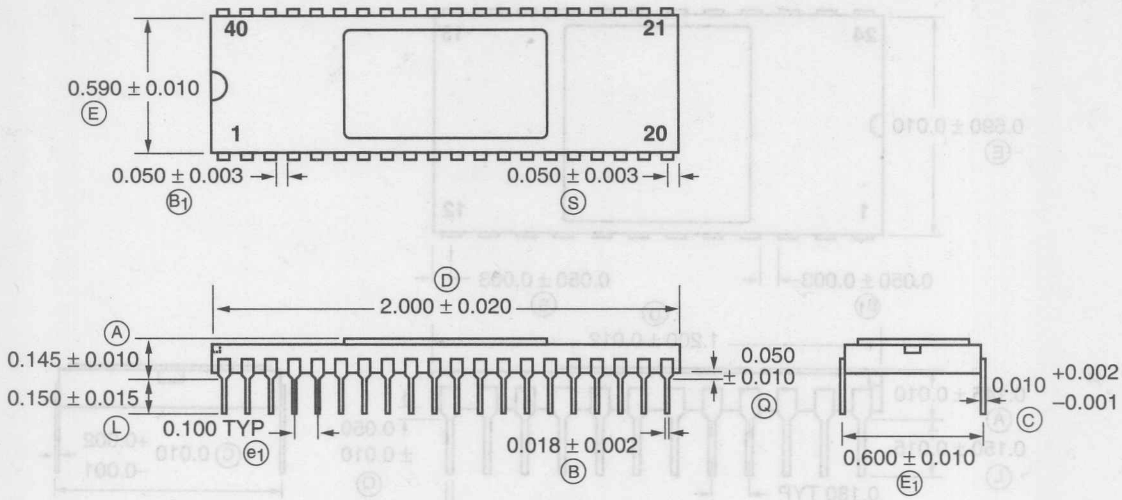
24-Lead Ceramic Side-Brazed Package



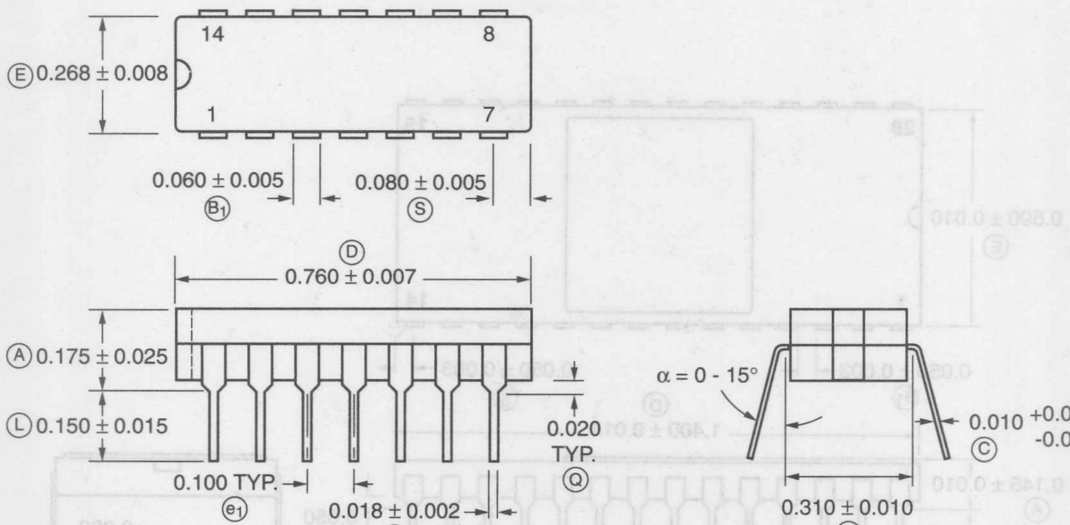
28-Lead Ceramic Side-Brazed Package

16

Note: Circle (e.g. B) indicates JEDEC Reference.

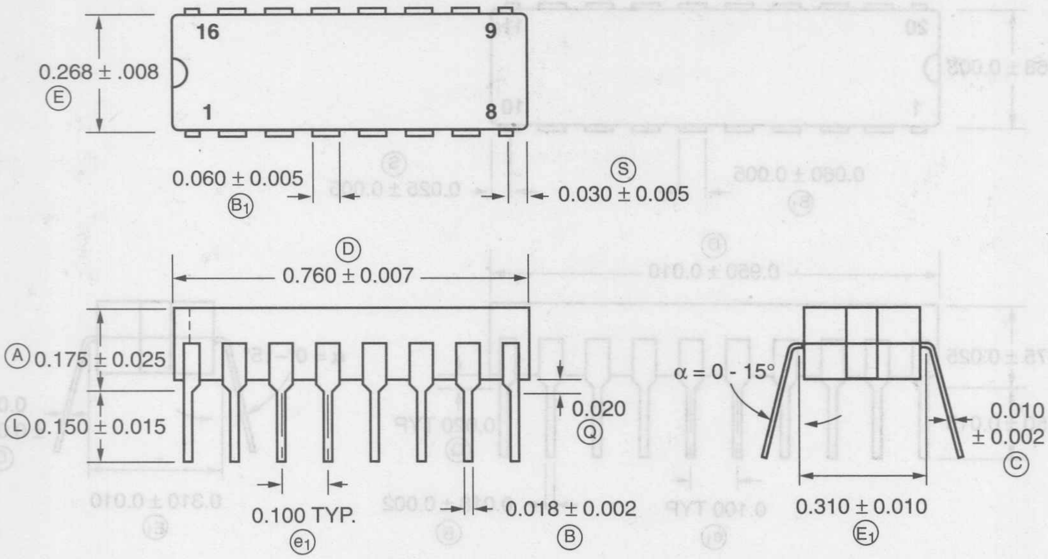


40-Lead Ceramic Side-Brazed Package

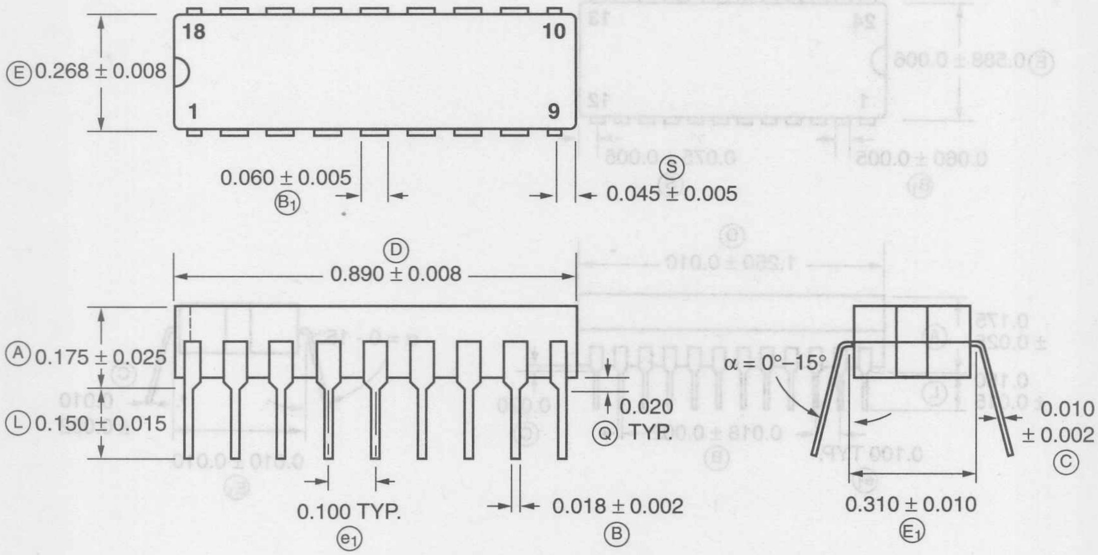


14-Lead CERDIP Package

Note: Circle (e.g. B) indicates JEDEC Reference.



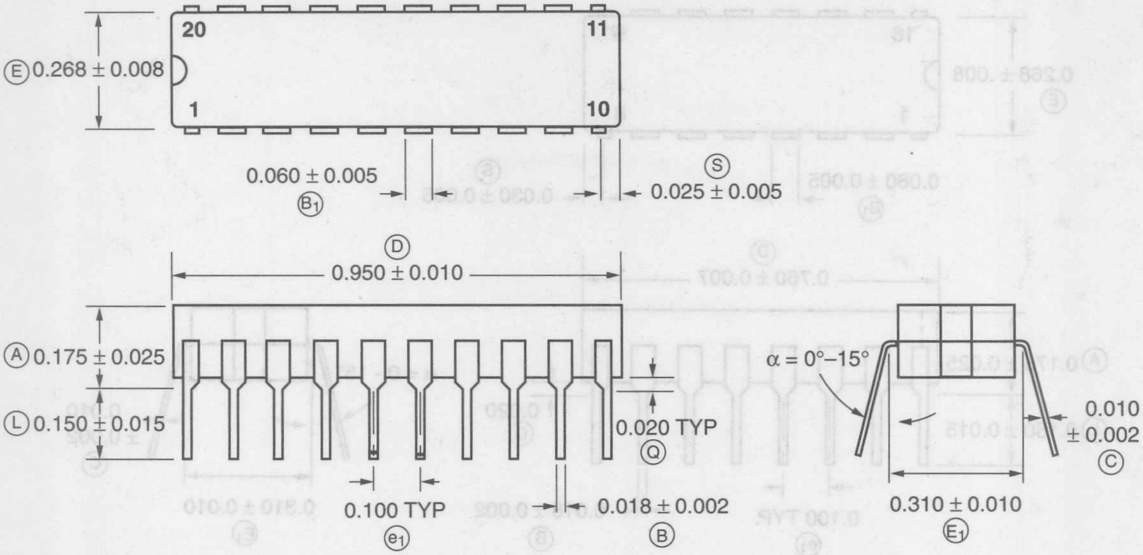
16-Lead CERDIP Package



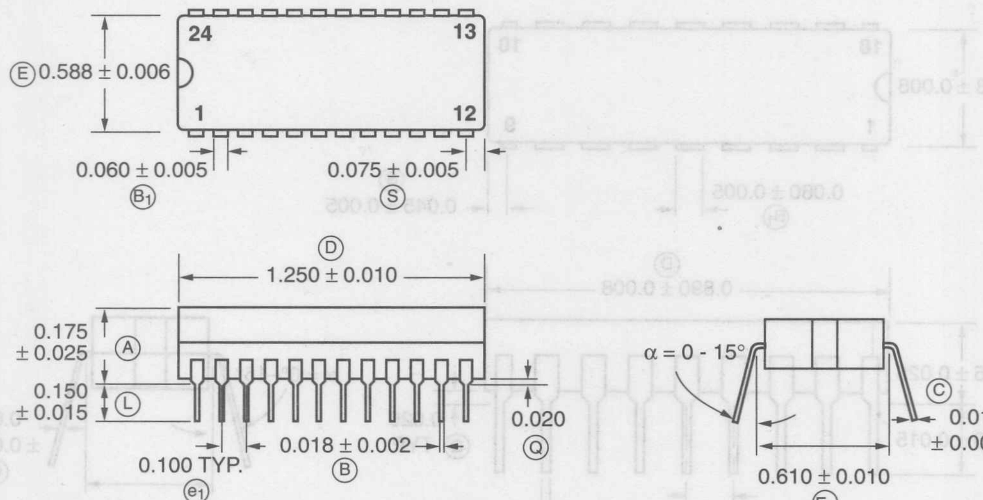
18-Lead CERDIP Package

16

Note: Circle (e.g. B) indicates JEDEC Reference.

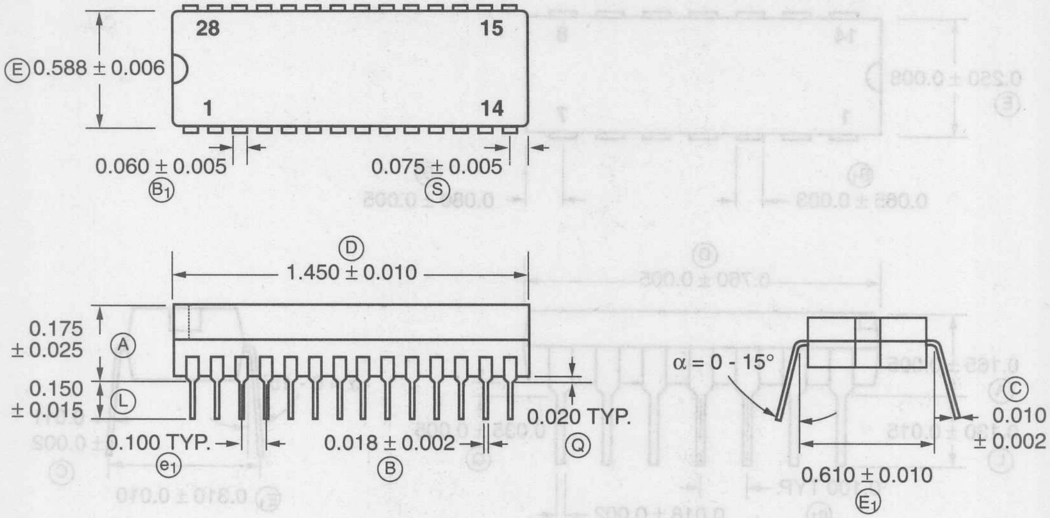


20-Lead CERDIP Package

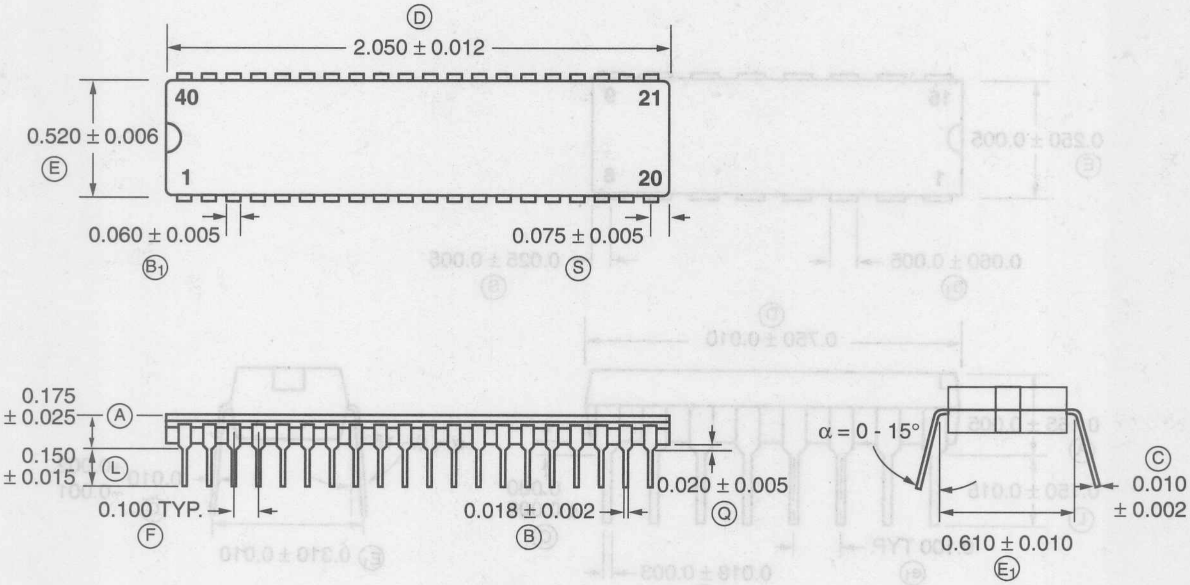


24-Lead CERDIP Package

Note: Circle (e.g. B) indicates JEDEC Reference.



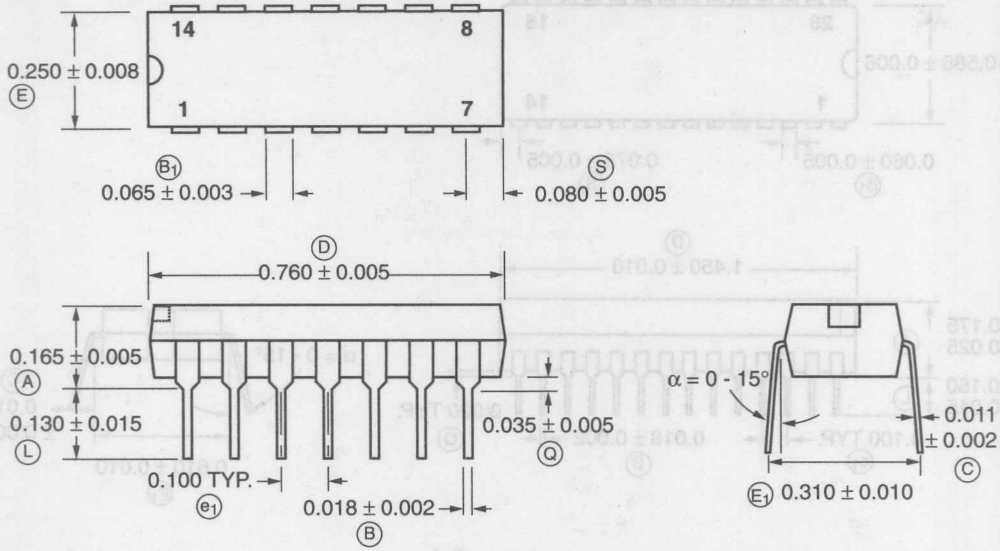
28-Lead CERDIP Package



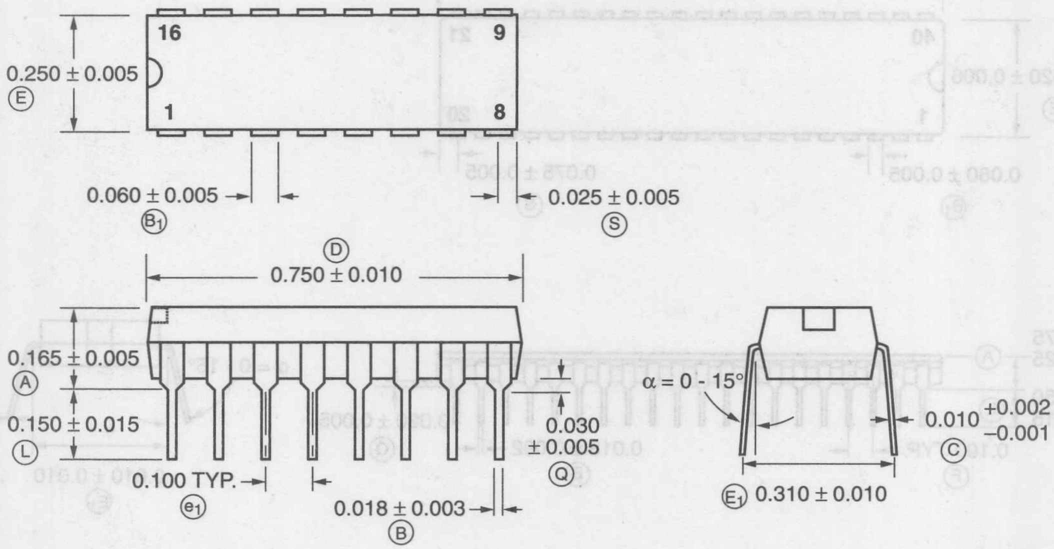
40-Lead CERDIP Package

16

Note: Circle (e.g. B) indicates JEDEC Reference.

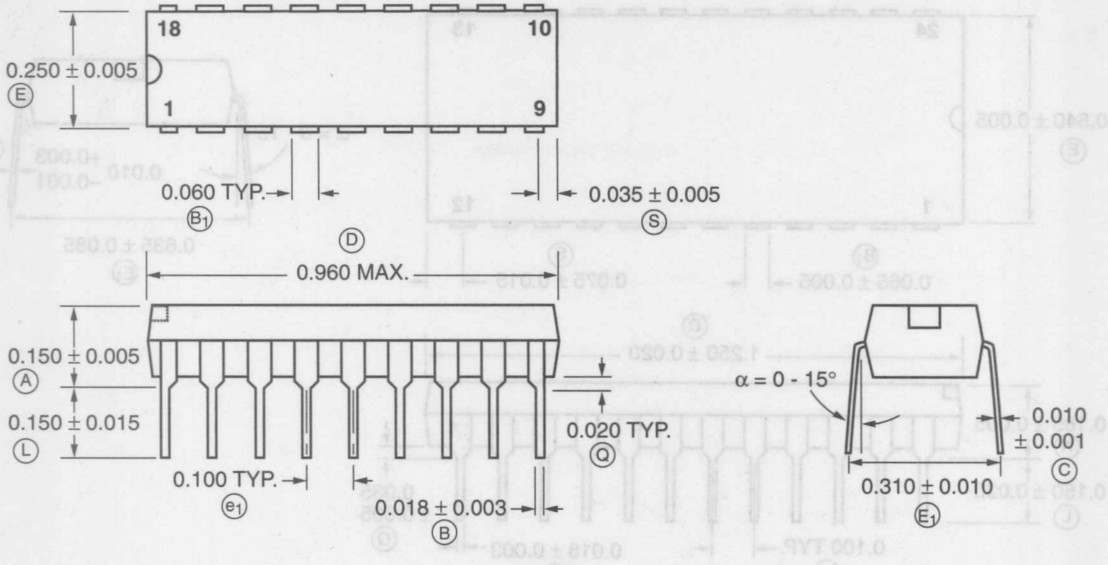


14-Lead Plastic Dual-In-Line Package

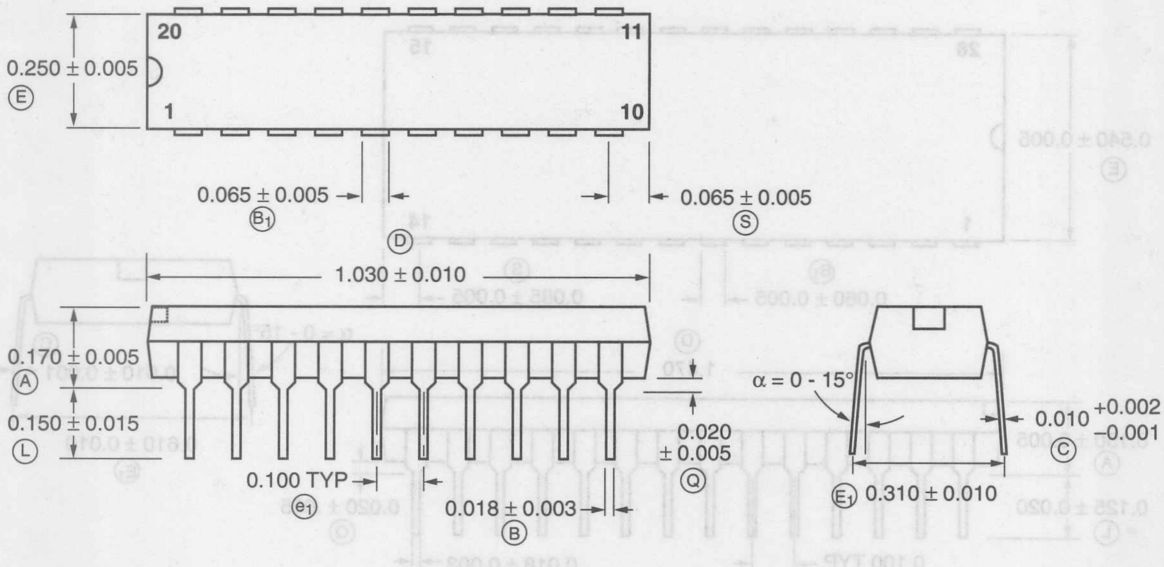


16-Lead Plastic Dual-In-Line Package

Note: Circle (e.g. B) indicates JEDEC Reference.



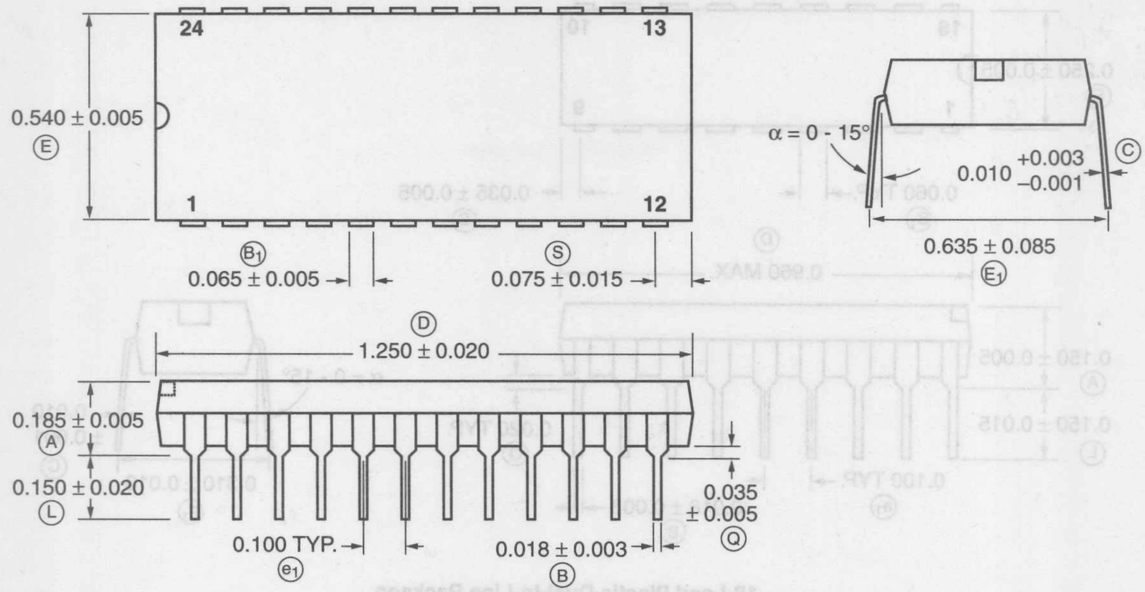
18-Lead Plastic Dual-In-Line Package



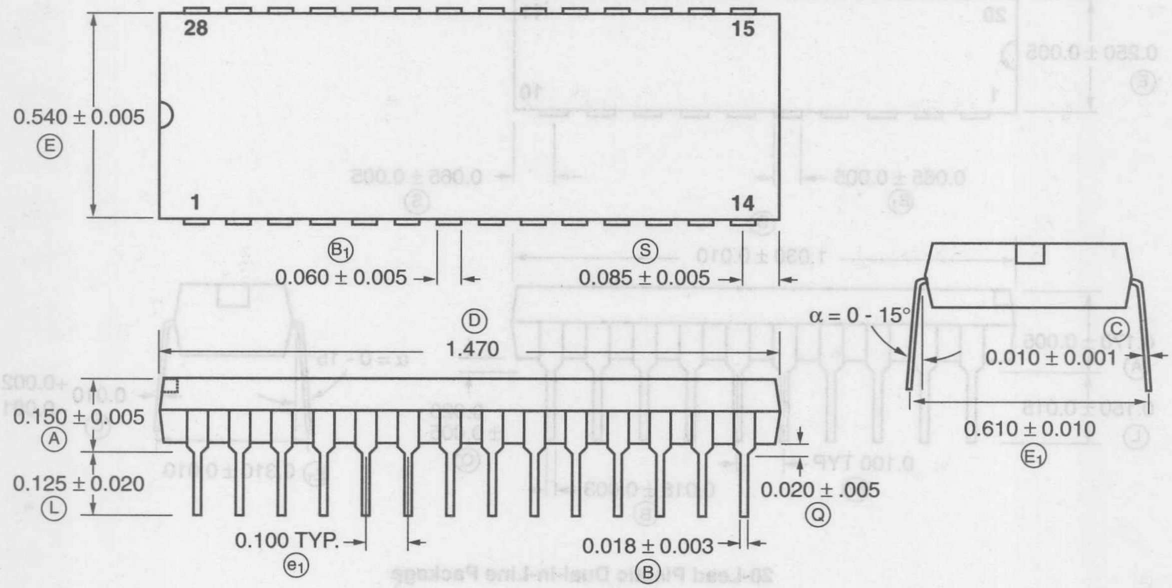
20-Lead Plastic Dual-In-Line Package

16

Note: Circle (e.g. B) indicates JEDEC Reference.

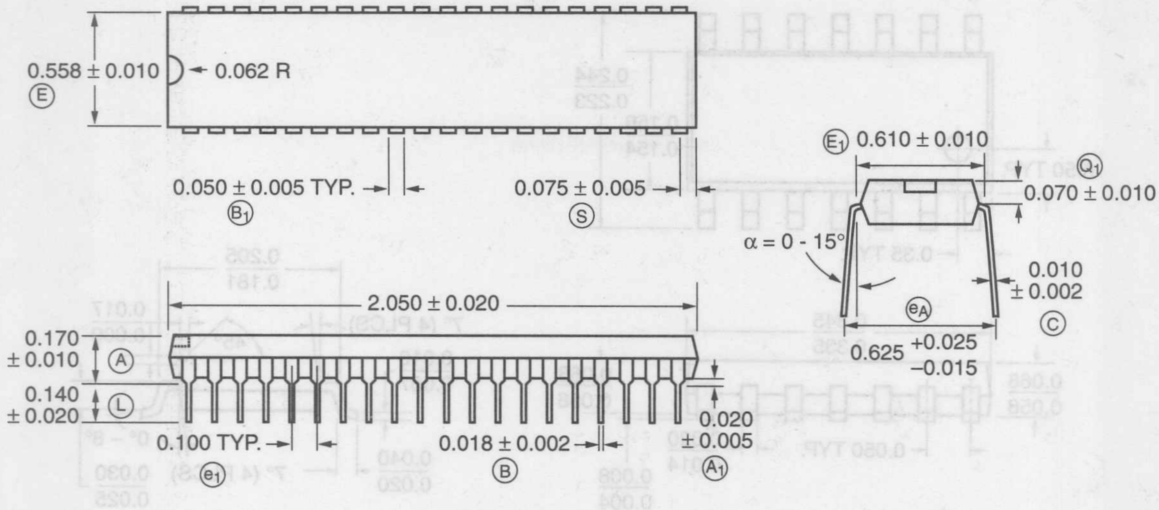


24-Lead Plastic Dual-In-Line Package

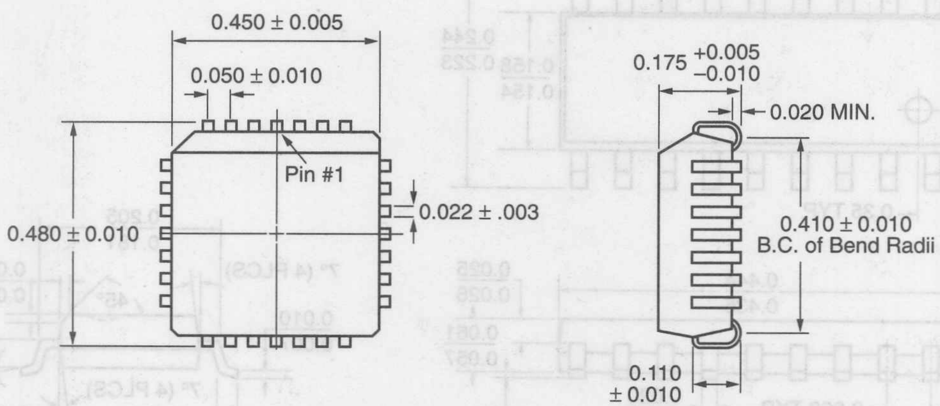


28-Lead Plastic Dual-In-Line Package

Note: Circle (e.g. B) indicates JEDEC Reference.

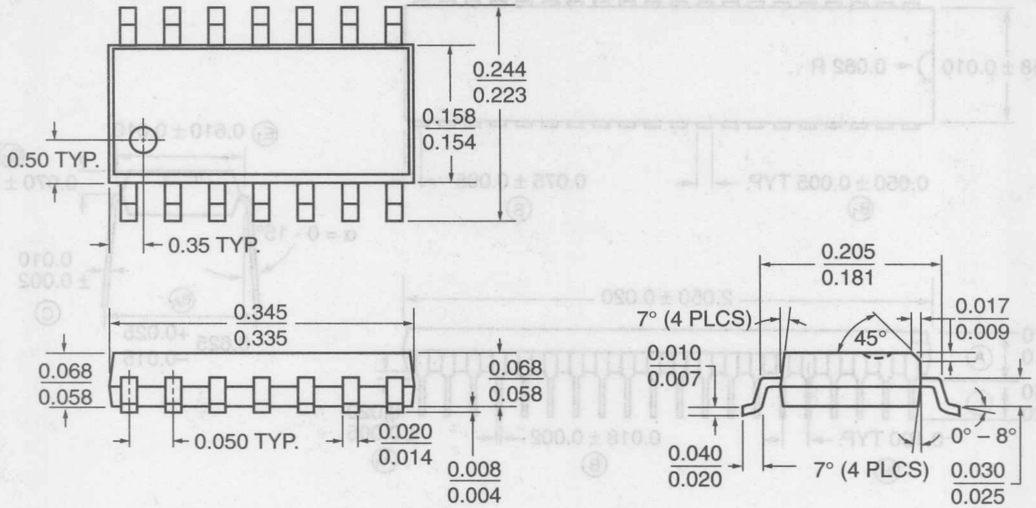


40-Lead Plastic Dual-In-Line Package

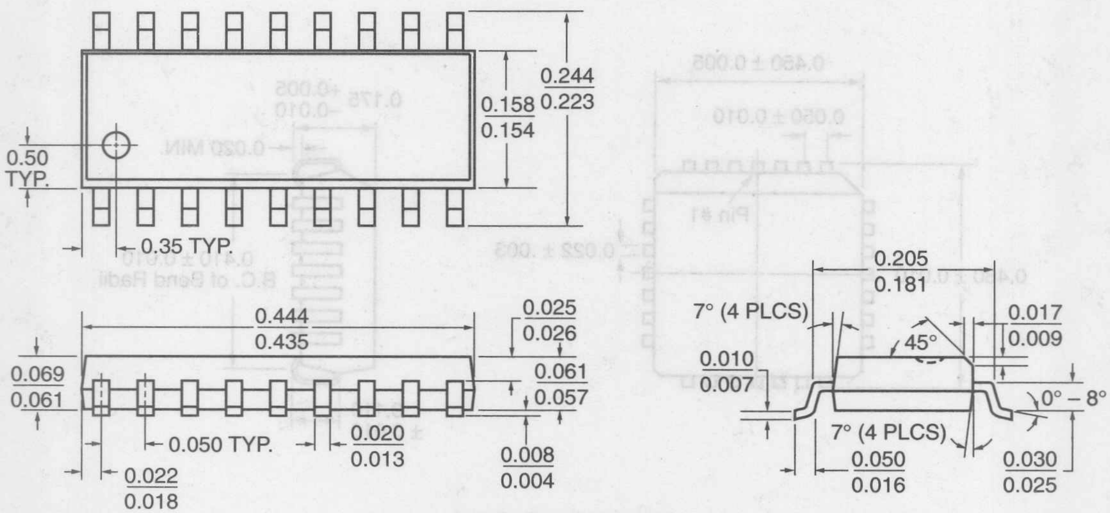


28-Lead Plastic Quad "J" Bend

Note: Circle (e.g. B) indicates JEDEC Reference.

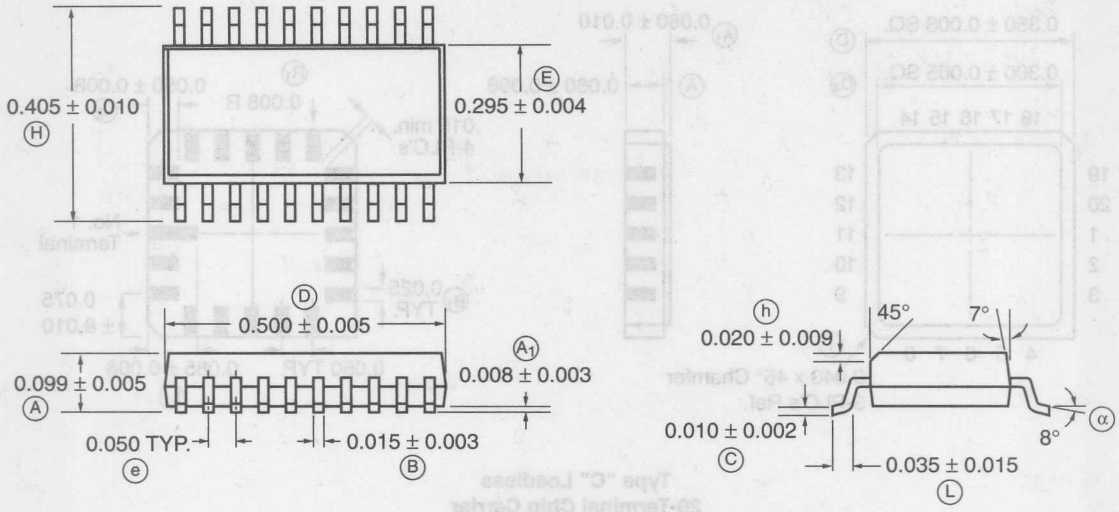


14-Lead SO Package
(Narrow Body)

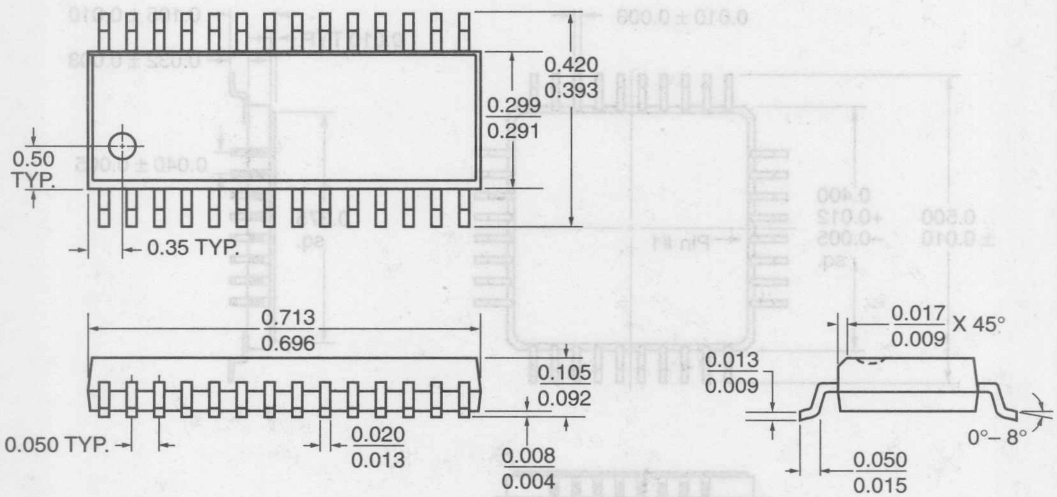


18-Lead SO Package
(Narrow Body)

Note: Circle (e.g. Ⓑ) indicates JEDEC Reference.



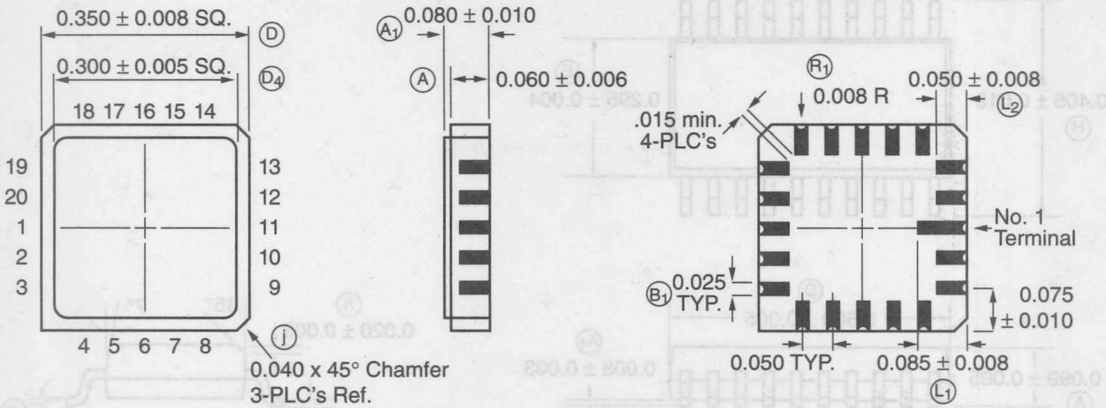
20-Lead SOW Package



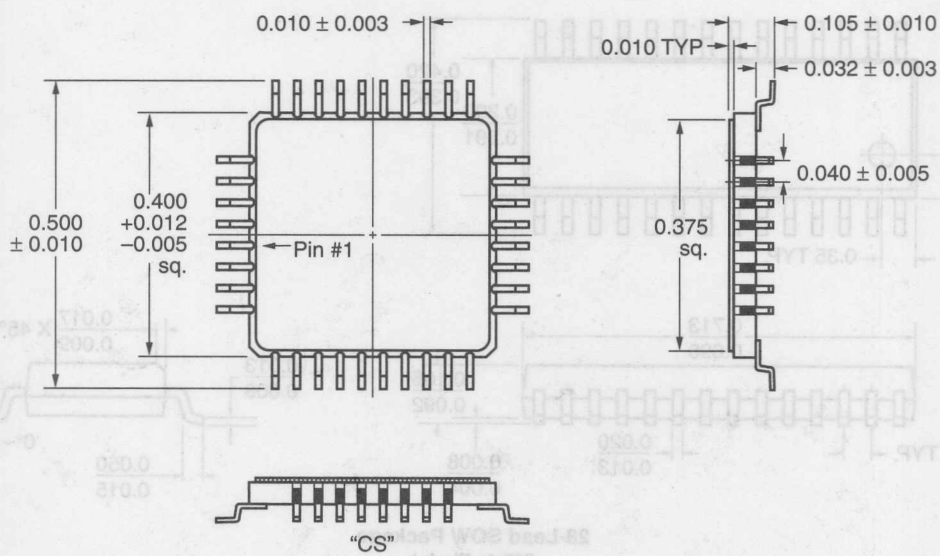
28-Lead SOW Package
(Wide Body)

16

Note: Circle (e.g. B) indicates JEDEC Reference.

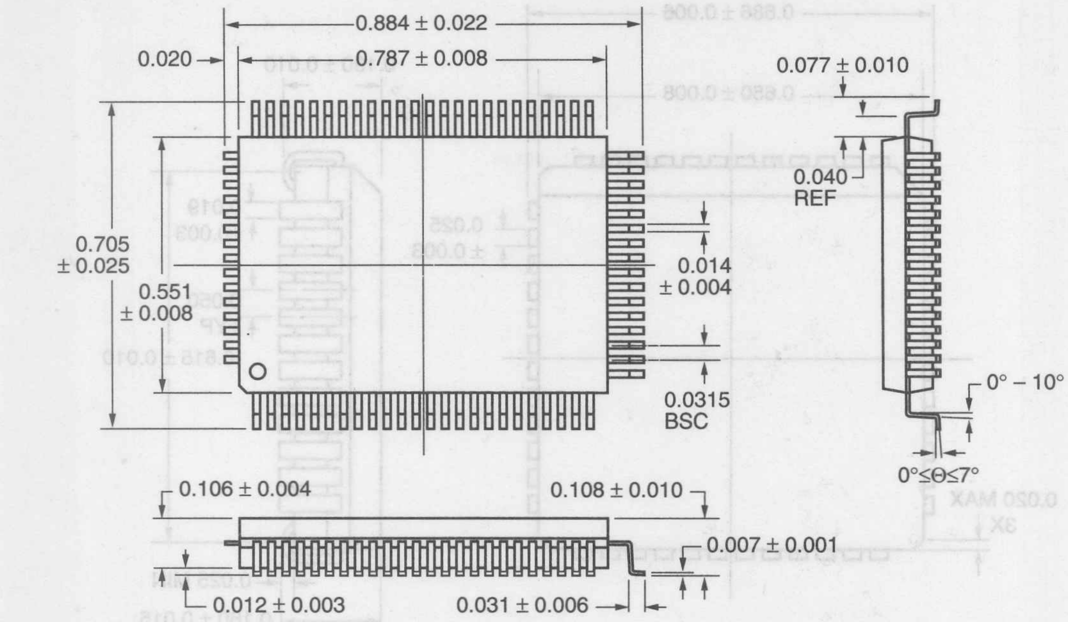


Type "C" Leadless
20-Terminal Chip Carrier

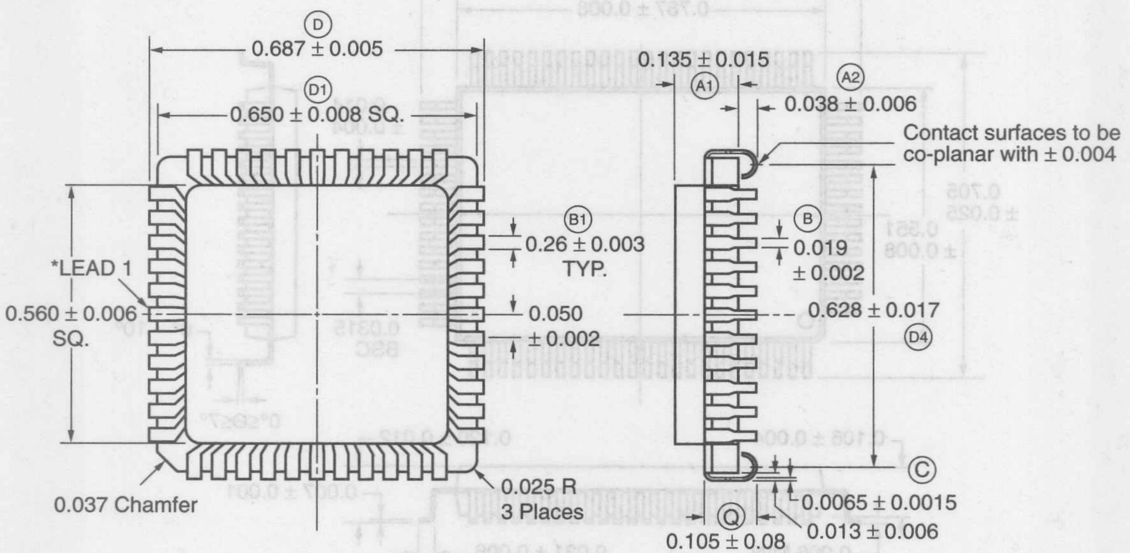


36-Leaded C/C
Bend Option "CS"

Note: Circle (e.g. B) indicates JEDEC Reference.

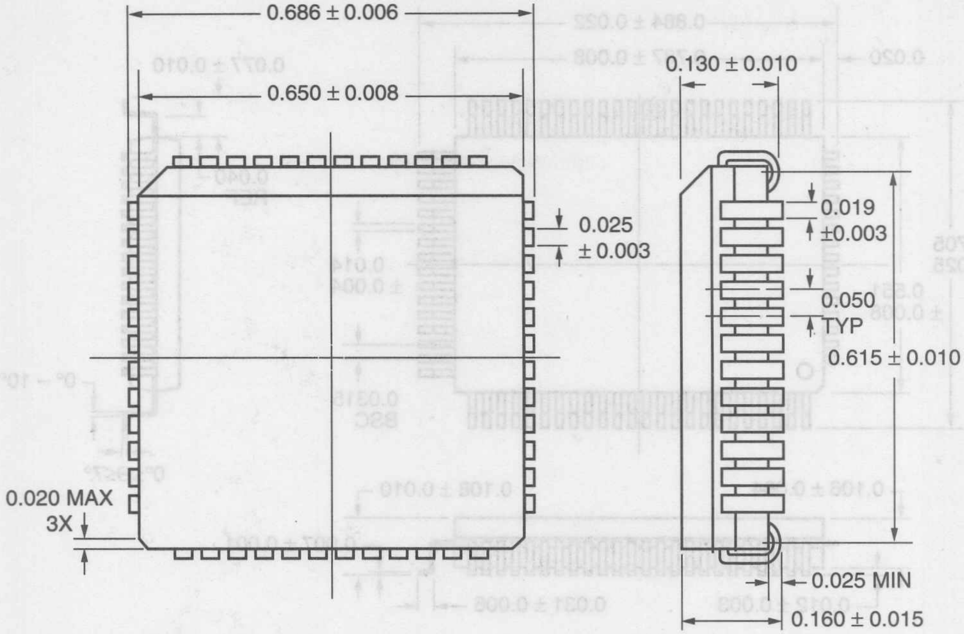


64-Lead 3-Sided Ceramic Quad Flat Package
("Gullwing" Package)

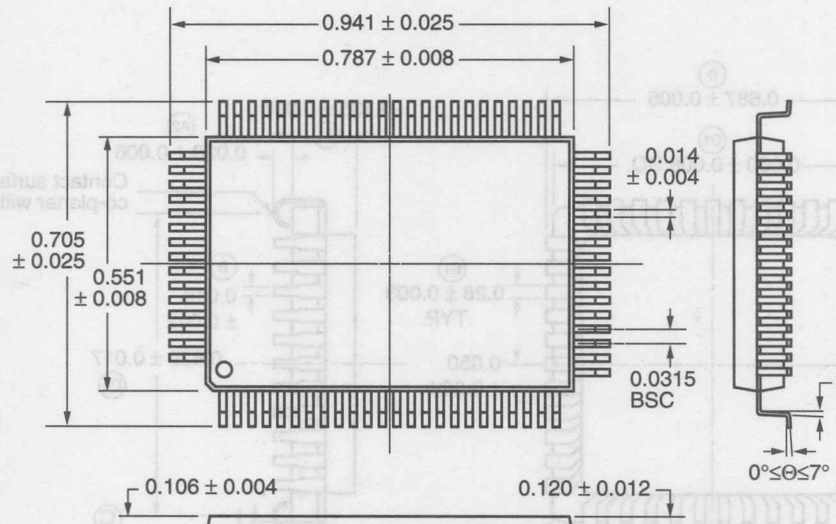


44-Lead Quad CERPAC "DJ" Package
(Gold Leads)

Note: Circle (e.g. B) indicates JEDEC Reference.

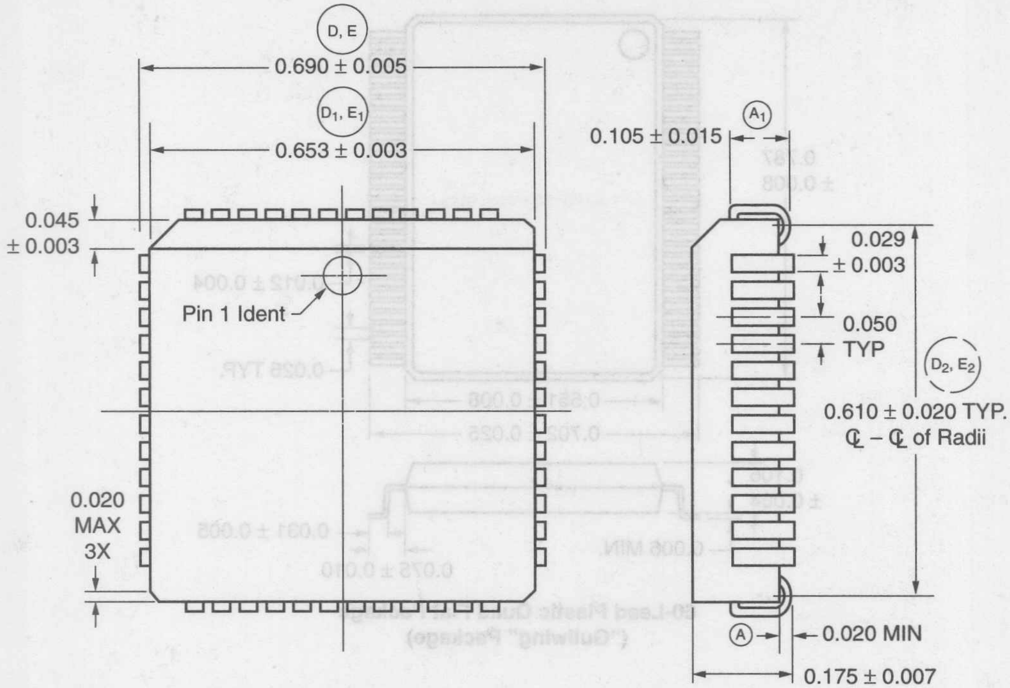


44-Lead Cerpac "J"-Bend M004 Suffix (Solder Dip Leads)

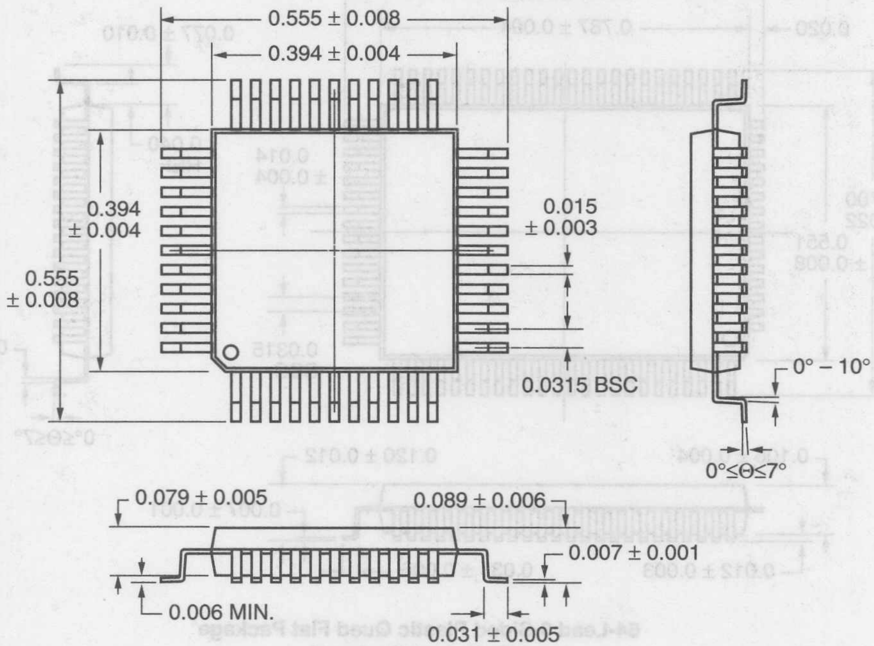


80-Lead Ceramic Quad Flat Package ("Gullwing" Package)

Note: Circle (e.g. B) indicates JEDEC Reference.

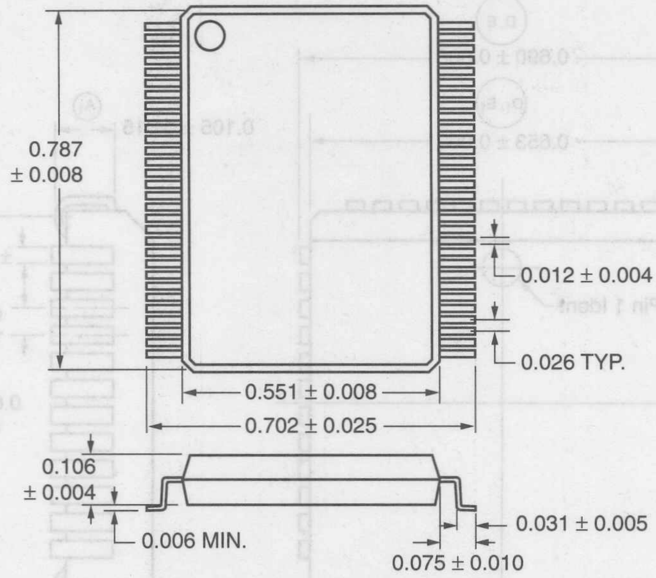


44-Lead Plastic “J” Bend

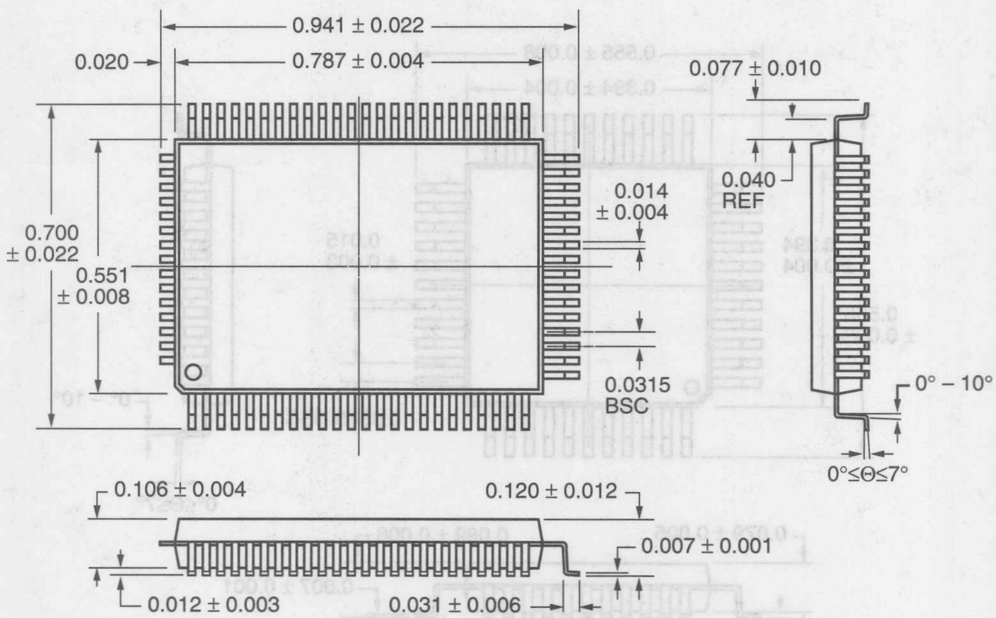


44-Lead Plastic Quad Flat Package
(“Gullwing” Package)

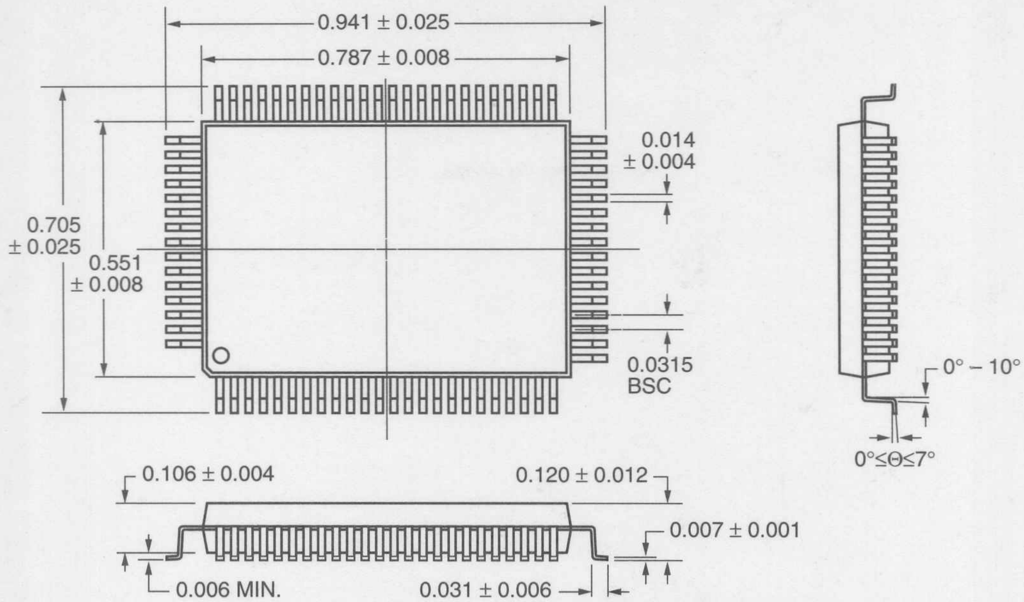
Note: Circle (e.g. B) indicates JEDEC Reference.



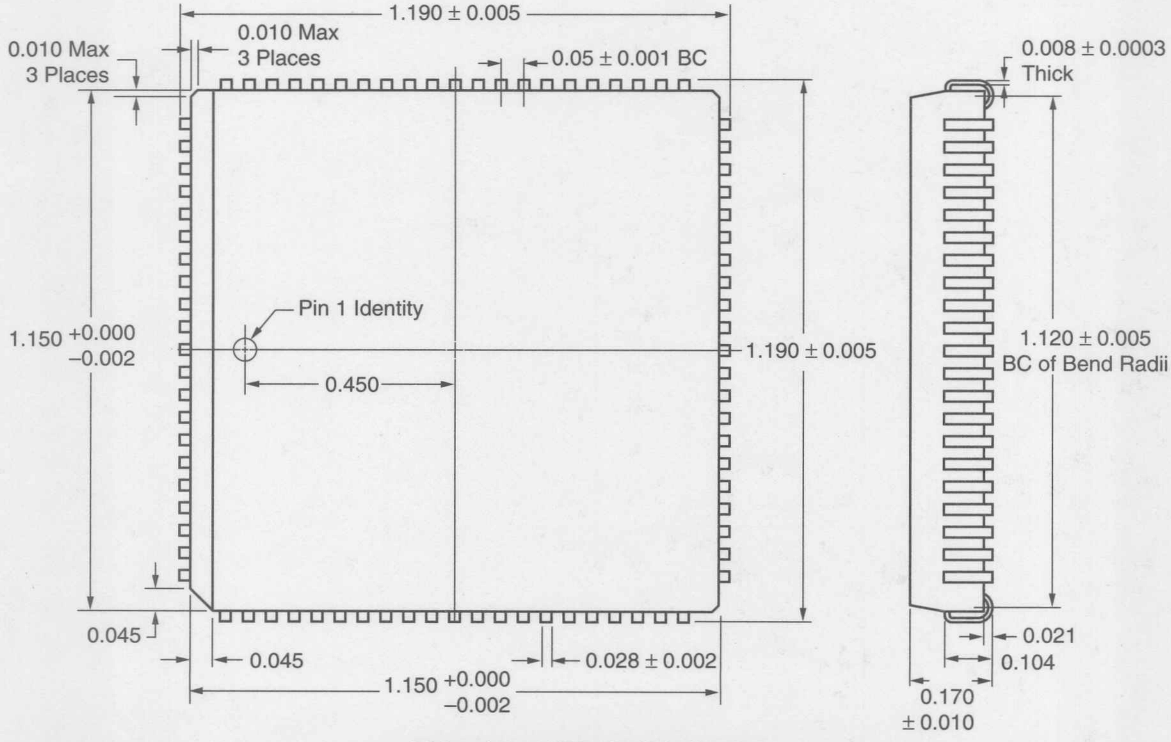
60-Lead Plastic Quad Flat Package
("Gullwing" Package)



64-Lead 3-Sided Plastic Quad Flat Package
("Gullwing" Package)



80-Lead Plastic Quad Flat Package
("Gullwing" Package)



84-Lead Quad Plastic Chip Carrier

16

Chapter 17 – Die Specifications

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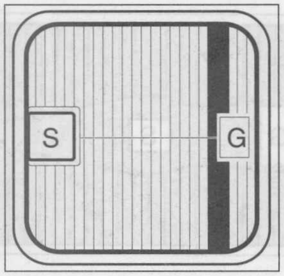
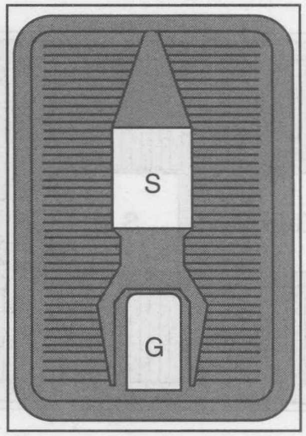
VF01/VF06
VF21/VF25
Die Specifications

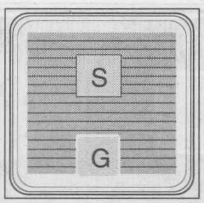
VF01



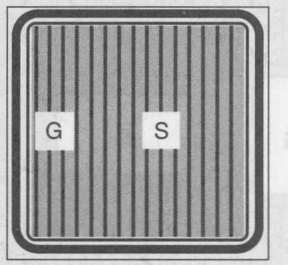
VF06



VF21



VF25



All dimensions in mils.

Die	Dimensions			Backside[2]	Bonding Pads[3]		Recommended Assembly Material		
Geometry	Length[1]	Width	Thickness	Metal	Material	Size	Wire[4]	Wire Size[4]	Preform[5]
VF01	42	42	11 ± 1.5	Au	Al-Cu-Si	5 x 5	Al	1.3	Au - Si Eutectic
VF06	70	50	11 ± 1.5	Au	Al-Cu-Si	8 x 15	Al	1.5	Au - Si Eutectic
VF21	30	30	11 ± 1.5	Au	Al-Cu-Si	6 x 5.5	Al	1.3	Au - Si Eutectic
VF25	45	45	11 ± 1.5	Au	Al-Cu-Si	6.4 x 6.6	Al	1.5	Au - Si Eutectic

Notes:
1. Maximum values
2. Standard Au back is alloyed for optimum eutectic die attach. Ag backing is optional.
3. Al-Cu-Si is used for higher operating current densities. Bond pad size represents smaller gate pad.
4. Bond wire size and material depends on AuTCB, TSB or Al VSB.
5. Soft solder or organic die attach methods may be used with appropriate backmetal option.

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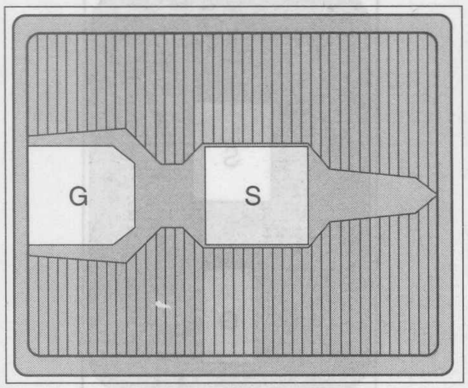
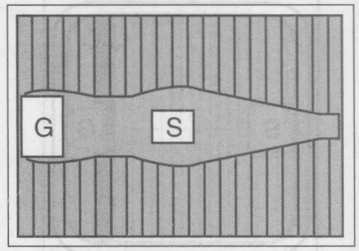
VF03/VF11 VF12/VF22
Die Specifications

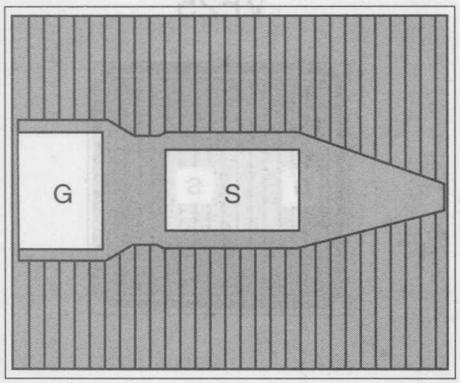
VF03



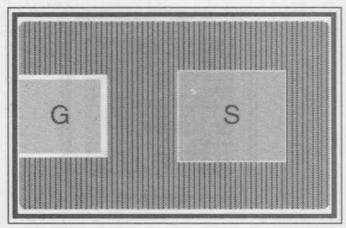
VF11



VF12



VF22

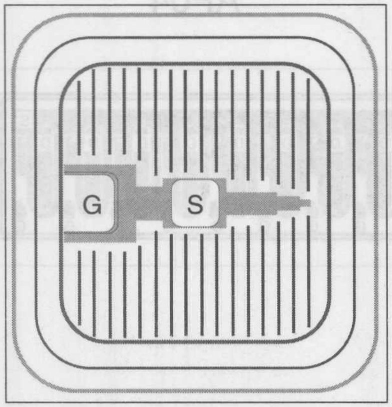


All dimensions in mils.

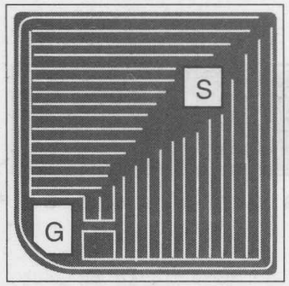
Die Geometry	Dimensions			Backside[2]	Bonding Pads[3]		Recommended Assembly Material		
	Length[1]	Width	Thickness	Metal	Material	Size	Wire[4]	Wire Size[4]	Preform[5]
VF03	146	118	11 ± 1.5	Au	Al-Cu-Si	15 x 20	Al	5	Au-Si Eutectic
VF11	104	70	11 ± 1.5	Au	Al-Cu-Si	17.5 x 11	Al	5	Au-Si Eutectic
VF12	146	118	11 ± 1.5	Au	Al-Cu-Si	40 x 24	Al	5	Au-Si Eutectic
VF22	105	70	11 ± 1.5	Au	Al-Cu-Si	20 x 27	Al	5	Au-Si Eutectic

Notes:
1. Maximum values
2. Standard Au back is alloyed for optimum eutectic die attach. Ag backing is optional.
3. Al-Cu-Si is used for higher operating current densities. Bond pad size represents smaller gate pad.
4. Bond wire size and material depends on AuTCB, TSB or Al VSB.
5. Soft solder or organic die attach methods may be used with appropriate backmetal option.

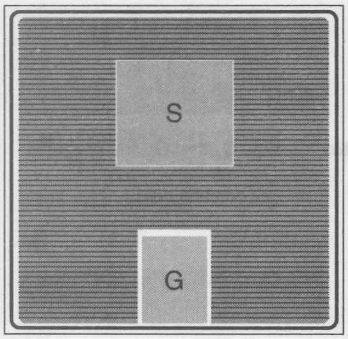
VF05



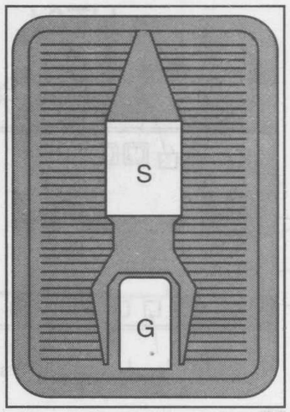
VF13



VF26



TN07

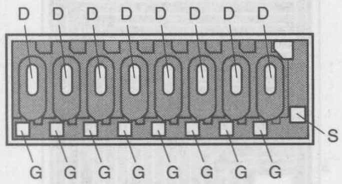


All dimensions in mils.

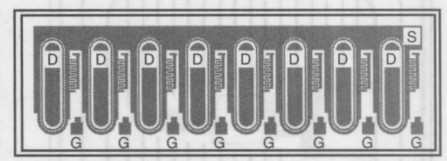
Die Geometry	Dimensions			Backside[2] Metal	Bonding Pads[3]		Recommended Assembly Material		
	Length[1]	Width	Thickness		Material	Size	Wire[4]	Wire Size[4]	Preform[5]
VF05	43	41	11 ± 1.5	Au	Al-Cu-Si	5 x 5	Al	1.3	Au-Si Eutectic
VF13	30	30	11 ± 1.5	Au	Al-Cu-Si	4 x 4	Al	1.3	Au-Si Eutectic
VF26	70	70	11 ± 1.5	Au	Al-Cu-Si	4 x 6.25	Al	1.5	Au-Si Entectic
TN07	50	70	11 ± 1.5	Au	Al-Cu-Si	8 x 15	Al	1.5	Au-Si Eutectic

Notes:
1. Maximum values
2. Standard Au back is alloyed for optimum eutectic die attach. Ag backing is optional.
3. Al-Cu-Si is used for higher operating current densities. Bond pad size represents smaller gate pad.
4. Bond wire size and material depends on AuTCB, TSB or Al VSB.
5. Soft solder or organic die attach methods may be used with appropriate backmetal option.

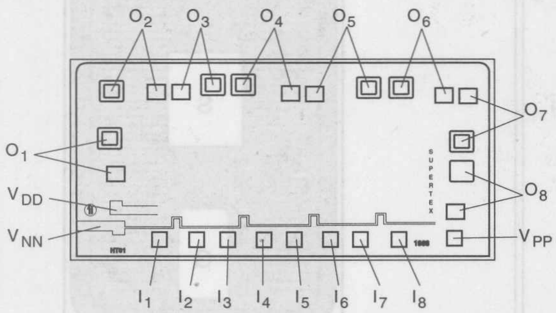
AF01



AF04



HT01



Note: Outputs O_2 thru O_8 each require two (2) wire bonds connected off-chip, as shown.

All dimensions in mils.

Die Geometry	Dimensions			Backside Metal	Bonding Pads		Recommended Assembly Material		
	Length	Width[1]	Thickness		Material	Size[2]	Wire[3]	Wire Size[3]	Preform
AF01	36	97	21 ± 1.5	None	Al-Si	4 x 4	Al	1.25	Epoxy
AF04[3]	48	146	21 ± 1.5	None	Al-Si	4 x 4	Al	1.25	Epoxy
HT01	68	136	21 ± 1.5	None	Al-Si	4 x 4	Al	1.25	Epoxy

Notes:
1. Maximum values
2. Bond pad size represents smallest pad.
3. Bond wire size and material depends on Au TCB, TSB or Al USB.
4. Preliminary information for AF04

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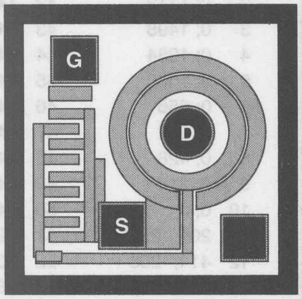
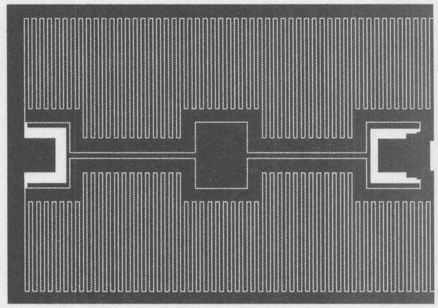
LND1/LP07

Die Specifications

LND1



LP07



All dimensions in mils.

Die Geometry	Dimensions			Backside[2] Metal	Bonding Pads		Recommended Assembly Material		
	Length[1]	Width	Thickness		Material	Size	Wire[4]	Wire Size[4]	Preform[5]
LND1	30	30	20 ± 1.5	None	Al-Si	3.8 x 3.8	Au	1.0	Epoxy
LP07	50	70	11 ± 1.5	None	Al-Si	4.7 x 4.7	Al	1.5	Epoxy

Notes:
1. Maximum values
2. Au or Ag backing is optional.
3. Bond pad size represents smaller gate pad.
4. Bond wire size and material depends on AuTCB, TSB or Al VSB.
5. Soft solder or organic die attach methods may be used with appropriate backmetal option.

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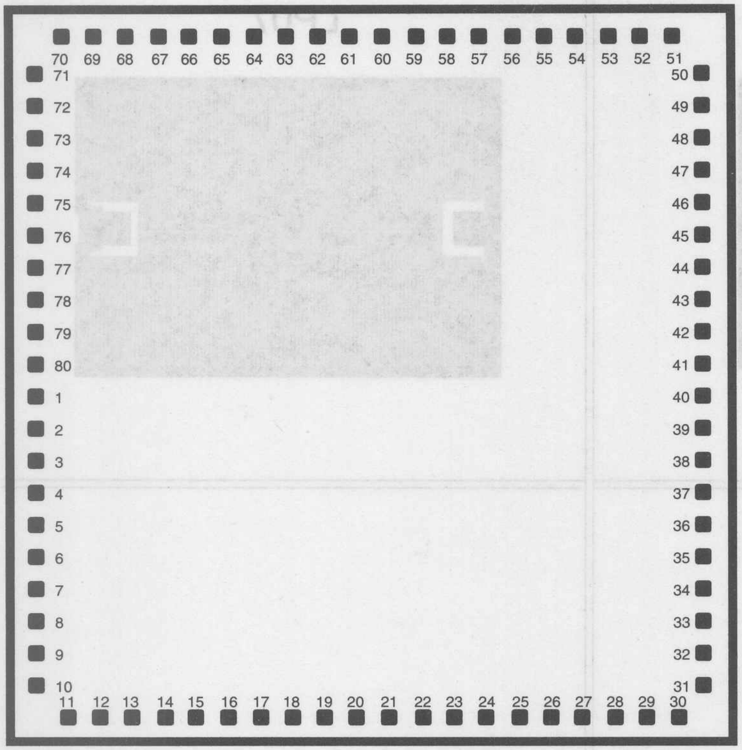
Die Specifications



Pad Coordinates in Microns

1	0; 1926	41	4448; 2158
2	0; 1712	42	4448; 2372
3	0; 1498	43	4448; 2586
4	0; 1284	44	4448; 2800
5	0; 1070	45	4448; 3014
6	0; 856	46	4448; 3228
7	0; 642	47	4448; 3442
8	0; 428	48	4448; 3656
9	0; 214	49	4448; 3870
10	0; 0	50	4448; 4084
11	200; -255	51	4248; 4339
12	414; -255	52	4034; 4339
13	628; -255	53	3820; 4339
14	842; -255	54	3606; 4339
15	1056; -255	55	3392; 4339
16	1270; -255	56	3178; 4339
17	1484; -255	57	2964; 4339
18	1698; -255	58	2750; 4339
19	1912; -255	59	2536; 4339
20	2126; -255	60	2322; 4339
21	2340; -255	61	2108; 4339
22	2554; -255	62	1894; 4339
23	2768; -255	63	1680; 4339
24	2982; -255	64	1466; 4339
25	3196; -255	65	1252; 4339
26	3410; -255	66	1038; 4339
27	3624; -255	67	824; 4333
28	3838; -255	68	610; 4339
29	4052; -255	69	396; 4333
30	4266; -255	70	182; 4339
31	4448; 0	71	0; 4084
32	4448; 214	72	0; 3870
33	4448; 446	73	0; 3638
34	4448; 660	74	0; 3424
35	4448; 874	75	0; 3210
36	4448; 1088	76	0; 2996
37	4448; 1302	77	0; 2782
38	4448; 1516	78	0; 2588
39	4448; 1730	79	0; 2354
40	4448; 1944	80	0; 2140

Die Specifications

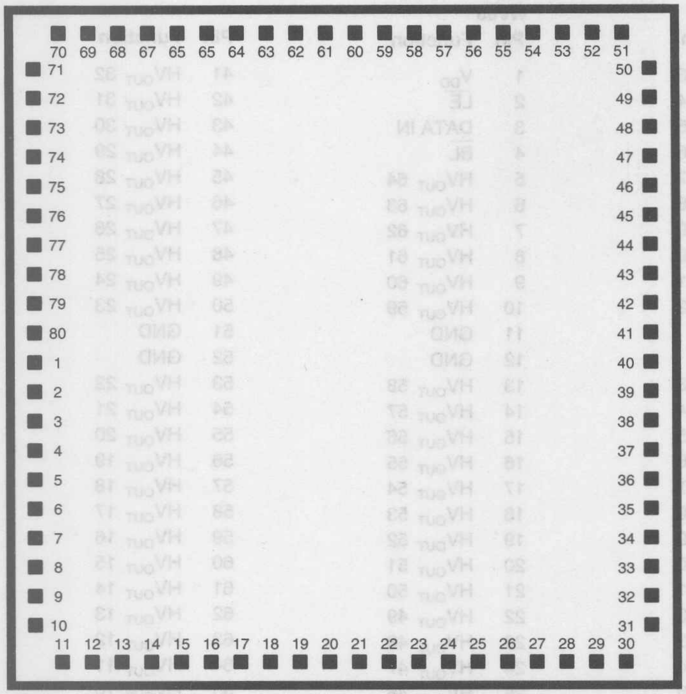
	mils	mm		
Die Size:	190 x 196	4.820 x 4.970	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV03

Pin	Function	Pin	Function
1	V_{DD}	41	HV_{OUT} 33
2	$\overline{LE}$	42	HV_{OUT} 34
3	DATA IN	43	HV_{OUT} 35
4	$\overline{BL}$	44	HV_{OUT} 36
5	HV_{OUT} 1	45	HV_{OUT} 37
6	HV_{OUT} 2	46	HV_{OUT} 38
7	HV_{OUT} 3	47	HV_{OUT} 39
8	HV_{OUT} 4	48	HV_{OUT} 40
9	HV_{OUT} 5	49	HV_{OUT} 41
10	HV_{OUT} 6	50	HV_{OUT} 42
11	GND	51	GND
12	GND	52	GND
13	HV_{OUT} 7	53	HV_{OUT} 43
14	HV_{OUT} 8	54	HV_{OUT} 44
15	HV_{OUT} 9	55	HV_{OUT} 45
16	HV_{OUT} 10	56	HV_{OUT} 46
17	HV_{OUT} 11	57	HV_{OUT} 47
18	HV_{OUT} 12	58	HV_{OUT} 48
19	HV_{OUT} 13	59	HV_{OUT} 49
20	HV_{OUT} 14	60	HV_{OUT} 50
21	HV_{OUT} 15	61	HV_{OUT} 51
22	HV_{OUT} 16	62	HV_{OUT} 52
23	HV_{OUT} 17	63	HV_{OUT} 53
24	HV_{OUT} 18	64	HV_{OUT} 54
25	HV_{OUT} 19	65	HV_{OUT} 55
26	HV_{OUT} 20	66	HV_{OUT} 56
27	HV_{OUT} 21	67	HV_{OUT} 57
28	HV_{OUT} 22	68	HV_{OUT} 58
29	GND	69	GND
30	GND	70	GND
31	HV_{OUT} 23	71	HV_{OUT} 59
32	HV_{OUT} 24	72	HV_{OUT} 60
33	HV_{OUT} 25	73	HV_{OUT} 61
34	HV_{OUT} 26	74	HV_{OUT} 62
35	HV_{OUT} 27	75	HV_{OUT} 63
36	HV_{OUT} 28	76	HV_{OUT} 64
37	HV_{OUT} 29	77	$\overline{POL}$
38	HV_{OUT} 30	78	DATA OUT
39	HV_{OUT} 31	79	CLK
40	HV_{OUT} 32	80	GND

HV05

Pin	Function	Pin	Function
1	V_{DD}	41	HV_{OUT} 32
2	$\overline{LE}$	42	HV_{OUT} 31
3	DATA IN	43	HV_{OUT} 30
4	$\overline{BL}$	44	HV_{OUT} 29
5	HV_{OUT} 64	45	HV_{OUT} 28
6	HV_{OUT} 63	46	HV_{OUT} 27
7	HV_{OUT} 62	47	HV_{OUT} 26
8	HV_{OUT} 61	48	HV_{OUT} 25
9	HV_{OUT} 60	49	HV_{OUT} 24
10	HV_{OUT} 59	50	HV_{OUT} 23
11	GND	51	GND
12	GND	52	GND
13	HV_{OUT} 58	53	HV_{OUT} 22
14	HV_{OUT} 57	54	HV_{OUT} 21
15	HV_{OUT} 56	55	HV_{OUT} 20
16	HV_{OUT} 55	56	HV_{OUT} 19
17	HV_{OUT} 54	57	HV_{OUT} 18
18	HV_{OUT} 53	58	HV_{OUT} 17
19	HV_{OUT} 52	59	HV_{OUT} 16
20	HV_{OUT} 51	60	HV_{OUT} 15
21	HV_{OUT} 50	61	HV_{OUT} 14
22	HV_{OUT} 49	62	HV_{OUT} 13
23	HV_{OUT} 48	63	HV_{OUT} 12
24	HV_{OUT} 47	64	HV_{OUT} 11
25	HV_{OUT} 46	65	HV_{OUT} 10
26	HV_{OUT} 45	66	HV_{OUT} 9
27	HV_{OUT} 44	67	HV_{OUT} 8
28	HV_{OUT} 43	68	HV_{OUT} 7
29	GND	69	GND
30	GND	70	GND
31	HV_{OUT} 42	71	HV_{OUT} 6
32	HV_{OUT} 41	72	HV_{OUT} 5
33	HV_{OUT} 40	73	HV_{OUT} 4
34	HV_{OUT} 39	74	HV_{OUT} 3
35	HV_{OUT} 38	75	HV_{OUT} 2
36	HV_{OUT} 37	76	HV_{OUT} 1
37	HV_{OUT} 36	77	$\overline{POL}$
38	HV_{OUT} 35	78	DATA OUT
39	HV_{OUT} 34	79	CLK
40	HV_{OUT} 33	80	GND



Pad Coordinates in Microns

1	0; 1926	41	4448; 2158
2	0; 1712	42	4448; 2372
3	0; 1498	43	4448; 2586
4	0; 1284	44	4448; 2800
5	0; 1070	45	4448; 3014
6	0; 856	46	4448; 3228
7	0; 642	47	4448; 3442
8	0; 428	48	4448; 3656
9	0; 214	49	4448; 3870
10	0; 0	50	4448; 4084
11	200; -255	51	4248; 4339
12	414; -255	52	4034; 4339
13	628; -255	53	3820; 4339
14	842; -255	54	3606; 4339
15	1056; -255	55	3392; 4339
16	1270; -255	56	3178; 4339
17	1484; -255	57	2964; 4339
18	1698; -255	58	2750; 4339
19	1912; -255	59	2536; 4339
20	2126; -255	60	2322; 4339
21	2340; -255	61	2108; 4339
22	2554; -255	62	1894; 4339
23	2768; -255	63	1680; 4339
24	2982; -255	64	1466; 4339
25	3196; -255	65	1252; 4339
26	3410; -255	66	1038; 4339
27	3624; -255	67	824; 4339
28	3838; -255	68	610; 4339
29	4052; -255	69	396; 4339
30	4266; -255	70	182; 4339
31	4448; 0	71	0; 4084
32	4448; 214	72	0; 3870
33	4448; 446	73	0; 3638
34	4448; 660	74	0; 3424
35	4448; 874	75	0; 3210
36	4448; 1088	76	0; 2996
37	4448; 1302	77	0; 2782
38	4448; 1516	78	0; 2588
39	4448; 1730	79	0; 2354
40	4448; 1944	80	0; 2140

Die Specifications

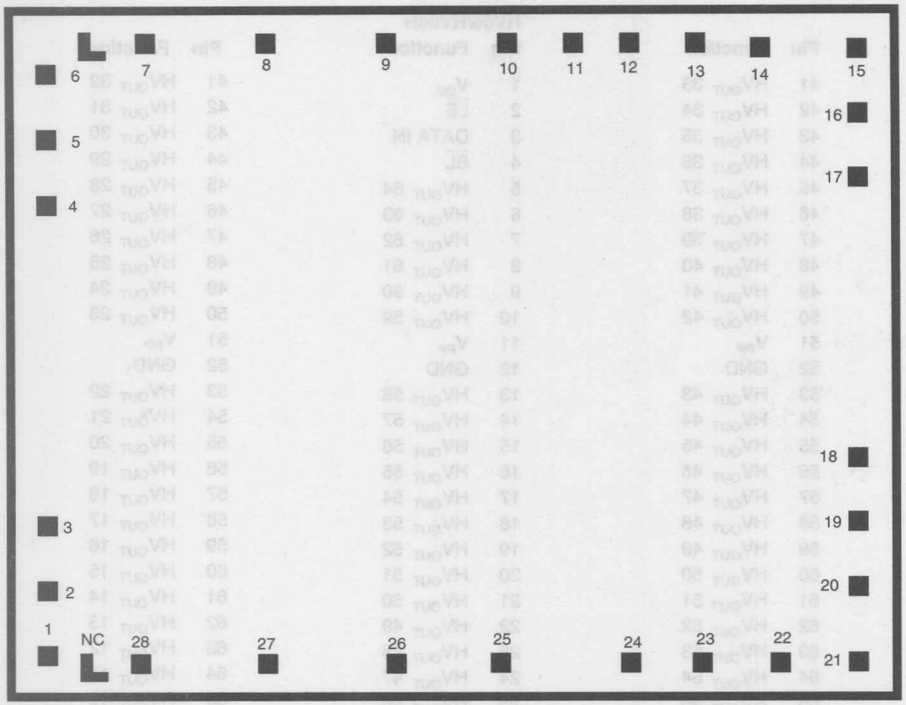
	mils	mm		
Die Size:	190 x 196	4.820 x 4.970	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4.5 x 4.5	0.11 x 0.11	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV04/HV04H

Pin	Function	Pin	Function
1	V_{DD}	41	HV_{OUT} 33
2	$\overline{LE}$	42	HV_{OUT} 34
3	DATA IN	43	HV_{OUT} 35
4	$\overline{BL}$	44	HV_{OUT} 36
5	HV_{OUT} 1	45	HV_{OUT} 37
6	HV_{OUT} 2	46	HV_{OUT} 38
7	HV_{OUT} 3	47	HV_{OUT} 39
8	HV_{OUT} 4	48	HV_{OUT} 40
9	HV_{OUT} 5	49	HV_{OUT} 41
10	HV_{OUT} 6	50	HV_{OUT} 42
11	V_{PP}	51	V_{PP}
12	GND	52	GND
13	HV_{OUT} 7	53	HV_{OUT} 43
14	HV_{OUT} 8	54	HV_{OUT} 44
15	HV_{OUT} 9	55	HV_{OUT} 45
16	HV_{OUT} 10	56	HV_{OUT} 46
17	HV_{OUT} 11	57	HV_{OUT} 47
18	HV_{OUT} 12	58	HV_{OUT} 48
19	HV_{OUT} 13	59	HV_{OUT} 49
20	HV_{OUT} 14	60	HV_{OUT} 50
21	HV_{OUT} 15	61	HV_{OUT} 51
22	HV_{OUT} 16	62	HV_{OUT} 52
23	HV_{OUT} 17	63	HV_{OUT} 53
24	HV_{OUT} 18	64	HV_{OUT} 54
25	HV_{OUT} 19	65	HV_{OUT} 55
26	HV_{OUT} 20	66	HV_{OUT} 56
27	HV_{OUT} 21	67	HV_{OUT} 57
28	HV_{OUT} 22	68	HV_{OUT} 58
29	GND	69	GND
30	V_{PP}	70	V_{PP}
31	HV_{OUT} 23	71	HV_{OUT} 59
32	HV_{OUT} 24	72	HV_{OUT} 60
33	HV_{OUT} 25	73	HV_{OUT} 61
34	HV_{OUT} 26	74	HV_{OUT} 62
35	HV_{OUT} 27	75	HV_{OUT} 63
36	HV_{OUT} 28	76	HV_{OUT} 64
37	HV_{OUT} 29	77	$\overline{POL}$
38	HV_{OUT} 30	78	DATA OUT
39	HV_{OUT} 31	79	CLK
40	HV_{OUT} 32	80	GND

HV06/HV06H

Pin	Function	Pin	Function
1	V_{DD}	41	HV_{OUT} 32
2	$\overline{LE}$	42	HV_{OUT} 31
3	DATA IN	43	HV_{OUT} 30
4	$\overline{BL}$	44	HV_{OUT} 29
5	HV_{OUT} 64	45	HV_{OUT} 28
6	HV_{OUT} 63	46	HV_{OUT} 27
7	HV_{OUT} 62	47	HV_{OUT} 26
8	HV_{OUT} 61	48	HV_{OUT} 25
9	HV_{OUT} 60	49	HV_{OUT} 24
10	HV_{OUT} 59	50	HV_{OUT} 23
11	V_{PP}	51	V_{PP}
12	GND	52	GND
13	HV_{OUT} 58	53	HV_{OUT} 22
14	HV_{OUT} 57	54	HV_{OUT} 21
15	HV_{OUT} 56	55	HV_{OUT} 20
16	HV_{OUT} 55	56	HV_{OUT} 19
17	HV_{OUT} 54	57	HV_{OUT} 18
18	HV_{OUT} 53	58	HV_{OUT} 17
19	HV_{OUT} 52	59	HV_{OUT} 16
20	HV_{OUT} 51	60	HV_{OUT} 15
21	HV_{OUT} 50	61	HV_{OUT} 14
22	HV_{OUT} 49	62	HV_{OUT} 13
23	HV_{OUT} 48	63	HV_{OUT} 12
24	HV_{OUT} 47	64	HV_{OUT} 11
25	HV_{OUT} 46	65	HV_{OUT} 10
26	HV_{OUT} 45	66	HV_{OUT} 9
27	HV_{OUT} 44	67	HV_{OUT} 8
28	HV_{OUT} 43	68	HV_{OUT} 7
29	GND	69	GND
30	V_{PP}	70	V_{PP}
31	HV_{OUT} 42	71	HV_{OUT} 6
32	HV_{OUT} 41	72	HV_{OUT} 5
33	HV_{OUT} 40	73	HV_{OUT} 4
34	HV_{OUT} 39	74	HV_{OUT} 3
35	HV_{OUT} 38	75	HV_{OUT} 2
36	HV_{OUT} 37	76	HV_{OUT} 1
37	HV_{OUT} 36	77	$\overline{POL}$
38	HV_{OUT} 35	78	DATA OUT
39	HV_{OUT} 34	79	CLK
40	HV_{OUT} 33	80	GND



Pad Coordinates in Microns

1	0; 0
2	0; 378
3	0; 756
4	0; 2640
5	0; 3018
6	0; 3396
7	565; 3565
8	1265; 3565
9	1965 ; 3565
10	2665; 3565
11	3043; 3565
12	3368; 3565
13	3746; 3565
14	4124; 3535
15	4689; 3529
16	4689; 3151
17	4689; 2773
18	4689; 1150
19	4689; 772
20	4689; 394
21	4689; -49
22	4235; -49
23	3781; -49
24	3365; -49
25	2615; -49
26	2015; -49
27	1265; -49
28	535; -49

Die Specifications

	mils	mm		
Die Size:	210 x 159	5.330 x 4.030	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4.5 x 4.5	0.11 x 0.11	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV10

Pin	Function
1	SW1
2	SW0
3	SW0
4	V_{DD}
5	GND
6	LE
7	N/C
8	$\overline{C0}$
9	$\overline{C1}$
10	N/C
11	N/C
12	N/C
13	$\overline{C2}$
14	N/C
15	$\overline{C3}$
16	V_{NN}
17	CL
18	V_{PP}
19	SW3
20	SW3
21	N/C
22	SW2
23	N/C
24	N/C
25	SW2
26	N/C
27	SW1
28	N/C

HV12

Pin	Function
1	N/C
2	Y2
3	Y3
4	Y4
5	Y5
6	N/C
7	Y6
8	N/C
9	Y7
10	N/C
11	N/C
12	D_{OUT}
13	CL
14	N/C
15	LE
16	CK
17	D_{IN}
18	N/C
19	V_{DD}
20	GND
21	V_{NN}
22	V_{PP}
23	N/C
24	YC
25	N/C
26	Y0
27	N/C
28	Y1

HV14

Pin	Function
1	N/C
2	Y6
3	Y4
4	V_{DD}
5	Y2
6	Y1
7	N/C
8	Y0
9	N/C
10	Y3
11	N/C
12	A
13	B
14	N/C
15	C
16	CL
17	D_{IN}
18	N/C
19	V_{PP}
20	$\overline{CS2}$
21	GND
22	V_{NN}
23	$\overline{CS1}$
24	Y5
25	N/C
26	Y7
27	N/C
28	YC

HV15

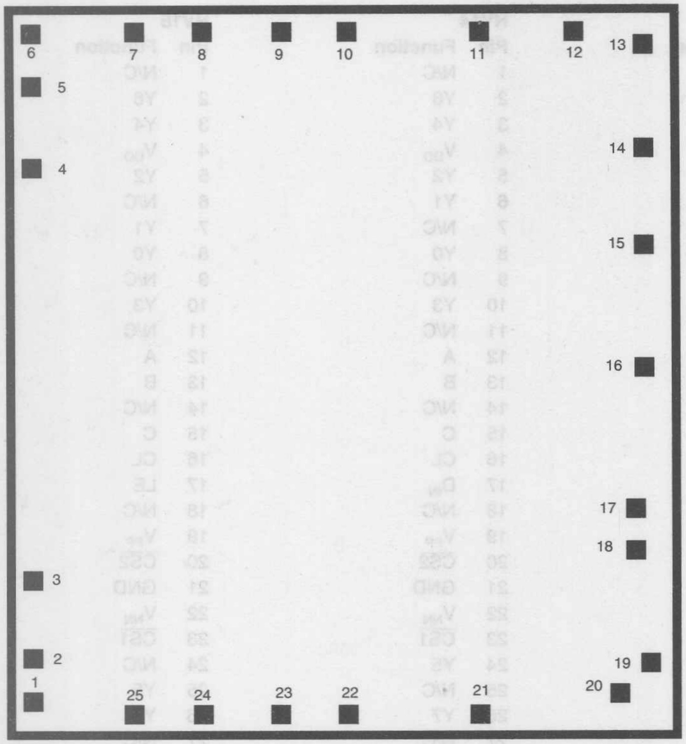
Pin	Function
1	N/C
2	Y6
3	Y4
4	V_{DD}
5	Y2
6	N/C
7	Y1
8	Y0
9	N/C
10	Y3
11	N/C
12	A
13	B
14	N/C
15	C
16	CL
17	LE
18	N/C
19	V_{PP}
20	$\overline{CS2}$
21	GND
22	V_{NN}
23	$\overline{CS1}$
24	N/C
25	Y5
26	Y7
27	N/C
28	Y6

HV16

Pin	Function	Pin	Function
1	N/C	15	LE
2	SW3	16	CK
3	SW3	17	D_{IN}
4	SW4	18	N/C
5	SW4	19	I_{DD}
6	SW5	20	GND
7	N/C	21	V_{NN}
8	SW5	22	V_{PP}
9	SW6	23	SW0
10	N/C	24	SW0
11	SW6	25	SW1
12	SW7	26	SW1
13	SW7	27	SW2
14	D_{OUT}	28	SW2

HV18

Pin	Function	Pin	Function
1	N/C	15	LE
2	SW3	16	CLK
3	SW3	17	D_{IN}
4	SW4	18	N/C
5	SW4	19	V_{DD}
6	SW5	20	GND
7	SW5	21	V_{NN}
8	SW6	22	V_{PP}
9	SW6	23	SW0
10	SW7	24	SW0
11	SW7	25	SW1
12	D_{OUT}	26	SW1
13	CL	27	SW2
14	N/C	28	SW2



Pad Coordinates in Microns

1	0; 0
2	-1; 302.5
3	0; 831
4	2; 3611
5	.5; 4156
6	-5.5; 4512
7	691; 4526
8	1148.5; 4527
9	1664.5; 4527
10	2104.5; 4527
11	2990.5; 4527
12	3622; 4525.5
13	4081.5; 4459.5
14	4081.5; 3763
15	4081.5; 3117
16	4081.5; 2279
17	4025.5; 1331
18	4029.5; 1051
19	4131.5; 285
20	3920.5; 84
21	2986.5; -70
22	2100.5; -85
23	1660.5; -85
24	1144.5; -85
25	677; -84

HV21/HV22

Pin	Function	Pin	Function	Pin	Function
1	SW2	9	SW6	17	V_{DD}
2	SW3	10	SW7	18	GND
3	SW3	11	SW7	19	V_{NN}
4	SW4	12	Data out	20	V_{PP}
5	SW4	13	N/C (CL for HV22)	21	SW0
6	SW5	14	LE	22	SW0
7	SW5	15	CK	23	SW1
8	SW6	16	DIN	24	SW1
				25	SW2

Die Specifications

	mils	mm		
Die Size:	223 x 183	5.660 x 4.640	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4.5 x 4.5	0.11 x 0.11	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

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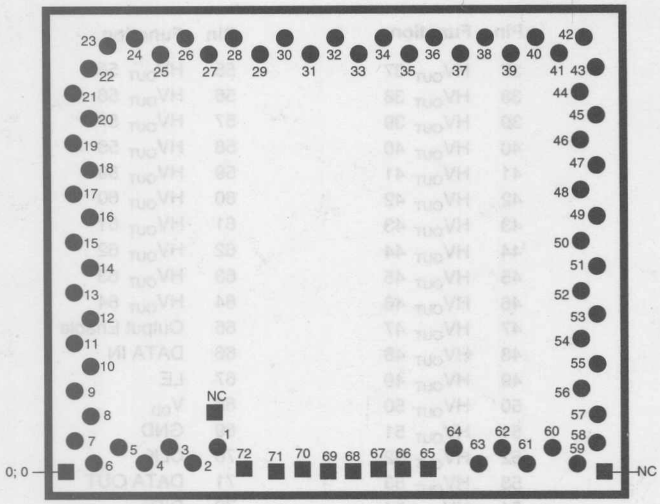
Die Specifications



Pad Coordinates in Microns

1	1222; 192	37	3162; 3370.5
2	1022; 62	38	3362; 3500.5
3	819; 192	39	3562.5; 3370.5
4	619; 62	40	3762.5; 3500.5
5	418.5; 192	41	3959.5; 3370.5
6	218.5; 62	42	4159.5; 3500.5
7	62.5; 240.5	43	4262; 3285.5
8	192.5; 440.5	44	4132; 3085.5
9	62; 641	45	4262; 2885
10	192; 841	46	4132; 2685
11	62; 1042	47	4262; 2484
12	192; 1242	48	4132; 2284
13	62; 1442.5	49	4262; 2083.5
14	192; 1642.5	50	4132; 1883.5
15	62; 1848.5	51	4262; 1677.5
16	192; 2048.5	52	4132; 1477.5
17	62; 2249	53	4262; 1277
18	192; 2449	54	4132; 1077
19	62; 2650	55	4262; 876
20	192; 2850	56	4132.5; 676
21	62; 3050.5	57	4262; 475.5
22	192; 3250.5	58	4266; 237.5
23	330; 3445	59	4108.5; 62
24	563.5; 3503	60	3908.5; 192
25	758.5; 3370.5	61	3709; 62
26	958.5; 3500.5	62	3509; 192
27	1159; 3370.5	63	3309; 62
28	1359; 3500.5	64	3109; 192
29	1560; 3370.5	65	2905.5; 4
30	1760; 3500.5	66	2704; 4
31	1960.5; 3370.5	67	2502.5; 4
32	2160.5; 3500.5	68	2311; 0
33	2360.5; 3370.5	69	2103; 0
34	2560.5; 3500.5	70	1901; 4
35	2761; 3370.5	71	1691; 0
36	2961; 3500.5	72	1426; 4

Die Specifications

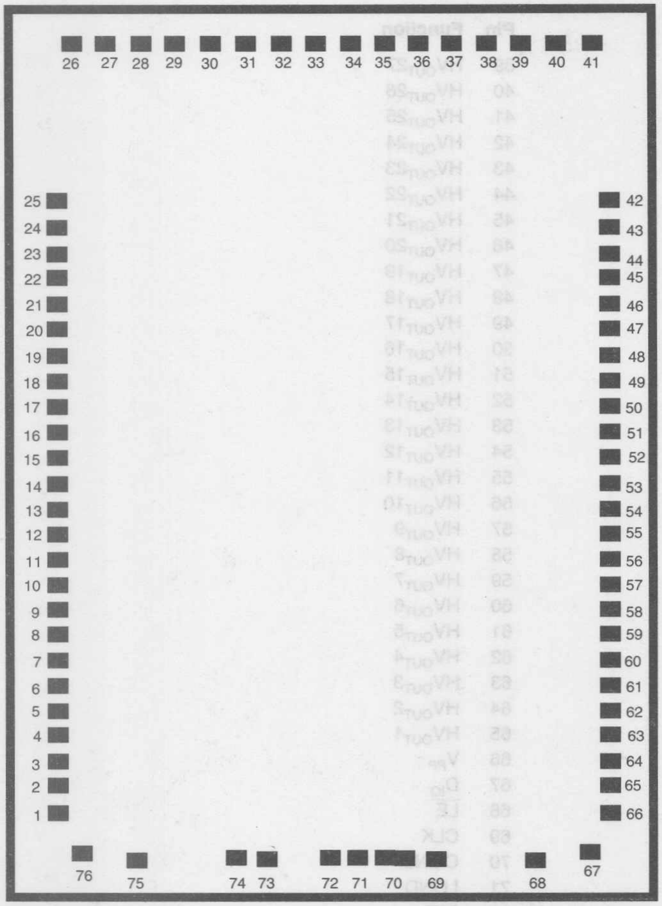
	mils	mm		
Die Size:	184 x 156	4.670 x 3.960	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or Equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV31

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HV_{OUT} 1	19	HV_{OUT} 19	37	HV_{OUT} 37	55	HV_{OUT} 55
2	HV_{OUT} 2	20	HV_{OUT} 20	38	HV_{OUT} 38	56	HV_{OUT} 56
3	HV_{OUT} 3	21	HV_{OUT} 21	39	HV_{OUT} 39	57	HV_{OUT} 57
4	HV_{OUT} 4	22	HV_{OUT} 22	40	HV_{OUT} 40	58	HV_{OUT} 58
5	HV_{OUT} 5	23	HV_{OUT} 23	41	HV_{OUT} 41	59	HV_{OUT} 59
6	HV_{OUT} 6	24	HV_{OUT} 24	42	HV_{OUT} 42	60	HV_{OUT} 60
7	HV_{OUT} 7	25	HV_{OUT} 25	43	HV_{OUT} 43	61	HV_{OUT} 61
8	HV_{OUT} 8	26	HV_{OUT} 26	44	HV_{OUT} 44	62	HV_{OUT} 62
9	HV_{OUT} 9	27	HV_{OUT} 27	45	HV_{OUT} 45	63	HV_{OUT} 63
10	HV_{OUT} 10	28	HV_{OUT} 28	46	HV_{OUT} 46	64	HV_{OUT} 64
11	HV_{OUT} 11	29	HV_{OUT} 29	47	HV_{OUT} 47	65	Output Enable
12	HV_{OUT} 12	30	HV_{OUT} 30	48	HV_{OUT} 48	66	DATA IN
13	HV_{OUT} 13	31	HV_{OUT} 31	49	HV_{OUT} 49	67	LE
14	HV_{OUT} 14	32	HV_{OUT} 32	50	HV_{OUT} 50	68	V_{DD}
15	HV_{OUT} 15	33	HV_{OUT} 33	51	HV_{OUT} 51	69	GND
16	HV_{OUT} 16	34	HV_{OUT} 34	52	HV_{OUT} 52	70	CLK
17	HV_{OUT} 17	35	HV_{OUT} 35	53	HV_{OUT} 53	71	DATA OUT
18	HV_{OUT} 18	36	HV_{OUT} 36	54	HV_{OUT} 54	72	DIR

Note: HV_{OUT} sequence dependent on DIR polarity

PIN	DIR	HV_{OUT}
1	H	1
1	L	64



Pad Coordinates in Microns

1	0;0	39	2622; 5185
2	6; 187	40	3816; 5185
3	6; 359	41	3010; 5185
4	6; 531	42	3092; 4143
5	6; 703	43	3092; 3971
6	6; 875	44	3092; 3799
7	6; 1047	45	3092; 3627
8	6; 1219	46	3092; 3455
9	6; 1391	47	3092; 3283
10	6; 1563	48	3092; 3111
11	6; 1735	49	3092; 2939
12	6; 1907	50	3092; 2767
13	6; 2079	51	3092; 2595
14	6; 2251	52	3092; 2423
15	6; 2423	53	3092; 2251
16	6; 2595	54	3092; 2079
17	6; 2767	55	3092; 1907
18	6; 2939	56	3092; 1735
19	6; 3111	57	3092; 1563
20	6; 3283	58	3092; 1391
21	6; 3455	59	3092; 1219
22	6; 3627	60	3092; 1047
23	6; 3799	61	3092; 875
24	6; 3971	62	3092; 703
25	6; 4143	63	3092; 531
26	100; 5185	64	3092; 359
27	294; 5185	65	3092; 187
28	488; 5185	66	3100; 0
29	682; 5185	67	2976; -262
30	876; 5185	68	2676; -307
31	1070; 5185	69	2118; -307
32	1264; 5185	70	1896; -307
33	1458; 5185	71	1674; -307
34	1652; 5185	72	1512; -307
35	1846; 5185	73	1147; -307
36	2040; 5185	74	985; -307
37	2234; 5185	75	427; -307
38	2428; 5185	76	172; -262

Die Specifications

	mils	mm		
Die Size:	235 x 140	5.969 x 3.556	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or Equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV34

Pin	Function	Pin	Function
1	V_{PP}	39	$HV_{OUT}27$
2	$HV_{OUT}64$	40	$HV_{OUT}26$
3	$HV_{OUT}63$	41	$HV_{OUT}25$
4	$HV_{OUT}62$	42	$HV_{OUT}24$
5	$HV_{OUT}61$	43	$HV_{OUT}23$
6	$HV_{OUT}60$	44	$HV_{OUT}22$
7	$HV_{OUT}59$	45	$HV_{OUT}21$
8	$HV_{OUT}58$	46	$HV_{OUT}20$
9	$HV_{OUT}57$	47	$HV_{OUT}19$
10	$HV_{OUT}56$	48	$HV_{OUT}18$
11	$HV_{OUT}55$	49	$HV_{OUT}17$
12	$HV_{OUT}54$	50	$HV_{OUT}16$
13	$HV_{OUT}53$	51	$HV_{OUT}15$
14	$HV_{OUT}52$	52	$HV_{OUT}14$
15	$HV_{OUT}51$	53	$HV_{OUT}13$
16	$HV_{OUT}50$	54	$HV_{OUT}12$
17	$HV_{OUT}49$	55	$HV_{OUT}11$
18	$HV_{OUT}48$	56	$HV_{OUT}10$
19	$HV_{OUT}47$	57	$HV_{OUT}9$
20	$HV_{OUT}46$	58	$HV_{OUT}8$
21	$HV_{OUT}45$	59	$HV_{OUT}7$
22	$HV_{OUT}44$	60	$HV_{OUT}6$
23	$HV_{OUT}43$	61	$HV_{OUT}5$
24	$HV_{OUT}42$	62	$HV_{OUT}4$
25	$HV_{OUT}41$	63	$HV_{OUT}3$
26	$HV_{OUT}40$	64	$HV_{OUT}2$
27	$HV_{OUT}39$	65	$HV_{OUT}1$
28	$HV_{OUT}38$	66	V_{PP}
29	$HV_{OUT}37$	67	D_{IO}
30	$HV_{OUT}36$	68	$\overline{LE}$
31	$HV_{OUT}35$	69	CLK
32	$HV_{OUT}34$	70	OGND
33	$HV_{OUT}33$	71	LGND
34	$HV_{OUT}32$	72	DIR
35	$HV_{OUT}31$	73	V_{DD}
36	$HV_{OUT}30$	74	$\overline{PL}$
37	$HV_{OUT}29$	75	$\overline{BL}$
38	$HV_{OUT}28$	76	D_{IO}

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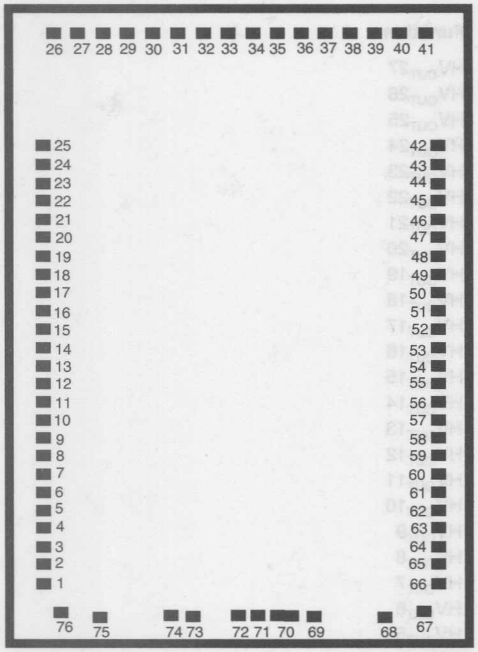
Die Specifications



Pad Coordinates in Microns

1	0; 0	39	2622; 5185
2	6; 187	40	2816; 5185
3	6; 359	41	3010; 5185
4	6; 531	42	3092; 4143
5	6; 703	43	3092; 3971
6	6; 875	44	3092; 3799
7	6; 1047	45	3092; 3627
8	6; 1219	46	3092; 3455
9	6; 1391	47	3092; 3283
10	6; 1563	48	3092; 3111
11	6; 1735	49	3092; 2939
12	6; 1907	50	3092; 2767
13	6; 2079	51	3092; 2595
14	6; 2251	52	3092; 2423
15	6; 2423	53	3092; 2251
16	6; 2595	54	3092; 2079
17	6; 2767	55	3092; 1907
18	6; 2939	56	3092; 1735
19	6; 3111	57	3092; 1563
20	6; 3283	58	3092; 1391
21	6; 3455	59	3092; 1219
22	6; 3627	60	3092; 1047
23	6; 3799	61	3092; 875
24	6; 3971	62	3092; 703
25	6; 4143	63	3092; 531
26	100; 5185	64	3092; 359
27	294; 5185	65	3092; 187
28	488; 5185	66	3100; 0
29	682; 5185	67	2976; -262
30	876; 5185	68	2676; -307
31	1070; 5185	69	2118; -307
32	1264; 5185	70	1896; -307
33	1458; 5185	71	1674; -307
34	1652; 5185	72	1512; -307
35	1846; 5185	73	1147; -307
36	2040; 5185	74	985; -307
37	2234; 5185	75	427; -307
38	2428; 5185	76	172; -262

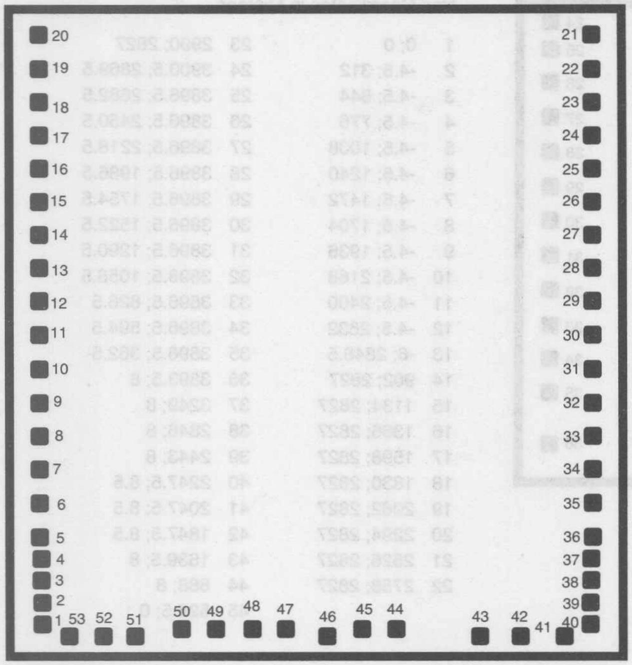
Die Specifications

	mils	mm		
Die Size:	235 x 140	5.969 x 3.556	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or Equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV35

Pin	Function	Pin	Function
1	V_{PP}	39	$HV_{OUT}27$
2	$HV_{OUT}64$	40	$HV_{OUT}26$
3	$HV_{OUT}63$	41	$HV_{OUT}25$
4	$HV_{OUT}62$	42	$HV_{OUT}24$
5	$HV_{OUT}61$	43	$HV_{OUT}23$
6	$HV_{OUT}60$	44	$HV_{OUT}22$
7	$HV_{OUT}59$	45	$HV_{OUT}21$
8	$HV_{OUT}58$	46	$HV_{OUT}20$
9	$HV_{OUT}57$	47	$HV_{OUT}19$
10	$HV_{OUT}56$	48	$HV_{OUT}18$
11	$HV_{OUT}55$	49	$HV_{OUT}17$
12	$HV_{OUT}54$	50	$HV_{OUT}16$
13	$HV_{OUT}53$	51	$HV_{OUT}15$
14	$HV_{OUT}52$	52	$HV_{OUT}14$
15	$HV_{OUT}51$	53	$HV_{OUT}13$
16	$HV_{OUT}50$	54	$HV_{OUT}12$
17	$HV_{OUT}49$	55	$HV_{OUT}11$
18	$HV_{OUT}48$	56	$HV_{OUT}10$
19	$HV_{OUT}47$	57	$HV_{OUT}9$
20	$HV_{OUT}46$	58	$HV_{OUT}8$
21	$HV_{OUT}45$	59	$HV_{OUT}7$
22	$HV_{OUT}44$	60	$HV_{OUT}6$
23	$HV_{OUT}43$	61	$HV_{OUT}5$
24	$HV_{OUT}42$	62	$HV_{OUT}4$
25	$HV_{OUT}41$	63	$HV_{OUT}3$
26	$HV_{OUT}40$	64	$HV_{OUT}2$
27	$HV_{OUT}39$	65	$HV_{OUT}1$
28	$HV_{OUT}38$	66	V_{PP}
29	$HV_{OUT}37$	67	D_{IOB}
30	$HV_{OUT}36$	68	$\overline{LE}$
31	$HV_{OUT}35$	69	CLK
32	$HV_{OUT}34$	70	GND
33	$HV_{OUT}33$	71	V_{BIAS}
34	$HV_{OUT}32$	72	DIR
35	$HV_{OUT}31$	73	V_{DD}
36	$HV_{OUT}30$	74	$\overline{PL}$
37	$HV_{OUT}29$	75	$\overline{BL}$
38	$HV_{OUT}28$	76	D_{IOA}

Note: Pad designation for DIR = H.



Pad Coordinates in Microns

1	0; 0	27	3993; 2826.5
2	0; 158	28	3993; 2582.5
3	1; 316	29	3993; 2338.5
4	1; 474	30	3993; 2094.5
5	-9; 630.5	31	3993; 1850.5
6	-9; 874.5	32	3993; 1606.5
7	-9; 1118.5	33	3993; 1362.5
8	-9; 1362.5	34	3993; 1118.5
9	-9; 1606.5	35	3993; 874.5
10	-9; 1850.5	36	3993; 630.5
11	-6; 2094.5	37	3990; 474
12	-9; 2338.5	38	3990; 316
13	-9; 2582.5	39	3991; 158
14	-9; 2826.5	40	3991; 0
15	-9; 3070.5	41	3788; -107
16	-9; 3314.5	42	3471; -107
17	-9; 3558.5	43	3179; -107
18	-9; 3802.5	44	2578; -47
19	-9; 4046.5	45	2328; -47
20	1; 4297.5	46	2078; -107
21	3980; 4297.5	47	1770; -48
22	3980; 4046.5	48	1525; -48
23	3993; 3802.5	49	1270; -48
24	3993; 3558.5	50	1020; -48
25	3993; 3314.5	51	682; -107
26	3993; 3070.5	52	450; -107
		53	208; -107

HV38

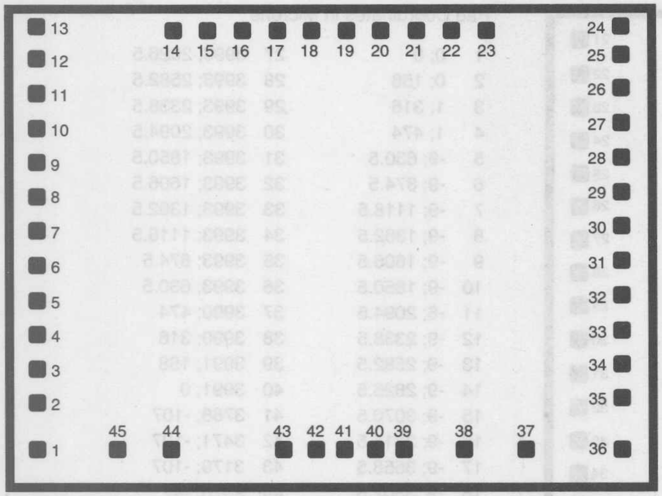
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HVGND	14	HV_{OUT}7	27	HV_{OUT}26	40	HVGND
2	V_{PP}1	15	HV_{OUT}6	28	HV_{OUT}25	41	Descent
3	VR	16	HV_{OUT}5	29	HV_{OUT}24	42	Count Clock
4	V_{PP}2	17	HV_{OUT}4	30	HV_{OUT}23	43	Load Count
5	HV_{OUT}16	18	HV_{OUT}3	31	HV_{OUT}22	44	V_{DD}
6	HV_{OUT}15	19	HV_{OUT}2	32	HV_{OUT}21	45	DIR
7	HV_{OUT}14	20	HV_{OUT}1	33	HV_{OUT}20	46	LVGND
8	HV_{OUT}13	21	HV_{OUT}32	34	HV_{OUT}19	47	D1
9	HV_{OUT}12	22	HV_{OUT}31	35	HV_{OUT}18	48	D2
10	HV_{OUT}11	23	HV_{OUT}30	36	HV_{OUT}17	49	D3
11	HV_{OUT}10	24	HV_{OUT}29	37	V_{PP}2	50	D4
12	HV_{OUT}9	25	HV_{OUT}28	38	VR	51	Shift Clock
13	HV_{OUT}8	26	HV_{OUT}27	39	V_{PP}1	52	N/C
						53	Ascent

Die Specifications

	mils	mm		
Die Size:	176 x 188	4.470 x 4.770	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

Supertex inc.

HV41/HV42
HV45/HV46
Die Specifications



Pad Coordinates in Microns

Pad	Coordinates	Pad	Coordinates
1	0; 0	23	2990; 2827
2	-4.5; 312	24	3900.5; 2869.5
3	-4.5; 544	25	3896.5; 2682.5
4	-4.5; 776	26	3896.5; 2450.5
5	-4.5; 1008	27	3896.5; 2218.5
6	-4.5; 1240	28	3896.5; 1986.5
7	-4.5; 1472	29	3896.5; 1754.5
8	-4.5; 1704	30	3896.5; 1522.5
9	-4.5; 1936	31	3896.5; 1290.5
10	-4.5; 2168	32	3896.5; 1058.5
11	-4.5; 2400	33	3896.5; 826.5
12	-4.5; 2632	34	3896.5; 594.5
13	-6; 2846.5	35	3896.5; 362.5
14	902; 2827	36	3893.5; 8
15	1134; 2827	37	3249; 8
16	1366; 2827	38	2846; 8
17	1598; 2827	39	2443; 8
18	1830; 2827	40	2247.5; 8.5
19	2062; 2827	41	2047.5; 8.5
20	2294; 2827	42	1847.5; 8.5
21	2526; 2827	43	1639.5; 8
22	2758; 2827	44	888; 8
		45	526.5; 0

Die Specifications

	mils			mm				
Die Size:	129	x	171	3.270	x	4.340	**Back Side Metal:**	None
Die Thickness:	20 ±1			0.50 ±0.02			**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4	x	4	0.10	x	0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3			0.03				

HV41

Pin	Function
1	NC
2	HV_{OUT} 32
3	HV_{OUT} 31
4	HV_{OUT} 30
5	HV_{OUT} 29
6	HV_{OUT} 28
7	HV_{OUT} 27
8	HV_{OUT} 26
9	HV_{OUT} 25
10	HV_{OUT} 24
11	HV_{OUT} 23
12	HV_{OUT} 22
13	NC
14	HV_{OUT} 21
15	HV_{OUT} 20
16	HV_{OUT} 19
17	HV_{OUT} 18
18	HV_{OUT} 17
19	HV_{OUT} 16
20	HV_{OUT} 15
21	HV_{OUT} 14
22	HV_{OUT} 13
23	HV_{OUT} 12
24	NC
25	HV_{OUT} 11
26	HV_{OUT} 10
27	HV_{OUT} 9
28	HV_{OUT} 8
29	HV_{OUT} 7
30	HV_{OUT} 6
31	HV_{OUT} 5
32	HV_{OUT} 4
33	HV_{OUT} 3
34	HV_{OUT} 2
35	HV_{OUT} 1
36	NC
37	Data In
38	Strobe
39	NC
40	V_{DD}
41	GND
42	GND
43	Clock
44	Output Enable
45	Data Out

HV42

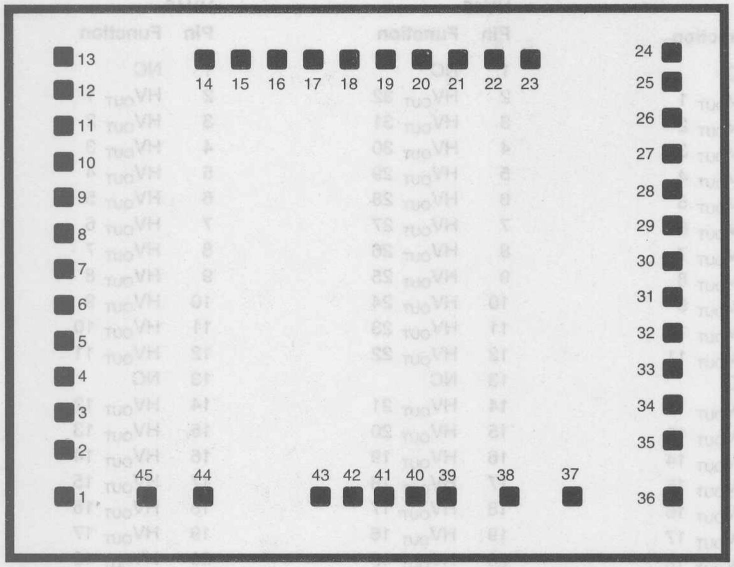
Pin	Function
1	NC
2	HV_{OUT} 1
3	HV_{OUT} 2
4	HV_{OUT} 3
5	HV_{OUT} 4
6	HV_{OUT} 5
7	HV_{OUT} 6
8	HV_{OUT} 7
9	HV_{OUT} 8
10	HV_{OUT} 9
11	HV_{OUT} 10
12	HV_{OUT} 11
13	NC
14	HV_{OUT} 12
15	HV_{OUT} 13
16	HV_{OUT} 14
17	HV_{OUT} 15
18	HV_{OUT} 16
19	HV_{OUT} 17
20	HV_{OUT} 18
21	HV_{OUT} 19
22	HV_{OUT} 20
23	HV_{OUT} 21
24	NC
25	HV_{OUT} 22
26	HV_{OUT} 23
27	HV_{OUT} 24
28	HV_{OUT} 25
29	HV_{OUT} 26
30	HV_{OUT} 27
31	HV_{OUT} 28
32	HV_{OUT} 29
33	HV_{OUT} 30
34	HV_{OUT} 31
35	HV_{OUT} 32
36	NC
37	Data In
38	Strobe
39	NC
40	V_{DD}
41	GND
42	GND
43	Clock
44	Output Enable
45	Data Out

HV45

Pin	Function
1	NC
2	HV_{OUT} 32
3	HV_{OUT} 31
4	HV_{OUT} 30
5	HV_{OUT} 29
6	HV_{OUT} 28
7	HV_{OUT} 27
8	HV_{OUT} 26
9	HV_{OUT} 25
10	HV_{OUT} 24
11	HV_{OUT} 23
12	HV_{OUT} 22
13	NC
14	HV_{OUT} 21
15	HV_{OUT} 20
16	HV_{OUT} 19
17	HV_{OUT} 18
18	HV_{OUT} 17
19	HV_{OUT} 16
20	HV_{OUT} 15
21	HV_{OUT} 14
22	HV_{OUT} 13
23	HV_{OUT} 12
24	NC
25	HV_{OUT} 11
26	HV_{OUT} 10
27	HV_{OUT} 9
28	HV_{OUT} 8
29	HV_{OUT} 7
30	HV_{OUT} 6
31	HV_{OUT} 5
32	HV_{OUT} 4
33	HV_{OUT} 3
34	HV_{OUT} 2
35	HV_{OUT} 1
36	NC
37	Blanking
38	Data In
39	LE
40	V_{DD}
41	GND
42	GND
43	Clock
44	Polarity
45	Data Out

HV46

Pin	Function
1	NC
2	HV_{OUT} 1
3	HV_{OUT} 2
4	HV_{OUT} 3
5	HV_{OUT} 4
6	HV_{OUT} 5
7	HV_{OUT} 6
8	HV_{OUT} 7
9	HV_{OUT} 8
10	HV_{OUT} 9
11	HV_{OUT} 10
12	HV_{OUT} 11
13	NC
14	HV_{OUT} 12
15	HV_{OUT} 13
16	HV_{OUT} 14
17	HV_{OUT} 15
18	HV_{OUT} 16
19	HV_{OUT} 17
20	HV_{OUT} 18
21	HV_{OUT} 19
22	HV_{OUT} 20
23	HV_{OUT} 21
24	NC
25	HV_{OUT} 22
26	HV_{OUT} 23
27	HV_{OUT} 24
28	HV_{OUT} 25
29	HV_{OUT} 26
30	HV_{OUT} 27
31	HV_{OUT} 28
32	HV_{OUT} 29
33	HV_{OUT} 30
34	HV_{OUT} 31
35	HV_{OUT} 32
36	NC
37	Blanking
38	Data In
39	LE
40	V_{DD}
41	GND
42	GND
43	Clock
44	Polarity
45	Data Out



Pad Coordinates in Microns

1	0; 0	24	3900.5; 2869.5
2	-4.5; 312	25	3896.5; 2682.5
3	-4.5; 544	26	3896.5; 2450.5
4	-4.5; 776	27	3896.5; 2218.5
5	-4.5; 1008	28	3896.5; 1986.5
6	-4.5; 1240	29	3896.5; 1754.5
7	-4.5; 1472	30	3896.5; 1522.5
8	-4.5; 1704	31	3896.5; 1290.5
9	-4.5; 1936	32	3896.5; 1058.5
10	-4.5; 2168	33	3896.5; 826.5
11	-4.5; 2400	34	3896.5; 594.5
12	-4.5; 2632	35	3896.5; 362.5
13	-6; 2846.5	36	3093.5; 8
14	902; 2827	37	3249; 8
15	1134; 2827	38	2846; 8
16	1366; 2827	39	2443; 8
17	1598; 2827	40	2247.5; 8.5
18	1830; 2827	41	2047.5; 8.5
19	2062; 2827	42	1847.5; 8.5
20	2294; 2827	43	1639.5; 8
21	2526; 2827	44	888; 8
22	2758; 2827	45	526.5; 0
23	2990; 2827		

Die Specifications

	mils	mm		
Die Size:	129 x 171	3.270 x 4.340	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV51

Pin	Function
1	GND
2	HV_{OUT} 32
3	HV_{OUT} 31
4	HV_{OUT} 30
5	HV_{OUT} 29
6	HV_{OUT} 28
7	HV_{OUT} 27
8	HV_{OUT} 26
9	HV_{OUT} 25
10	HV_{OUT} 24
11	HV_{OUT} 23
12	HV_{OUT} 22
13	GND
14	HV_{OUT} 21
15	HV_{OUT} 20
16	HV_{OUT} 19
17	HV_{OUT} 18
18	HV_{OUT} 17
19	HV_{OUT} 16
20	HV_{OUT} 15
21	HV_{OUT} 14
22	HV_{OUT} 13
23	HV_{OUT} 12
24	GND
25	HV_{OUT} 11
26	HV_{OUT} 10
27	HV_{OUT} 9
28	HV_{OUT} 8
29	HV_{OUT} 7
30	HV_{OUT} 6
31	HV_{OUT} 5
32	HV_{OUT} 4
33	HV_{OUT} 3
34	HV_{OUT} 2
35	HV_{OUT} 1
36	GND
37	Data In
38	Strobe
39	NC
40	V_{DD}
41	GND
42	GND
43	Clock
44	Output Enable
45	Data Out

HV52

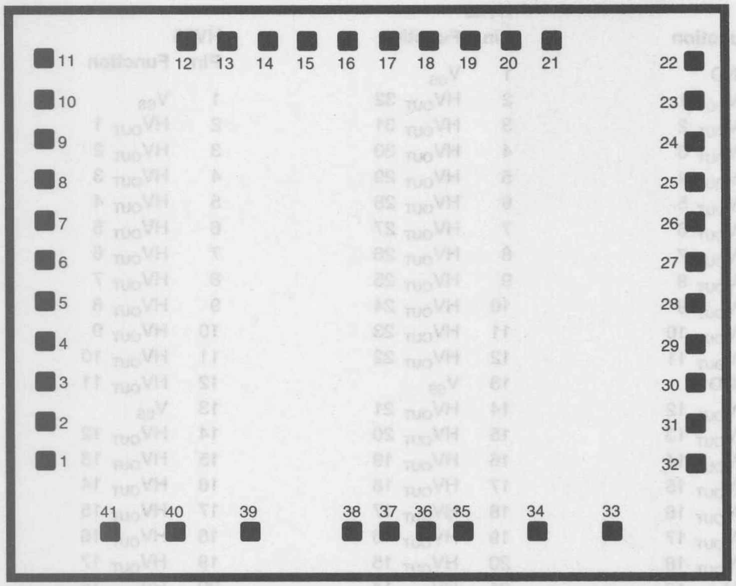
Pin	Function
1	GND
2	HV_{OUT} 1
3	HV_{OUT} 2
4	HV_{OUT} 3
5	HV_{OUT} 4
6	HV_{OUT} 5
7	HV_{OUT} 6
8	HV_{OUT} 7
9	HV_{OUT} 8
10	HV_{OUT} 9
11	HV_{OUT} 10
12	HV_{OUT} 11
13	GND
14	HV_{OUT} 12
15	HV_{OUT} 13
16	HV_{OUT} 14
17	HV_{OUT} 15
18	HV_{OUT} 16
19	HV_{OUT} 17
20	HV_{OUT} 18
21	HV_{OUT} 19
22	HV_{OUT} 20
23	HV_{OUT} 21
24	GND
25	HV_{OUT} 22
26	HV_{OUT} 23
27	HV_{OUT} 24
28	HV_{OUT} 25
29	HV_{OUT} 26
30	HV_{OUT} 27
31	HV_{OUT} 28
32	HV_{OUT} 29
33	HV_{OUT} 30
34	HV_{OUT} 31
35	HV_{OUT} 32
36	GND
37	Data In
38	Strobe
39	NC
40	V_{DD}
41	GND
42	GND
43	Clock
44	Output Enable
45	Data Out

HV55

Pin	Function
1	V_{SS}
2	HV_{OUT} 32
3	HV_{OUT} 31
4	HV_{OUT} 30
5	HV_{OUT} 29
6	HV_{OUT} 28
7	HV_{OUT} 27
8	HV_{OUT} 26
9	HV_{OUT} 25
10	HV_{OUT} 24
11	HV_{OUT} 23
12	HV_{OUT} 22
13	V_{SS}
14	HV_{OUT} 21
15	HV_{OUT} 20
16	HV_{OUT} 19
17	HV_{OUT} 18
18	HV_{OUT} 17
19	HV_{OUT} 16
20	HV_{OUT} 15
21	HV_{OUT} 14
22	HV_{OUT} 13
23	HV_{OUT} 12
24	V_{SS}
25	HV_{OUT} 11
26	HV_{OUT} 10
27	HV_{OUT} 9
28	HV_{OUT} 8
29	HV_{OUT} 7
30	HV_{OUT} 6
31	HV_{OUT} 5
32	HV_{OUT} 4
33	HV_{OUT} 3
34	HV_{OUT} 2
35	HV_{OUT} 1
36	V_{SS}
37	Blanking
38	Data In
39	Latch Enable
40	V_{DD}
41	V_{SS}
42	V_{SS}
43	Clock
44	Polarity
45	Data Out

HV56

Pin	Function
1	V_{SS}
2	HV_{OUT} 1
3	HV_{OUT} 2
4	HV_{OUT} 3
5	HV_{OUT} 4
6	HV_{OUT} 5
7	HV_{OUT} 6
8	HV_{OUT} 7
9	HV_{OUT} 8
10	HV_{OUT} 9
11	HV_{OUT} 10
12	HV_{OUT} 11
13	V_{SS}
14	HV_{OUT} 12
15	HV_{OUT} 13
16	HV_{OUT} 14
17	HV_{OUT} 15
18	HV_{OUT} 16
19	HV_{OUT} 17
20	HV_{OUT} 18
21	HV_{OUT} 19
22	HV_{OUT} 20
23	HV_{OUT} 21
24	V_{SS}
25	HV_{OUT} 22
26	HV_{OUT} 23
27	HV_{OUT} 24
28	HV_{OUT} 25
29	HV_{OUT} 26
30	HV_{OUT} 27
31	HV_{OUT} 28
32	HV_{OUT} 29
33	HV_{OUT} 30
34	HV_{OUT} 31
35	HV_{OUT} 32
36	V_{SS}
37	Blanking
38	Data In
39	Latch Enable
40	V_{DD}
41	V_{SS}
42	V_{SS}
43	Clock
44	Polarity
45	Data Out



Pad Coordinates in Microns

1	0; 0	22	3522.5; 2200.5
2	0; 220	23	3522.5; 1980.5
3	0; 440	24	3522.5; 1760.5
4	0; 660	25	3522.5; 1540.5
5	0; 880	26	3522.5; 1320.5
6	0; 1100	27	3522.5; 1100.5
7	0; 1320	28	3522.5; 880.5
8	0; 1540	29	3522.5; 660.5
9	0; 1760	30	3522.5; 440.5
10	0; 1980	31	3522.5; 220.5
11	0; 2200	32	3522.5; 0.5
12	770.5; 2312	33	3069.25; -390.75
13	990.5; 2312	34	2666.75; -390.75
14	1210.5; 2312	35	2263.75; -390.75
15	1430.5; 2312	36	2062.75; -390.75
16	1650.5; 2312	37	1862.75; -390.75
17	1870.5; 2312	38	1662.75; -390.75
18	1870.5; 2312	39	1110.75; 390.75
19	2310.5; 2312	40	708.25; 390.75
20	2530.5; 2312	41	346.75; 390.75
21	2750.5; 2312		

Die Specifications

	mils	mm		
Die Size:	155 x 125	3.930 x 3.170	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or Equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

Backside is V_{PP}

HV53/HV54
HV57/HV58
Die Specifications

HV53

Pin	Function
1	HV_{OUT} 1
2	HV_{OUT} 2
3	HV_{OUT} 3
4	HV_{OUT} 4
5	HV_{OUT} 5
6	HV_{OUT} 6
7	HV_{OUT} 7
8	HV_{OUT} 8
9	HV_{OUT} 9
10	HV_{OUT} 10
11	HV_{OUT} 11
12	HV_{OUT} 12
13	HV_{OUT} 13
14	HV_{OUT} 14
15	HV_{OUT} 15
16	HV_{OUT} 16
17	HV_{OUT} 17
18	HV_{OUT} 18
19	HV_{OUT} 19
20	HV_{OUT} 20
21	HV_{OUT} 21
22	HV_{OUT} 22
23	HV_{OUT} 23
24	HV_{OUT} 24
25	HV_{OUT} 25
26	HV_{OUT} 26
27	HV_{OUT} 27
28	HV_{OUT} 28
29	HV_{OUT} 29
30	HV_{OUT} 30
31	HV_{OUT} 31
32	HV_{OUT} 32
33	OE
34	Data In
35	LE
36	V_{DD}
37	V_{PP}
38	V_{SS}
39	CLK
40	NC
41	Data Out

HV54

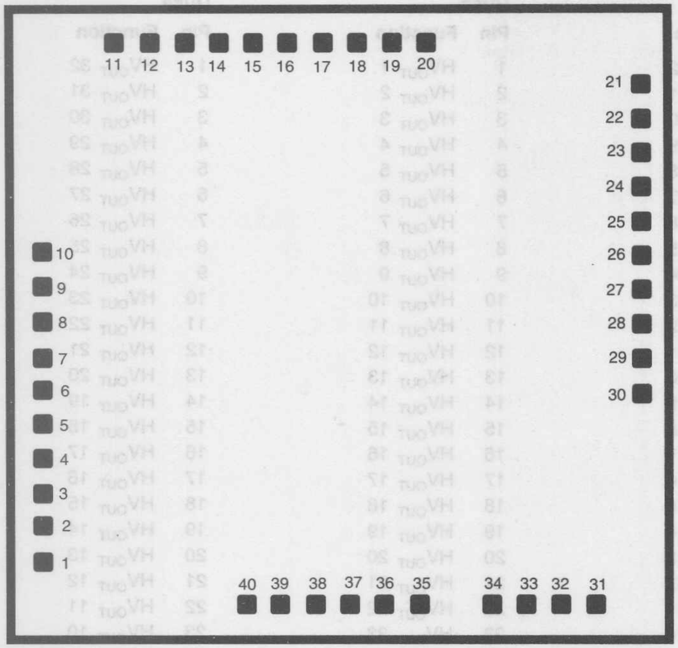
Pin	Function
1	HV_{OUT} 32
2	HV_{OUT} 31
3	HV_{OUT} 30
4	HV_{OUT} 29
5	HV_{OUT} 28
6	HV_{OUT} 27
7	HV_{OUT} 26
8	HV_{OUT} 25
9	HV_{OUT} 24
10	HV_{OUT} 23
11	HV_{OUT} 22
12	HV_{OUT} 21
13	HV_{OUT} 20
14	HV_{OUT} 19
15	HV_{OUT} 18
16	HV_{OUT} 17
17	HV_{OUT} 16
18	HV_{OUT} 15
19	HV_{OUT} 14
20	HV_{OUT} 13
21	HV_{OUT} 12
22	HV_{OUT} 11
23	HV_{OUT} 10
24	HV_{OUT} 9
25	HV_{OUT} 8
26	HV_{OUT} 7
27	HV_{OUT} 6
28	HV_{OUT} 5
29	HV_{OUT} 4
30	HV_{OUT} 3
31	HV_{OUT} 2
32	HV_{OUT} 1
33	OE
34	Data In
35	LE
36	V_{DD}
37	V_{PP}
38	V_{SS}
39	CLK
40	NC
41	Data Out

HV57

Pin	Function
1	HV_{OUT} 1
2	HV_{OUT} 2
3	HV_{OUT} 3
4	HV_{OUT} 4
5	HV_{OUT} 5
6	HV_{OUT} 6
7	HV_{OUT} 7
8	HV_{OUT} 8
9	HV_{OUT} 9
10	HV_{OUT} 10
11	HV_{OUT} 11
12	HV_{OUT} 12
13	HV_{OUT} 13
14	HV_{OUT} 14
15	HV_{OUT} 15
16	HV_{OUT} 16
17	HV_{OUT} 17
18	HV_{OUT} 18
19	HV_{OUT} 19
20	HV_{OUT} 20
21	HV_{OUT} 21
22	HV_{OUT} 22
23	HV_{OUT} 23
24	HV_{OUT} 24
25	HV_{OUT} 25
26	HV_{OUT} 26
27	HV_{OUT} 27
28	HV_{OUT} 28
29	HV_{OUT} 29
30	HV_{OUT} 30
31	HV_{OUT} 31
32	HV_{OUT} 32
33	Blanking
34	Data In
35	Latch Enable
36	V_{DD}
37	V_{PP}
38	V_{SS}
39	CLK
40	Polarity
41	Data Out

HV58

Pin	Function
1	HV_{OUT} 32
2	HV_{OUT} 31
3	HV_{OUT} 30
4	HV_{OUT} 29
5	HV_{OUT} 28
6	HV_{OUT} 27
7	HV_{OUT} 26
8	HV_{OUT} 25
9	HV_{OUT} 24
10	HV_{OUT} 23
11	HV_{OUT} 22
12	HV_{OUT} 21
13	HV_{OUT} 20
14	HV_{OUT} 19
15	HV_{OUT} 18
16	HV_{OUT} 17
17	HV_{OUT} 16
18	HV_{OUT} 15
19	HV_{OUT} 14
20	HV_{OUT} 13
21	HV_{OUT} 12
22	HV_{OUT} 11
23	HV_{OUT} 10
24	HV_{OUT} 9
25	HV_{OUT} 8
26	HV_{OUT} 7
27	HV_{OUT} 6
28	HV_{OUT} 5
29	HV_{OUT} 4
30	HV_{OUT} 3
31	HV_{OUT} 2
32	HV_{OUT} 1
33	Blanking
34	Data In
35	Latch Enable
36	V_{DD}
37	V_{PP}
38	V_{SS}
39	CLK
40	Polarity
41	Data Out



Pad Coordinates in Microns

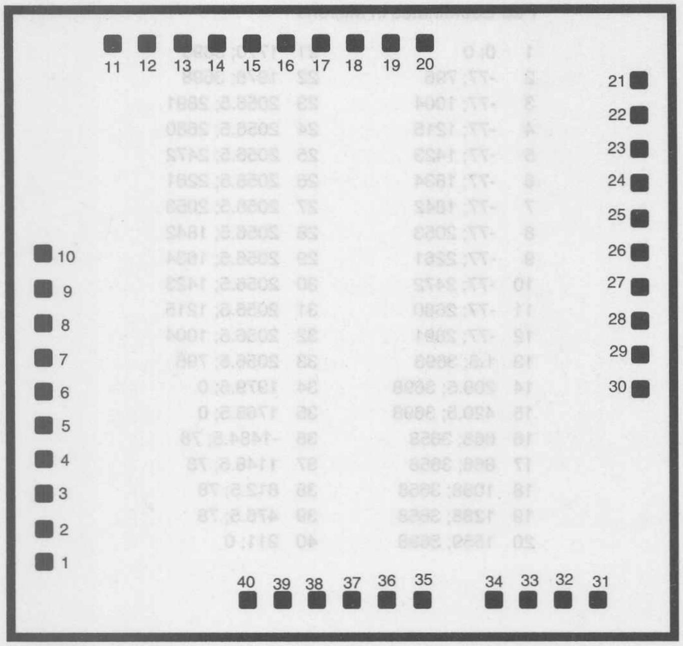
1	0; 0	21	3451; 2816
2	0; 200	22	3451; 2616
3	0; 400	23	3451; 2416
4	0; 600	24	3451; 2216
5	0; 800	25	3451; 2016
6	0; 1000	26	3451; 1816
7	0; 1200	27	3451; 1616
8	0; 1400	28	3451; 1416
9	0; 1600	29	3451; 1216
10	0; 1800	30	3451; 1016
11	406; 3030	31	3195; -228
12	606; 3030	32	2995; -228
13	806; 3030	33	2795; -228
14	1006; 3030	34	2595; -228
15	1206; 3030	35	2174; -228
16	1406; 3030	36	1974; -228
17	1606; 3030	37	1774; -228
18	1806; 3030	38	1574; -228
19	2006; 3030	39	1374; -228
20	2206; 3030	40	1174; -228

HV500

Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	4Q1	11	3Q3	21	2Q6	31	1Q4
2	4Q2	12	3Q4	22	2Q5	32	1Q3
3	4Q3	13	3Q5	23	2Q4	33	1Q2
4	4Q4	14	3Q6	24	2Q3	34	1Q1
5	4Q5	15	3Q7	25	2Q2	35	Clock
6	4Q6	16	3Q8	26	2Q1	36	Data In
7	4Q7	17	V_{PP}	27	1Q8	37	Select
8	4Q8	18	GND	28	1Q7	38	V_{DD}
9	3Q1	19	2Q8	29	1Q6	39	Select 1
10	3Q2	20	2Q7	30	1Q5	40	Strobe

Die Specifications

	mils	mm		
Die Size:	153 x 146	3.880 x 3.700	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4.5 x 4.5	0.11 x 0.11	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		



Pad Coordinates in Microns

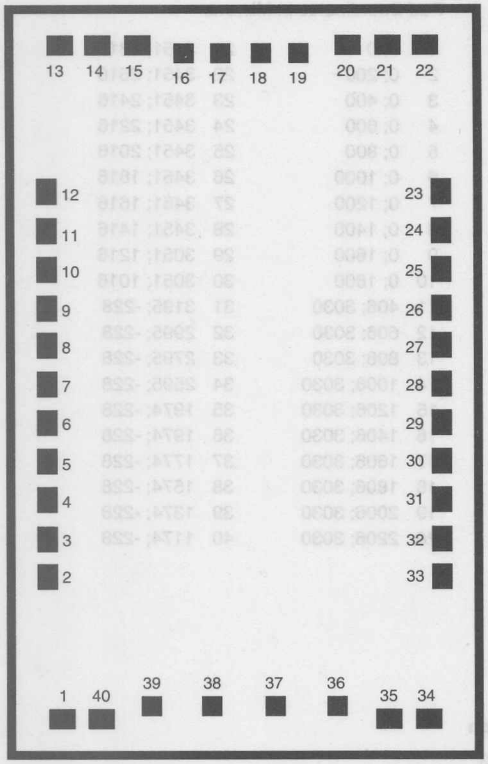
1	0; 0	21	3451; 2816
2	0; 200	22	3451; 2616
3	0; 400	23	3451; 2416
4	0; 600	24	3451; 2216
5	0; 800	25	3451; 2016
6	0; 1000	26	3451; 1816
7	0; 1200	27	3451; 1616
8	0; 1400	28	3451; 1416
9	0; 1600	29	3051; 1216
10	0; 1800	30	3051; 1016
11	406; 3030	31	3195; -228
12	606; 3030	32	2995; -228
13	806; 3030	33	2795; -228
14	1006; 3030	34	2595; -228
15	1206; 3030	35	1974; -228
16	1406; 3030	36	1974; -228
17	1606; 3030	37	1774; -228
18	1806; 3030	38	1574; -228
19	2006; 3030	39	1374; -228
20	2206; 3030	40	1174; -228

HV501

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HV_{OUT} 32	12	HV_{OUT} 21	22	HV_{OUT} 13	32	HV_{OUT} 3
2	HV_{OUT} 31	13	HV_{OUT} 20	23	HV_{OUT} 12	33	HV_{OUT} 2
3	HV_{OUT} 30	14	HV_{OUT} 19	24	HV_{OUT} 11	34	HV_{OUT} 1
4	HV_{OUT} 29	15	HV_{OUT} 18	25	HV_{OUT} 10	35	Strobe
6	HV_{OUT} 27	16	HV_{OUT} 17	26	HV_{OUT} 9	36	Sustain
7	HV_{OUT} 26	17	V_{PP}	27	HV_{OUT} 8	37	Clock
8	HV_{OUT} 25	18	GND	28	HV_{OUT} 7	38	V_{DD}
9	HV_{OUT} 24	19	HV_{OUT} 16	29	HV_{OUT} 6	39	Data in
10	HV_{OUT} 23	20	HV_{OUT} 15	30	HV_{OUT} 5	40	Data out
11	HV_{OUT} 22	21	HV_{OUT} 14	31	HV_{OUT} 4		

Die Specifications

	mils			mm				
Die Size:	153	x	146	3.880	x	3.700	**Back Side Metal:**	None
Die Thickness:	20 ±1			0.50 ±0.02			**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4.5	x	4.5	0.11	x	0.11	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3			0.03				



Pad Coordinates in Microns

Pad	Coordinates	Pad	Coordinates
1	0; 0	21	1770; 3698
2	-77; 796	22	1978; 3698
3	-77; 1004	23	2056.5; 2891
4	-77; 1215	24	2056.5; 2680
5	-77; 1423	25	2056.5; 2472
6	-77; 1634	26	2056.5; 2261
7	-77; 1842	27	2056.5; 2053
8	-77; 2053	28	2056.5; 1842
9	-77; 2261	29	2056.5; 1634
10	-77; 2472	30	2056.5; 1423
11	-77; 2680	31	2056.5; 1215
12	-77; 2891	32	2056.5; 1004
13	1.5; 3698	33	2056.5; 796
14	209.5; 3698	34	1979.5; 0
15	420.5; 3698	35	1768.5; 0
16	668; 3658	36	-1484.5; 78
17	868; 3658	37	1148.5; 78
18	1088; 3658	38	812.5; 78
19	1288; 3658	39	476.5; 78
20	1559; 3698	40	211; 0

HV518

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HV_{OUT} 18	11	HV_{OUT} 28	21	HV_{OUT} 2	31	HV_{OUT} 12
2	HV_{OUT} 19	12	HV_{OUT} 29	22	HV_{OUT} 3	32	HV_{OUT} 13
3	HV_{OUT} 20	13	HV_{OUT} 30	23	HV_{OUT} 4	33	HV_{OUT} 14
4	HV_{OUT} 21	14	HV_{OUT} 31	24	HV_{OUT} 5	34	HV_{OUT} 15
5	HV_{OUT} 22	15	HV_{OUT} 32	25	HV_{OUT} 6	35	HV_{OUT} 16
6	HV_{OUT} 23	16	Serial out	26	HV_{OUT} 7	36	Latch Enable
7	HV_{OUT} 24	17	V_{PP}	27	HV_{OUT} 8	37	Clock
8	HV_{OUT} 25	18	V_{DD}	28	HV_{OUT} 9	38	GND
9	HV_{OUT} 26	19	Data In	29	HV_{OUT} 10	39	Strobe
10	HV_{OUT} 27	20	HV_{OUT} 1	30	HV_{OUT} 11	40	HV_{OUT} 17

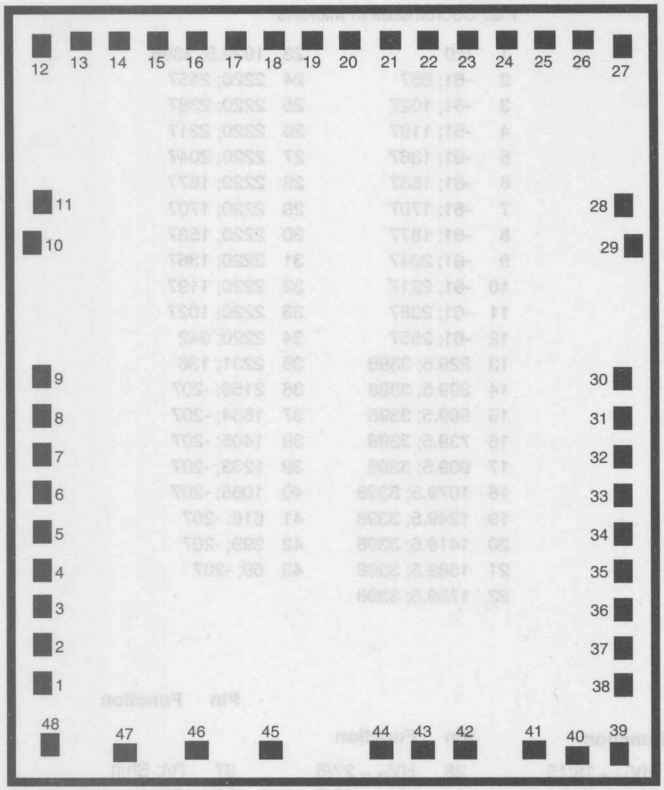
Die Specifications

	mils	mm		
Die Size:	101 x 163	2.560 x 4.140	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

Backside is V_{PP}

Supertex inc.

Die Specifications



Pad Coordinates in Microns

1	-53.5; 450	25	3593; 5142.5
2	-53.5; 730	26	3872; 5142.5
3	-53.5; 1010	27	4148.5; 5109.5
4	-53.5; 1290	28	4154.4; 3952
5	-53.5; 1570	29	4218; 3662
6	053; 1850	30	4146.5; 2690
7	-53.5; 2130	31	4146.5; 2409
8	-53.5; 2410	32	4146.5; 2130
9	-53.5; 2690	33	4146.5; 1849
10	-120; 3676.5	34	4146.5; 1570
11	-45; 3966	35	4146.5; 1289
12	-45; 3966	36	4146.5; 1010
13	223; 5142.5	37	4146.5; 729
14	512; 5142.5	38	4146.5; 450
15	793; 5142.5	39	4092.5; -30
16	1072; 5142.5	40	3801; -70.5
17	1353; 5142.5	41	3491; -32.5
18	1632; 5142.5	42	3007; -32.5
19	1913; 5142.5	43	2702; -32.5
20	2192; 5142.5	44	2392; -32.5
21	2473; 5142.5	45	1599; -32.5
22	2752; 5142.5	46	1060; -32.5
23	3033; 5142.5	47	537.5; -61
24	3312; 5142.5	48	0; 0

HV60

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HV_{OUT} 1	11	V_{NN}	21	HV_{OUT} 18	31	HV_{OUT} 25	41	V_{DD}(2)+5
2	HV_{OUT} 2	12	GND	22	HV_{OUT} 19	32	HV_{OUT} 26	42	ENABLE
3	HV_{OUT} 3	13	HV_{OUT} 10	23	HV_{OUT} 20	33	HV_{OUT} 27	43	V_{DD}(1)-5
4	HV_{OUT} 4	14	HV_{OUT} 11	24	HV_{OUT} 21	34	HV_{OUT} 28	44	$\overline{\text{CLEAR}}$
5	HV_{OUT} 5	15	HV_{OUT} 12	25	HV_{OUT} 22	35	HV_{OUT} 29	45	CLOCK
6	HV_{OUT} 6	16	HV_{OUT} 13	26	HV_{OUT} 23	36	HV_{OUT} 30	46	PHASE SHIFT
7	HV_{OUT} 7	17	HV_{OUT} 14	27	GND	37	HV_{OUT} 31	47	GND
8	HV_{OUT} 8	18	HV_{OUT} 15	28	V_{NN}	38	HV_{OUT} 32	48	DATA IN
9	HV_{OUT} 9	19	HV_{OUT} 16	29	V_{PP}	39	DATA OUT		
10	V_{PP}	20	HV_{OUT} 17	30	HV_{OUT} 24	40	GND		

Die Specifications

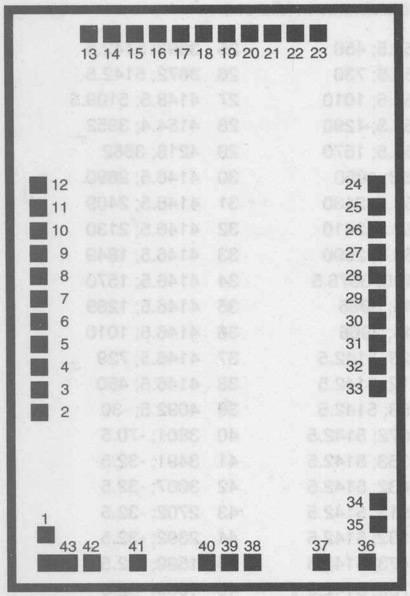
	mils			mm			
Die Size:	184	x	224	4.670	x	5.680	**Back Side Metal:** None
Die Thickness:	20 ±1			0.50 ±0.02			**Die Attach Material:** Epoxy Ablestick 84-1 or equal
Bond Pad Size:	4	x	4	0.10	x	0.10	**Bond Pad Metal:** Al/Si
Bond Wire Size:	1.3			0.03			

Back side is GND

17

Supertex inc.

Die Specifications



Pad Coordinates in Microns

1	0;0	23	1929.5; 3398
2	-61; 857	24	2220; 2557
3	-61; 1027	25	2220; 2387
4	-61; 1197	26	2220; 2217
5	-61; 1367	27	2220; 2047
6	-61; 1537	28	2220; 1877
7	-61; 1707	29	2220; 1707
8	-61; 1877	30	2220; 1537
9	-61; 2047	31	2220; 1367
10	-61; 2217	32	2220; 1197
11	-61; 2387	33	2220; 1027
12	-61; 2557	34	2220; 342
13	229.5; 3398	35	2231; 136
14	399.5; 3398	36	2158; -207
15	569.5; 3398	37	1854; -207
16	739.5; 3398	38	1405; -207
17	909.5; 3398	39	1233; -207
18	1079.5; 3398	40	1065; -207
19	1249.5; 3398	41	616; -207
20	1419.5; 3398	42	299; -207
21	1589.5; 3398	43	69; -207
22	1759.5; 3398		

HV6506

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Data Out	10	HV_{OUT} 9/24	19	HV_{OUT} 18/15	28	HV_{OUT} 27/6	37	R/L Shift
2	HV_{OUT} 1/32	11	HV_{OUT} 10/23	20	HV_{OUT} 19/14	29	HV_{OUT} 28/5	38	Clock
3	HV_{OUT} 2/31	12	HV_{OUT} 11/22	21	HV_{OUT} 20/13	30	HV_{OUT} 29/4	39	V_{DD}
4	HV_{OUT} 3/30	13	HV_{OUT} 12/21	22	HV_{OUT} 21/12	31	HV_{OUT} 30/3	40	LE
5	HV_{OUT} 4/29	14	HV_{OUT} 13/20	23	HV_{OUT} 22/11	32	HV_{OUT} 31/2	41	POL
6	HV_{OUT} 5/28	15	HV_{OUT} 14/19	24	HV_{OUT} 23/10	33	HV_{OUT} 32/1	42	N/C
7	HV_{OUT} 6/27	16	HV_{OUT} 15/18	25	HV_{OUT} 24/9	34	BP_{OUT}	43	GND
8	HV_{OUT} 7/26	17	HV_{OUT} 16/17	26	HV_{OUT} 25/8	35	V_{PP}		
9	HV_{OUT} 8/25	18	HV_{OUT} 17/16	27	HV_{OUT} 26/7	36	Data In		

Note: Pad designation for F/L shift = H/L.

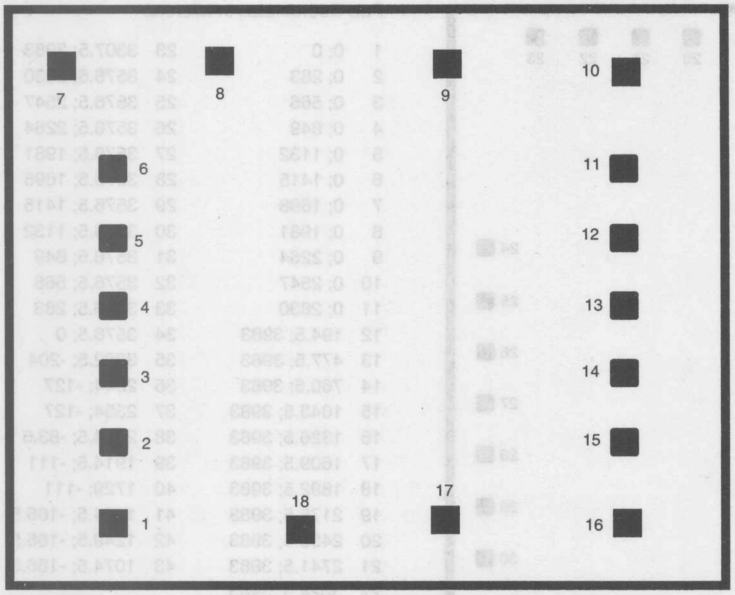
Die Specifications

	mils			mm				
Die Size:	105	x	160	2.625	x	4.000	**Back Side Metal:**	None
Die Thickness:	20 ±1			0.50 ±0.02			**Die Attach Material:**	Ablestick 84-1
Bond Pad Size:	4	x	4	0.10	x	0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3			0.03				

Supertex inc.

HV6810

Die Specifications



Pad Coordinates in Microns

1	0; 0
2	-4.5; 262.5
3	-4.5; 483.5
4	-4.5; 704.5
5	-4.5; 925.5
6	-4.5; 1146.5
7	-161; 1484
8	347; 1499
9	1069; 1484
10	1646; 1466
11	1640.5; 1146.5
12	1640.5; 925.5
13	1640.5; 704.5
14	1640.5; 483.5
15	1640.5; 262.5
16	1650; 0
17	1069; 14
18	599; -18

HV6810

Pin	Function	Pin	Function
1	Clock	10	Blanking
2	Q6	11	Q1
3	Q7	12	Q2
4	Q8	13	Q3
5	Q9	14	Q4
6	Q10	15	Q5
7	Serial Data out	16	STB
8	V_{BB}	17	V_{DD}
9	Serial Data out	18	V_{SS}

Die Specifications

	mils	mm		
Die Size:	76 x 93	1.930 x 2.360	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

17

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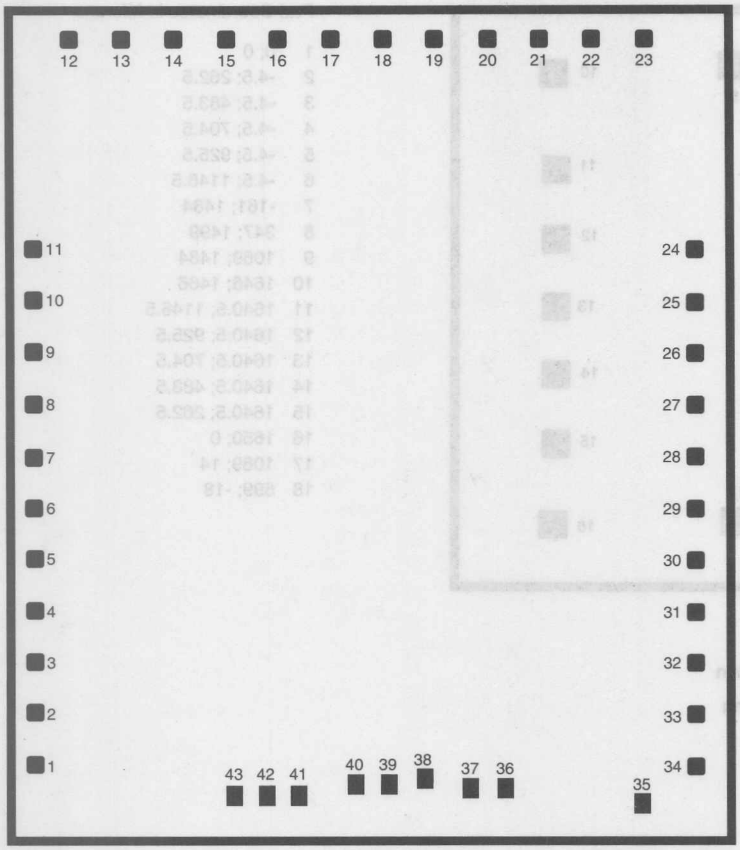
HV70

Die Specifications



Pad Coordinates in Microns

1	0; 0	23	3307.5; 3983
2	0; 283	24	3576.5; 2830
3	0; 566	25	3576.5; 2547
4	0; 849	26	3576.5; 2264
5	0; 1132	27	3576.5; 1981
6	0; 1415	28	3576.5; 1698
7	0; 1698	29	3576.5; 1415
8	0; 1981	30	3576.5; 1132
9	0; 2264	31	3576.5; 849
10	0; 2547	32	3576.5; 566
11	0; 2830	33	3576.5; 283
12	194.5; 3983	34	3576.5; 0
13	477.5; 3983	35	3282.5; -204
14	760.5; 3983	36	2544; -127
15	1043.5; 3983	37	2354; -127
16	1326.5; 3983	38	2104.5; -83.5
17	1609.5; 3983	39	1914.5; -111
18	1892.5; 3983	40	1729; -111
19	2175.5; 3983	41	1424.5; -166.5
20	2458.5; 3983	42	1249.5; -166.5
21	2741.5; 3983	43	1074.5; -166.5
22	3024.5; 3983		

HV70[1]

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HV_{OUT}1/34	8	HV_{OUT}8/27	15	HV_{OUT}15/20	22	HV_{OUT}22/13	29	HV_{OUT}29/6	36	Data In
2	HV_{OUT}2/33	9	HV_{OUT}9/26	16	HV_{OUT}16/19	23	HV_{OUT}23/12	30	HV_{OUT}30/5	37	POL
3	HV_{OUT}3/32	10	HV_{OUT}10/25	17	HV_{OUT}17/18	24	HV_{OUT}24/11	31	HV_{OUT}31/4	38	V_{DD}
4	HV_{OUT}4/31	11	HV_{OUT}11/24	18	HV_{OUT}18/17	25	HV_{OUT}25/10	32	HV_{OUT}32/3	39	DIR
5	HV_{OUT}5/30	12	HV_{OUT}12/23	19	HV_{OUT}19/16	26	HV_{OUT}26/9	33	HV_{OUT}33/2	40	GND
6	HV_{OUT}6/29	13	HV_{OUT}13/22	20	HV_{OUT}20/15	27	HV_{OUT}27/8	34	HV_{OUT}34/1	41	CLK
7	HV_{OUT}7/28	14	HV_{OUT}14/21	21	HV_{OUT}21/14	28	HV_{OUT}28/7	35	V_{PP}	42	OE
										43	Data Out

Die Specifications

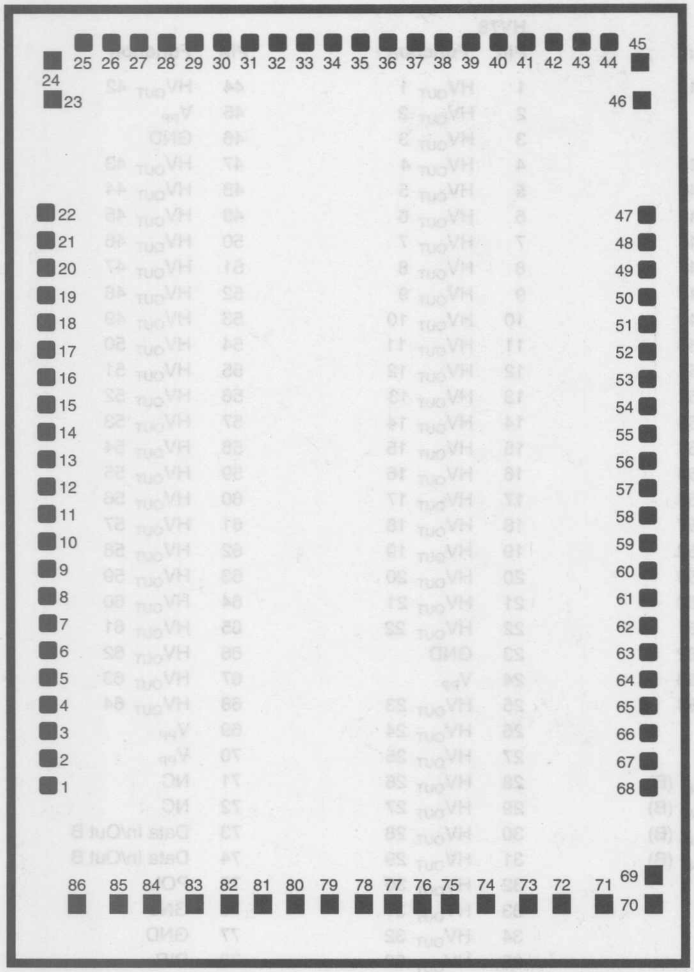
	mils			mm				
Die Size:	155	x	180	3.930	x	4.570	**Back Side Metal:**	None
Die Thickness:	20 ±1			0.50 ±0.02			**Die Attach Material:**	Ablestick 84-1 or equal
Bond Pad Size:	4	x	4	0.10	x	0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3			0.03				

1 DIR = H PIN 1 = HV_{OUT}1; DIR = L PIN 1 = HV_{OUT} 34

2 Backside is V_{PP}

Supertex inc.

Die Specifications



Pad Coordinates in Microns

1	0; 0	44	3253; 4367
2	0; 160	45	3431.5; 4249.5
3	0; 320	46	3436; 4024
4	0; 480	47	3466; 3360
5	0; 640	48	3466; 3200
6	0; 800	49	3466; 3040
7	0; 960	50	3466; 2880
8	0; 1120	51	3466; 2720
9	0; 1280	52	3466; 2560
10	0; 1440	53	3466; 2400
11	0; 1600	54	3466; 2240
12	0; 1760	55	3466; 2080
13	0; 1920	56	3466; 1920
14	0; 2080	57	3466; 1760
15	0; 2240	58	3466; 1600
16	0; 2400	59	3466; 1440
17	0; 2560	60	3466; 1280
18	0; 2720	61	3466; 1120
19	0; 2880	62	3466; 960
20	0; 3040	63	3466; 800
21	0; 3200	64	3466; 640
22	0; 3360	65	3466; 480
23	30; 4024	66	3466; 320
24	34.5; 4249.5	67	3466; 160
25	213; 4367	68	3466; 0
26	373; 4367	69	3497.5; -509.5
27	533; 4367	70	3497.5; -684.5
28	693; 4367	71	3208.5; - 693.5
29	853; 4367	72	2966.5; -693.5
30	1013; 4367	73	2768.5; -693.5
31	1173; 4367	74	2526.5; -693.5
32	1333; 4367	75	2324.5; -693.5
33	1493; 4367	76	2161; -693.5
34	1653; 4367	77	1986; -693.5
35	1813; 4367	78	1823.5; -693.5
36	1973; 4367	79	1624; -693.5
37	2133; 4367	80	1424.5; -693.5
38	2293; 4367	81	1235.5; -693.5
39	2453; 4367	82	1044.5; -693.5
40	2613; 4367	83	842.5; -693.5
41	2773; 4367	84	600.5; - 693.5
42	2933; 4367	85	402.5; -693.5
43	3093; 4367	86	160.5; -693.5

Notes:

1. HV_{OUT} location is dependent on DIR pin. The label above is for DIR high.
2. Backside is V_{PP}
3. For I_{PP} > 1.5A use pads 23, 46 for GND and pads 24, 45 for V_{PP}

Die Specifications

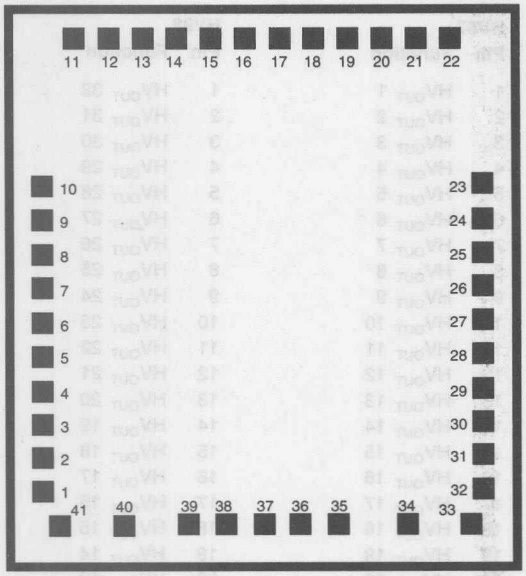
	mils	mm		
Die Size:	155 x 222	3.930 x 5.630	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV77

Pin	Function	Pin	Function
1	HV_{OUT} 1	44	HV_{OUT} 42
2	HV_{OUT} 2	45	V_{PP}
3	HV_{OUT} 3	46	GND
4	HV_{OUT} 4	47	HV_{OUT} 43
5	HV_{OUT} 5	48	HV_{OUT} 44
6	HV_{OUT} 6	49	HV_{OUT} 45
7	HV_{OUT} 7	50	HV_{OUT} 46
8	HV_{OUT} 8	51	HV_{OUT} 47
9	HV_{OUT} 9	52	HV_{OUT} 48
10	HV_{OUT} 10	53	HV_{OUT} 49
11	HV_{OUT} 11	54	HV_{OUT} 50
12	HV_{OUT} 12	55	HV_{OUT} 51
13	HV_{OUT} 13	56	HV_{OUT} 52
14	HV_{OUT} 14	57	HV_{OUT} 53
15	HV_{OUT} 15	58	HV_{OUT} 54
16	HV_{OUT} 16	59	HV_{OUT} 55
17	HV_{OUT} 17	60	HV_{OUT} 56
18	HV_{OUT} 18	61	HV_{OUT} 57
19	HV_{OUT} 19	62	HV_{OUT} 58
20	HV_{OUT} 20	63	HV_{OUT} 59
21	HV_{OUT} 21	64	HV_{OUT} 60
22	HV_{OUT} 22	65	HV_{OUT} 61
23	GND	66	HV_{OUT} 62
24	V_{PP}	67	HV_{OUT} 63
25	HV_{OUT} 23	68	HV_{OUT} 64
26	HV_{OUT} 24	69	V_{PP}
27	HV_{OUT} 25	70	V_{PP}
28	HV_{OUT} 26	71	$D_{OUT}1/_{IN}4$ (B)
29	HV_{OUT} 27	72	$D_{OUT}2/_{IN}3$ (B)
30	HV_{OUT} 28	73	$D_{OUT}3/_{IN}2$ (B)
31	HV_{OUT} 29	74	$D_{OUT}4/_{IN}1$ (B)
32	HV_{OUT} 30	75	POL
33	HV_{OUT} 31	76	GND
34	HV_{OUT} 32	77	GND
35	HV_{OUT} 33	78	DIR
36	HV_{OUT} 34	79	V_{DD}
37	HV_{OUT} 35	80	Blanking
38	HV_{OUT} 36	81	CLK
39	HV_{OUT} 37	82	LE
40	HV_{OUT} 38	83	$D_{IN}4/_{OUT}1$ (A)
41	HV_{OUT} 39	84	$D_{IN}3/_{OUT}2$ (A)
42	HV_{OUT} 40	85	$D_{IN}2/_{OUT}3$ (A)
43	HV_{OUT} 41	86	$D_{IN}1/_{OUT}4$ (A)

HV78

Pin	Function	Pin	Function
1	HV_{OUT} 1	44	HV_{OUT} 42
2	HV_{OUT} 2	45	V_{PP}
3	HV_{OUT} 3	46	GND
4	HV_{OUT} 4	47	HV_{OUT} 43
5	HV_{OUT} 5	48	HV_{OUT} 44
6	HV_{OUT} 6	49	HV_{OUT} 45
7	HV_{OUT} 7	50	HV_{OUT} 46
8	HV_{OUT} 8	51	HV_{OUT} 47
9	HV_{OUT} 9	52	HV_{OUT} 48
10	HV_{OUT} 10	53	HV_{OUT} 49
11	HV_{OUT} 11	54	HV_{OUT} 50
12	HV_{OUT} 12	55	HV_{OUT} 51
13	HV_{OUT} 13	56	HV_{OUT} 52
14	HV_{OUT} 14	57	HV_{OUT} 53
15	HV_{OUT} 15	58	HV_{OUT} 54
16	HV_{OUT} 16	59	HV_{OUT} 55
17	HV_{OUT} 17	60	HV_{OUT} 56
18	HV_{OUT} 18	61	HV_{OUT} 57
19	HV_{OUT} 19	62	HV_{OUT} 58
20	HV_{OUT} 20	63	HV_{OUT} 59
21	HV_{OUT} 21	64	HV_{OUT} 60
22	HV_{OUT} 22	65	HV_{OUT} 61
23	GND	66	HV_{OUT} 62
24	V_{PP}	67	HV_{OUT} 63
25	HV_{OUT} 23	68	HV_{OUT} 64
26	HV_{OUT} 24	69	V_{PP}
27	HV_{OUT} 25	70	V_{PP}
28	HV_{OUT} 26	71	NC
29	HV_{OUT} 27	72	NC
30	HV_{OUT} 28	73	Data In/Out B
31	HV_{OUT} 29	74	Data In/Out B
32	HV_{OUT} 30	75	POL
33	HV_{OUT} 31	76	GND
34	HV_{OUT} 32	77	GND
35	HV_{OUT} 33	78	DIR
36	HV_{OUT} 34	79	V_{DD}
37	HV_{OUT} 35	80	Blanking
38	HV_{OUT} 36	81	CLK
39	HV_{OUT} 37	82	LE
40	HV_{OUT} 38	83	NC
41	HV_{OUT} 39	84	NC
42	HV_{OUT} 40	85	Data In/Out A
43	HV_{OUT} 41	86	Data In/Out A



Pad Coordinates in Microns

1	0; 0	22	1959.5; 2190
2	0;164	23	2115; 1476
3	0; 328	24	2115; 1312
4	0; 492	25	2115; 1148
5	0;656	26	2115; 984
6	0; 820	27	2115; 820
7	0; 984	28	2115; 656
8	0; 1148	29	2115; 492
9	0; 1312	30	2115; 328
10	0; 1476	31	2115; 164
11	155.5; 2190	32	2115; 0
12	319.5; 2190	33	2056; -177
13	483.5; 2190	34	1741.5; -182
14	647.5; 2190	35	-1406; -177
15	811.5; 2190	36	1228.5; -177
16	975.5; 2190	37	1051; -177
17	1139.5; 2190	38	867.5; -177
18	1303.5; 2190	39	685; -177
19	1467.5; 2190	40	376.5; -182
20	1631.5; 2190	41	69; -177
21	1795.5; 2190		

Die Specifications

	mils	mm		
Die Size:	97 x 109	2.463 x 2.768	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 or Equal
Bond Pad Size:	4 x 4	0.10 x 0.10	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.3	0.03		

HV83

Pin	Function
1	HV_{OUT} 1
2	HV_{OUT} 2
3	HV_{OUT} 3
4	HV_{OUT} 4
5	HV_{OUT} 5
6	HV_{OUT} 6
7	HV_{OUT} 7
8	HV_{OUT} 8
9	HV_{OUT} 9
10	HV_{OUT} 10
11	HV_{OUT} 11
12	HV_{OUT} 12
13	HV_{OUT} 13
14	HV_{OUT} 14
15	HV_{OUT} 15
16	HV_{OUT} 16
17	HV_{OUT} 17
18	HV_{OUT} 18
19	HV_{OUT} 19
20	HV_{OUT} 20
21	HV_{OUT} 21
22	HV_{OUT} 22
23	HV_{OUT} 23
24	HV_{OUT} 24
25	HV_{OUT} 25
26	HV_{OUT} 26
27	HV_{OUT} 27
28	HV_{OUT} 28
29	HV_{OUT} 29
30	HV_{OUT} 30
31	HV_{OUT} 31
32	HV_{OUT} 32
33	OE
34	Data In
35	LE
36	V_{DD}
37	V_{PP}
38	GND
39	CLK
40	NC
41	Data Out

HV84

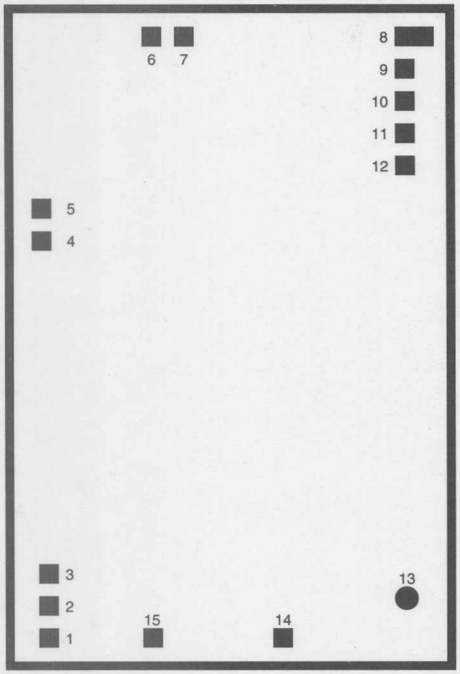
Pin	Function
1	HV_{OUT} 32
2	HV_{OUT} 31
3	HV_{OUT} 30
4	HV_{OUT} 29
5	HV_{OUT} 28
6	HV_{OUT} 27
7	HV_{OUT} 26
8	HV_{OUT} 25
9	HV_{OUT} 24
10	HV_{OUT} 23
11	HV_{OUT} 22
12	HV_{OUT} 21
13	HV_{OUT} 20
14	HV_{OUT} 19
15	HV_{OUT} 18
16	HV_{OUT} 17
17	HV_{OUT} 16
18	HV_{OUT} 15
19	HV_{OUT} 14
20	HV_{OUT} 13
21	HV_{OUT} 12
22	HV_{OUT} 11
23	HV_{OUT} 10
24	HV_{OUT} 9
25	HV_{OUT} 8
26	HV_{OUT} 7
27	HV_{OUT} 6
28	HV_{OUT} 5
29	HV_{OUT} 4
30	HV_{OUT} 3
31	HV_{OUT} 2
32	HV_{OUT} 1
33	OE
34	Data In
35	LE
36	V_{DD}
37	V_{PP}
38	GND
39	CLK
40	NC
41	Data Out

HV87

Pin	Function
1	HV_{OUT} 1
2	HV_{OUT} 2
3	HV_{OUT} 3
4	HV_{OUT} 4
5	HV_{OUT} 5
6	HV_{OUT} 6
7	HV_{OUT} 7
8	HV_{OUT} 8
9	HV_{OUT} 9
10	HV_{OUT} 10
11	HV_{OUT} 11
12	HV_{OUT} 12
13	HV_{OUT} 13
14	HV_{OUT} 14
15	HV_{OUT} 15
16	HV_{OUT} 16
17	HV_{OUT} 17
18	HV_{OUT} 18
19	HV_{OUT} 19
20	HV_{OUT} 20
21	HV_{OUT} 21
22	HV_{OUT} 22
23	HV_{OUT} 23
24	HV_{OUT} 24
25	HV_{OUT} 25
26	HV_{OUT} 26
27	HV_{OUT} 27
28	HV_{OUT} 28
29	HV_{OUT} 29
30	HV_{OUT} 30
31	HV_{OUT} 31
32	HV_{OUT} 32
33	Blanking
34	Data In
35	LE
36	V_{DD}
37	V_{PP}
38	GND
39	CLK
40	POL
41	Data Out

HV88

Pin	Function
1	HV_{OUT} 32
2	HV_{OUT} 31
3	HV_{OUT} 30
4	HV_{OUT} 29
5	HV_{OUT} 28
6	HV_{OUT} 27
7	HV_{OUT} 26
8	HV_{OUT} 25
9	HV_{OUT} 24
10	HV_{OUT} 23
11	HV_{OUT} 22
12	HV_{OUT} 21
13	HV_{OUT} 20
14	HV_{OUT} 19
15	HV_{OUT} 18
16	HV_{OUT} 17
17	HV_{OUT} 16
18	HV_{OUT} 15
19	HV_{OUT} 14
20	HV_{OUT} 13
21	HV_{OUT} 12
22	HV_{OUT} 11
23	HV_{OUT} 10
24	HV_{OUT} 9
25	HV_{OUT} 8
26	HV_{OUT} 7
27	HV_{OUT} 6
28	HV_{OUT} 5
29	HV_{OUT} 4
30	HV_{OUT} 3
31	HV_{OUT} 2
32	HV_{OUT} 1
33	Blanking
34	Data In
35	LE
36	V_{DD}
37	V_{PP}
38	GND
39	CLK
40	POL
41	Data Out



Pad Coordinates in Microns

1	0; 0
2	10; 168
3	10; 328
4	10; 1600.5
5	10; 1793.5
6	330; 2288
7	490; 2288
8	1300.5; 2341
9	1261; 2181
10	1261; 2021
11	1261; 1861
12	1261; 1665
13	1193; 83.5
14	814; -14
15	394; -14

HV91

Pin	**Function**	**Pin**	**Function**
1	COMP	9	$-V_{IN}$
2	Reset	10	NC
3	Shutdown	11	Output
4	V_{REF}	12	Sense
5	Discharge	13	$+V_{IN}$
6	OSC IN	14	BIAS
7	OSC OUT	15	FB
8	V_{DD}		

Die Specifications

	mils	mm		
Die Size:	65 x 105	1.650 x 2.670	**Back Side Metal:**	None
Die Thickness:	20 ±1	0.50 ±0.02	**Die Attach Material:**	Epoxy Ablestick 84-1 LMIS
Bond Pad Size:	3.3 x 3.3	0.084 x 0.084	**Bond Pad Metal:**	Al/Si
Bond Wire Size:	1.25	0.032		